NXP Semiconductors
Application Note

Document Number: AN5085
Rev. 0, 07/2017

Powering the LS102xA with the MC34VR500 Power Management Interface Chip

1 Introduction

The MC34VR500 power management solution for network processor systems is a high-efficiency, quad buck regulator with up to 4.5 A output and five user-programmable LDOs. With four buck regulators and five LDO output channels, the MC34VR500 powers more than the network processor, significantly reducing design complexity and the overall bill of materials (BOM). The highly integrated MC34VR500 output voltage, frequency, and turn-on sequence are user programmable using I^2C.

The MC34VR500 is ideally suited to power system solutions based on QorIQ T1 and LS1 networking communications processors with unique programmable multiple buck regulators and LDOs. All regulators are internally compensated. Startup, slew rate control, and DVS are internally controlled, which means minimal external components are required.

This application note explains how to incorporate the MC34VR500 into an LS1 design. It uses the LS1021A-IOT as a design example.

Contents

2 Buck regulators and LDOs in the MC34VR500

This section describes how the MC34VR500 buck regulators and LDOs can be used in a LS102xA processor design.

The MC34VR500 has been designed to match the power rail requirements of the LS1021A processor. The single Power Management Interface Chip (PMIC) solution supplies all the LS1021A rails except for 3.3 V. As the MC34VR500 is supplied from a 3.3 V input supply, it can be used for the LS1 I/O, if necessary.

The LS1021A-IOT is a reference design that uses the MC34VR500V1ES. This figure shows how the MC34VR500 supplies the LS1021A rails and DDR3L memory, as well as peripheral devices in that design.

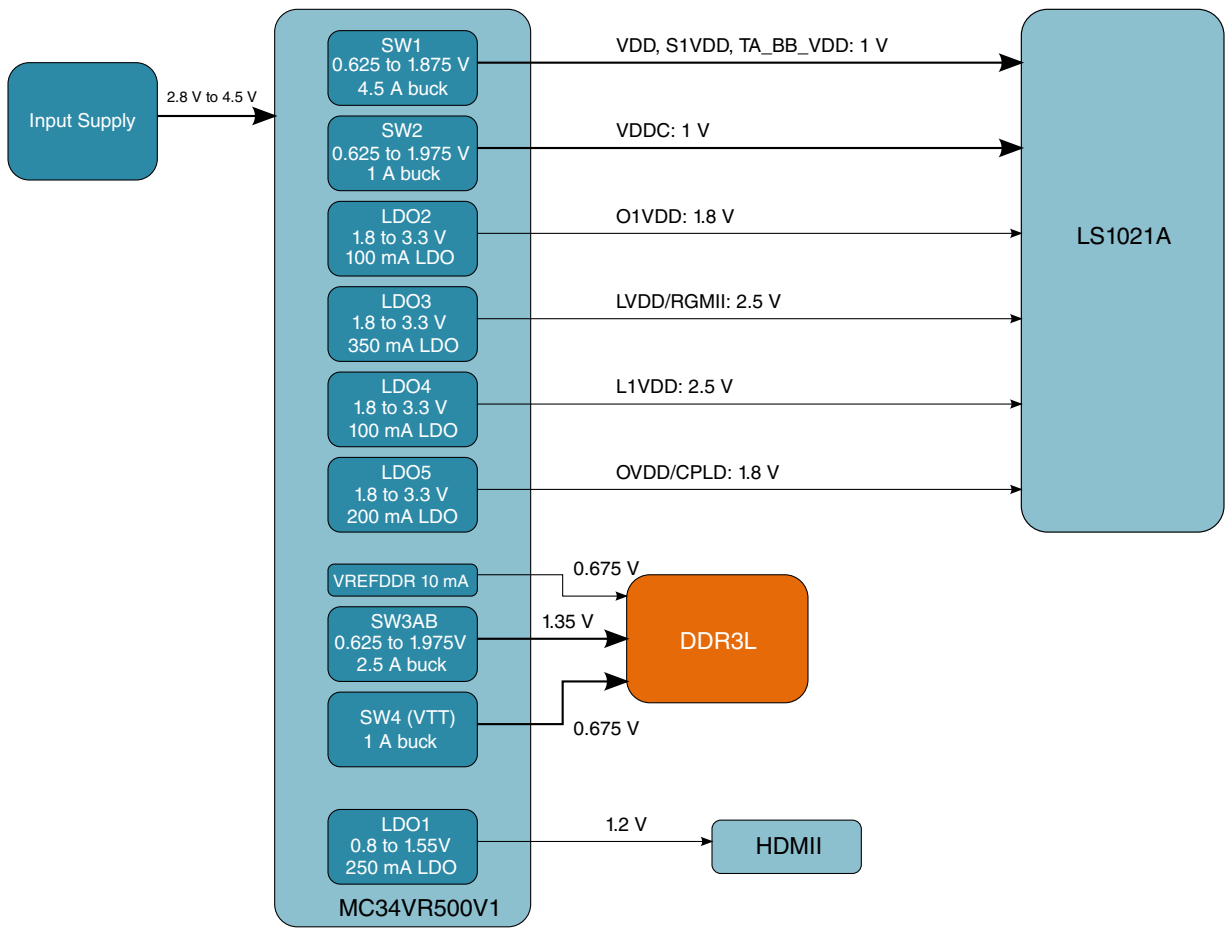


Figure 1. MC34VR500 powering the LS1021A-IOT gateway

2.1 Configuring buck regulators for LS102xA

The four buck regulators (SW1-4) on the MC34VR500 can produce high current outputs suitable for the LS102xA cores and DDR3 and DDR4 supplies:

- Use SW1 for the switchable core voltage and SW2 for the always on V_{DDC} supply.
- Use SW3 to generate the GV_{DD} for the LS1 and DDR devices.
- Use SW4 in its V_{TT} mode for DDR memory termination. In the V_{TT} mode:

- Its reference voltage internally tracks the output voltage of SW3, scaled by 0.5.
- Only the PWM switching mode is allowed to have sinking current capability.

There are three switching modes available for the buck's regulators:

1. Pulse Width Modulation (PWM): This mode allows continuous pulses generated by the internal MOSFETs, irrespective of the load current. This is the preferred mode of switching at load currents greater than 100 mA.
2. Pulse Frequency Modulation (PFM): In this mode, the switching frequency is proportional to the load current. Turn off the internal bottom MOSFET if the inductor current goes negative. This is the preferred mode at load currents less than 100 mA.
3. Auto Pulse Skip Mode (APS): This is the default mode in the MC34VR500. This offers a good compromise between PFM and PWM.

The switching frequency selections are: 1 MHz, 2 MHz, or 4 MHz (useful for certain applications with strict EMC requirement). By default, 2 MHz is used.

If we take a more detailed look at the LS1021A power requirements, we see that the MC34VR500 adequately meets the specification of the LS1021A core and DDR power requirements. We assume worst-case values that are taken from the data sheet.

The following tables summarize the voltage and current capabilities of the buck regulators with respect to the LS1021A requirements.

NOTE

The regulators max current is the normal operating maximum. Each regulator can handle instantaneous currents in excess of this. See the MC34VR500 data sheet for more information.

Table 1. SW1 (supplies V_{DD}, TA_BB_V_{DD}, S1V_{DD}, and USB_SxV_{DD})

LS1 rail			Regulator		
Rail name	**Voltage**	**Max current**	**Regulator name**	**Voltage**	**Max current**
V_{DD}	1.0 V ± 30 mV	3.06 A	SW1ABC	1.0 V ± 25 mV	4.5 A
TA_BB_V_{DD}		0.02 A			
S1V_{DD}		0.32 A			
USB1_SDV_{DD}		0.011 A			
USB1_SXV_{DD}		0.026 A			
USB1_SPV_{DD}		0.044 A			
	Total	3.891 A			

Table 2. SW2 (supplies V_{DDC} only)

LS1 rail			Regulator		
Rail name	**Voltage**	**Max current**	**Regulator name**	**Voltage**	**Max current**
V_{DDC}	1.0 V ± 30 mV	0.41 A	SW2	1.0 V ± 30 mV	2.0 A
	Total	0.41 A			

Table 3. SW3 (supplies GV_{DD} to the LS1 and DDR memories, SerDes PLLs, and SerDes)

LS1 rail			Regulator		
Rail name	**Voltage**	**Max current**	**Regulator name**	**Voltage**	**Max current**
GV_{DD} @ 1600 MHz	1.35 V ± 67 mV	0.883 A	SW3AB	1.35 V ± 67 mV	2.5 A
GV_{DD} DDR3L x3		0.973 A			
AV_{DD}_SD1_PLL1 AV_{DD}_SD1_PLL2		0.185 A			
$X1V_{DD}$		0.258 A			
	Total	2.3 A			

Table 4. SW4 (supplies V_{TT})

LS1 rail			Regulator		
Rail name	**Voltage**	**Max current**	**Regulator name**	**Voltage**	**Max current**
V_{TT}	0.675 V	~500 mA	SW4	0.675 V ± 40 mV	1.0 A

2.2 Configuring LDO1-LDO5 regulators

The five general-purpose LDO regulators in the MC34VR500 are suitable for the I/O voltages required by the LS102xA processors. All LDOs have a short circuit and over-current protection.

The following tables provide the voltage and current ratings of each regulator, as well as example peripherals on the LS1021A-IOT, such as PHYs, that would use the voltage rail.

Table 5. LDO1 (powers external HDMI peripheral)

Rail			Regulator		
1.2 V rail	**Voltage**	**Max current**	**Regulator name**	**Regulator voltage**	**Regulator max current**
HDMI	1.2 V ± 120 mV	65 mA	LDO1	1.2 V ± 36 mV	250 mA

Table 6. LDO2

Rail			Regulator		
Always On 1.8 V rail	**Voltage**	**Max current**	**Regulator name**	**Regulator voltage**	**Regulator max current**
$O1V_{DD}$	1.8 V ± 90 mV	12 mA	LDO2	1.8 V ± 54 mV	100 mA

Table 7. LDO3

Rail			Regulator		
2.5 V rails	**Voltage**	**Max current**	**Regulator name**	**Regulator voltage**	**Regulator max current**
LV_{DD} (assume 2x RGMII I/F)	2.5 V ± 125 mV	137 mA	LDO3	2.5 V ± 75 mV	350 mA
LV_{DD} (assume 2x RGMII I/F)		30 mA			
LV_{DD} (assume 2x RGMII I/F)		3 mA			
	Total	170 mA			

Table 8. LDO4

Rail			Regulator		
Always On 2.5 V rail	**Voltage**	**Max current**	**Regulator name**	**Regulator voltage**	**Regulator max current**
$L1V_{DD}$ (assume 1x RGMII I/F)	2.5 V ± 125 mV	69 mA	LDO4	2.5 V ± 75 mV	100 mA

Table 9. LDO5[1]

Rail			Regulator		
1.8 V rails	**Voltage**	**Max current**	**Regulator name**	**Regulator voltage**	**Regulator max current**
OV_{DD}	1.8 V ± 90 mV	12 mA	LDO5	1.8 V ± 54 mV	200 mA
AV_{DD}_CGA1 AV_{DD}_PLAT 1.8 V		69 mA			
AV_{DD}_D1 1.8 V		69 mA			
	Total	170 mA			

Note:

1. These regulators are straight forward to work with and require a single 4.7 uF output capacitor.

Table 10. REFOUT (VREF DDR)[1]

Rail			Regulator		
VREF rail	**Voltage**	**Max current**	**Regulator name**	**Regulator voltage**	**Regulator max current**
VREF	0.675 V ± 13.5 mV	500 uA	REFOUT	0.675 V ± 6.75 mV	10 mA

Note:

1. REFOUT is an internal PMOS half supply voltage follower capable of supplying up to 10 mA. The output voltage is at one half the input voltage. It is typically used as the reference voltage for DDR memories. A filtered resistor divider is used to create a low frequency pole. This divider then uses a voltage follower to drive the load.

3 Power sequence

The LS1021A requires that its power rails be applied in a specific sequence in order to ensure proper device operation. For details, refer to the Power sequencing section of LS1021A datasheet.

This figure shows the MC34VR500 pre-programmed power sequence. It has been implemented to match the previously discussed LS1 requirements.

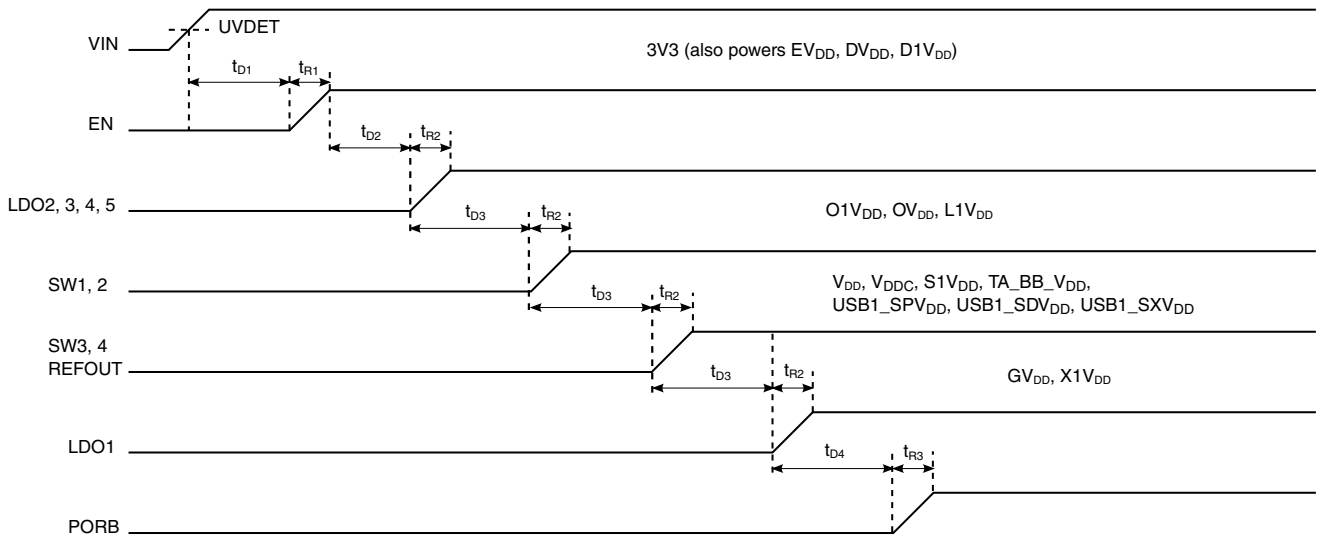


Figure 2. Starting sequence

Table 11. MC34VR500 start-up sequence timing

Parameter	Description	Typical	Unit
t_{D1}	Turn-on delay	Depends on the external signal driving EN	ms
t_{R1}	Rise time of EN	Depends on the external signal driving EN	ms
t_{D2}	Turn-on delay of first regulator	2.5	ms
t_{R2}	Rise time of regulators[1]	0.2	ms
t_{D3}	Delay between regulators	1.0	ms
t_{D4}	Turn-on delay of PORB	2.0	ms
t_{R3}	Rise time of PORB	0.2	ms

Note:

1. Rise time is a function of slew rate of regulators and nominal voltage selected.

4 Digital control

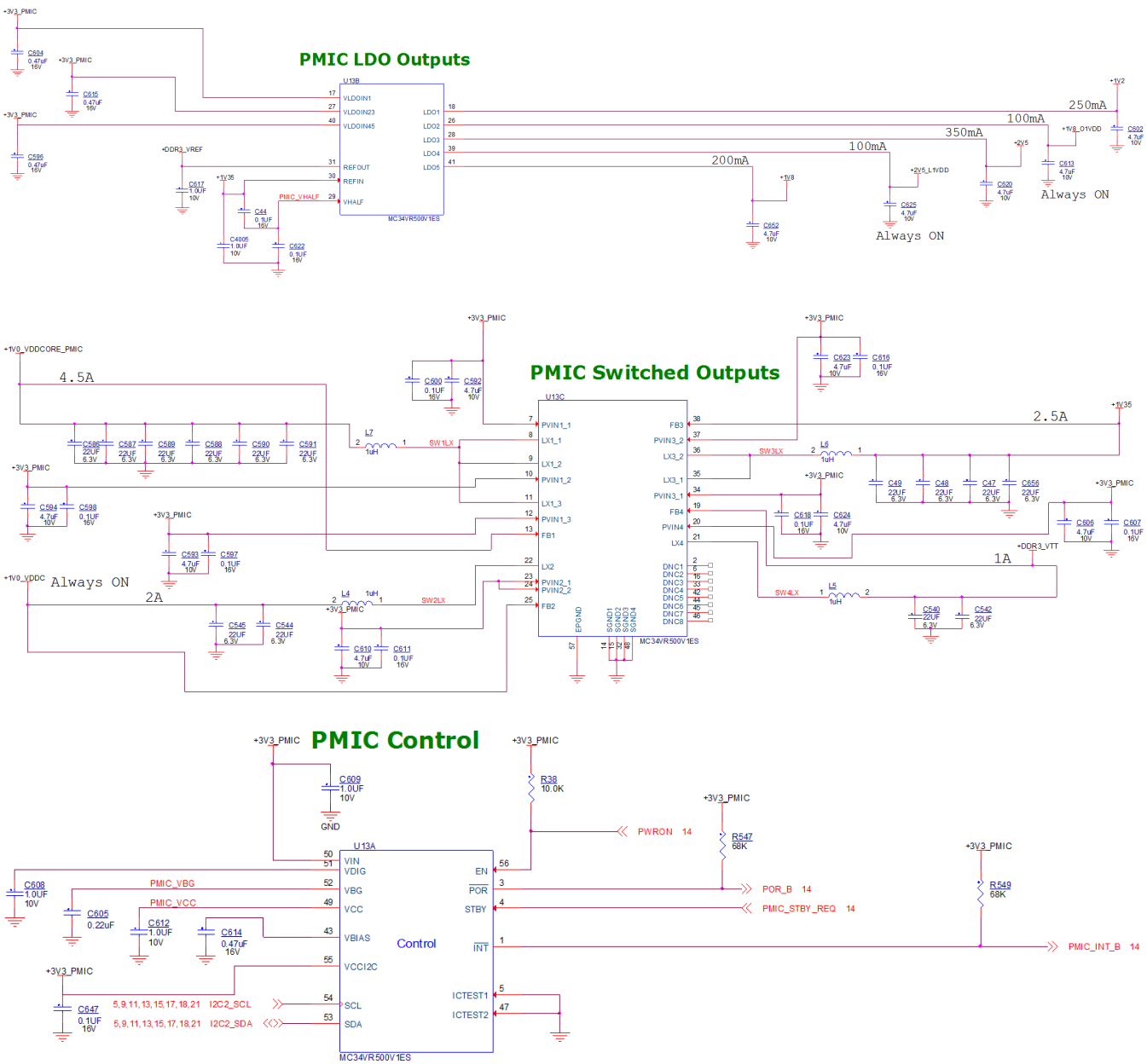
The MC34VR500 has an EN control pin to allow the system to control the startup of the device, for example, if it is part of a greater power tree. Typically, the device powers up with the One Time Programming (OTP) values stored in the device. You can also program and configure the MC34VR500 via the I^2C bus.

Additional communication is provided by direct logic interfacing, including interrupt and reset. Startup voltage and sequence are internally programmed. After power up, you can change the regulator voltages via the I^2C bus.

5 Schematic reference

The MC34VR500V1ES has been used successfully in the LS1021A-IOT design. The schematics are available for reference from http://www.nxp.com.

The following figures show the PMIC power schematics. See the MC34VR500 data sheet for recommended external component values for the PMIC.



Powering the LS102xA with the MC34VR500 Power Management Interface Chip, Rev. 0, 07/2017

6 References

This table provides URLs where you can obtain information on related NXP products and application solutions.

Table 12. References

Document number and description		URL
LS1021A	Data sheet	https://www.nxp.com/webapp/Download?colCode=LS1021A&location=null&fsrch=1&sr=1&pageNum=1amp;&Parent_nodeId=&Parent_pageType=&Parent_nodeId=&Parent_pageType=
MC34VR500	Data sheet	http://cache.nxp.com/docs/en/data-sheet/MC34VR500.pdf?pspll=1
AN5064	Schematic Guidelines for the MC34VR500	http://cache.nxp.com/docs/en/application-note/AN5064.pdf?fsrch=1&sr=1&pageNum=1
AN5076	MC34VR500 Layout Guidelines	http://cache.nxp.com/docs/en/application-note/AN5076.pdf?fsrch=1&sr=2&pageNum=1
AN4878	LS1021A Design Checklist	https://www.nxp.com/webapp/Download?colCode=AN4878&location=null&fsrch=1&sr=1&pageNum=1&Parent_nodeId=&Parent_pageType=&Parent_nodeId=&Parent_pageType=&Parent_nodeId=&Parent_pageType=
NXP support pages		**URL**
MC34VR500 Product Summary page		http://www.nxp.com/products/automotive-products/energy-power-management/pmics/pmic-for-networking-processors/multi-output-dc-dc-regulator:MC34VR500
LS1021A Product Summary page		http://www.nxp.com/products/microcontrollers-and-processors/arm-processors/qoriq-layerscape-arm-processors/qoriq-layerscape-1021a-dual-core-communications-processor-with-lcd-controller:LS1021A
LS1021A-IOT Product Summary page		http://www.nxp.com/products/reference-designs/qoriq-ls1021a-iot-gateway-reference-design:LS1021A-IoT?lang_cd=en

7 Revision history

This table provides a revision history for this application note.

Table 13. Document revision history

Revision	Date	Description
0	07/2017	Initial public release

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Document Number AN5085
Revision 0, 07/2017