NXP Semiconductors
Application Note

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How to Use GDU Module in MC9S08SU16

1. Introduction

MC9S08SU16 is new NXP low-cost, high-performance and high integration UHV HCS08 8-bit microcontroller MCU. It uses the enhanced S08L central processor unit with one Gate Drive Unit (GDU) module integrated.
GDU module has 3-phase MOSFET pre-drivers unit which supports three high-side PMOSes and three low-side NMOSes, motor BEMF zero crossing detection circuit, two current sensing amplifiers with per-configured 20x gain and current/voltage limitation detection.
It is put into a 4mm x 4mm 24-pin QFN package, targeting drone electrical speed controller, low power motor control, small form cooling fan control and portable tools.

This application note describes the features of GDU and how to use different components in GDU module. It also provides a software example code of typical usecase in sensorless Brushless Direct Current Motor Control (BLDC) application. The software provided in this document is based on MC9S08SU16 headfiles based on latest CodeWarrior 10.7.

Contents

2. GDU features

2.1 GDU introduction

The Gate Drive Unit (GDU) module is primarily designed for power conversion and three phase motor control applications. It includes high side and low side Field Effect Transistor (FET) pre-drivers, motor BEMF zero crossing detection circuit, two current sensing amplifiers with per-configured 20x gain and current/voltage limitation detection. GDU is internally connected to crossbar, MCPWM and ADC modules so that the signal propagation delay can be effectively reduced or minimized.

Figure 1 is the overall GDU block diagram. From design perspective, the key components of GDU are internal clamp circuit, high/low side pre-drivers, 3 phase detectors and 2 current sensors, and also the over current/voltage protection circuits.

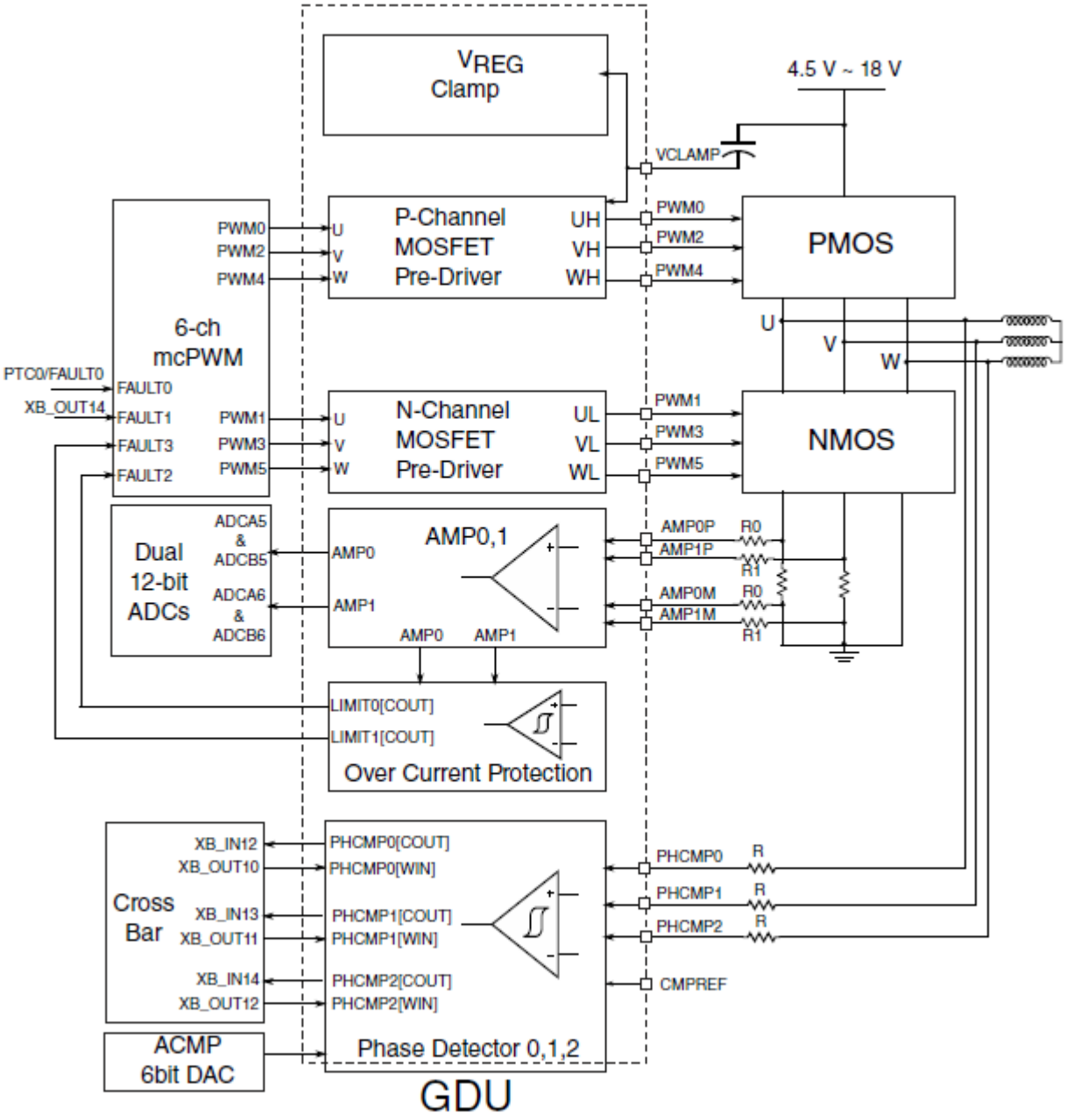

Figure 1. GDU Block Diagram

2.2 Clamp circuit

Since SU16 power supply could vary from 4.5V~18V in different application usage, which means the external power lines (DC Bus) varies in the same range. So GDU has implemented one clamp circuit inside to supply a stable, reliable and floating 5V power supply to high side gate driver to charging and discharging the gate capacitance of the P-channel mosfet. The “ground” is virtually floating. In contrast to conventional methods such as bootstrap, the floating regulator use less external components. It just need one external bypass capacitor (recommended value is 1uF) between VDD and VCLAMP pin.

Clamp circuit is enabled by GDU_CLMPCTRL[CLAMPEN] bit , the output voltage can be tuned by GDU_CLMPCTRL[TUNE] bits. After SU16 chip powers on and clamp circuit enabled, user could adjust the power supply connected to VDD pin from 4.5 V to 18 V, if the voltage of VCLAMP pin is about (VDD-5)V, then the Clamp circuit works correctly. *Figure 2* is the clamp circuit diagram.

NOTE

After Clamp is enabled, need about 100 us waiting time to enable high side pre-driver,100 us is safe time between Clamp enable and high side pre-driver enable.

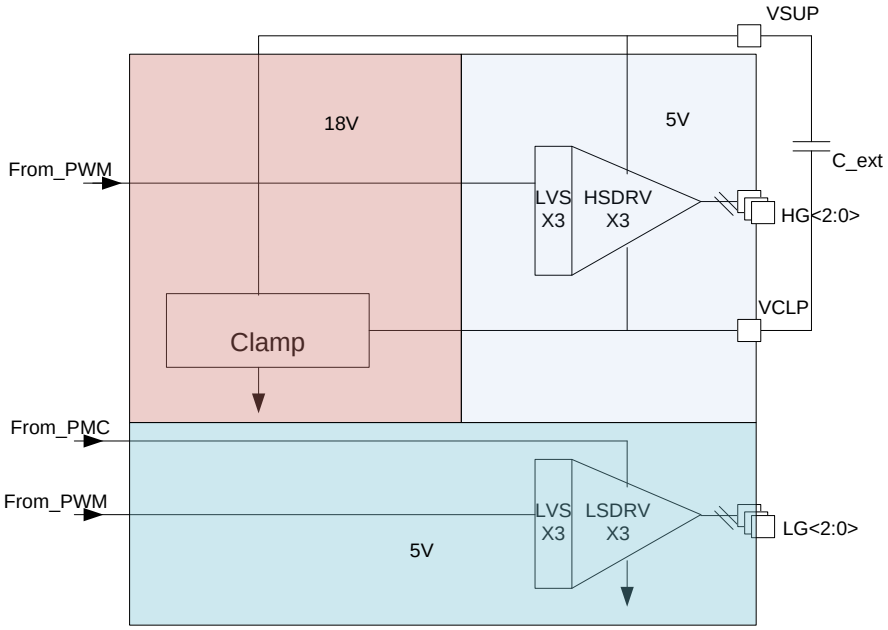

Figure 2. Clamp Circuit Diagram

2.3 Pre-driver and OVP

SU16 uses the complementary power switches: that are 3 sets of PMOSFETs as high side switch, three sets of NMOSFETs as low side switch. This architecture achieves minimum number of off-chip devices comparing with the NMOSFETs as high-side in bootstrap circuit. *Figure 3* is the pre-driver circuit diagram. The pre-driver high side and low side output buffer and driver strength are controlled by GDU_IOCTRL register. Users could choose different driver strength level according to external loading devices in different applications.

NOTE

High side has internal pullup resistors 226 KΩ which could not be disabled by user, but low side pulldown resistors 40 KΩ can be configured to enable or disable by software using GDU_IOCTRL[PDE] bit.

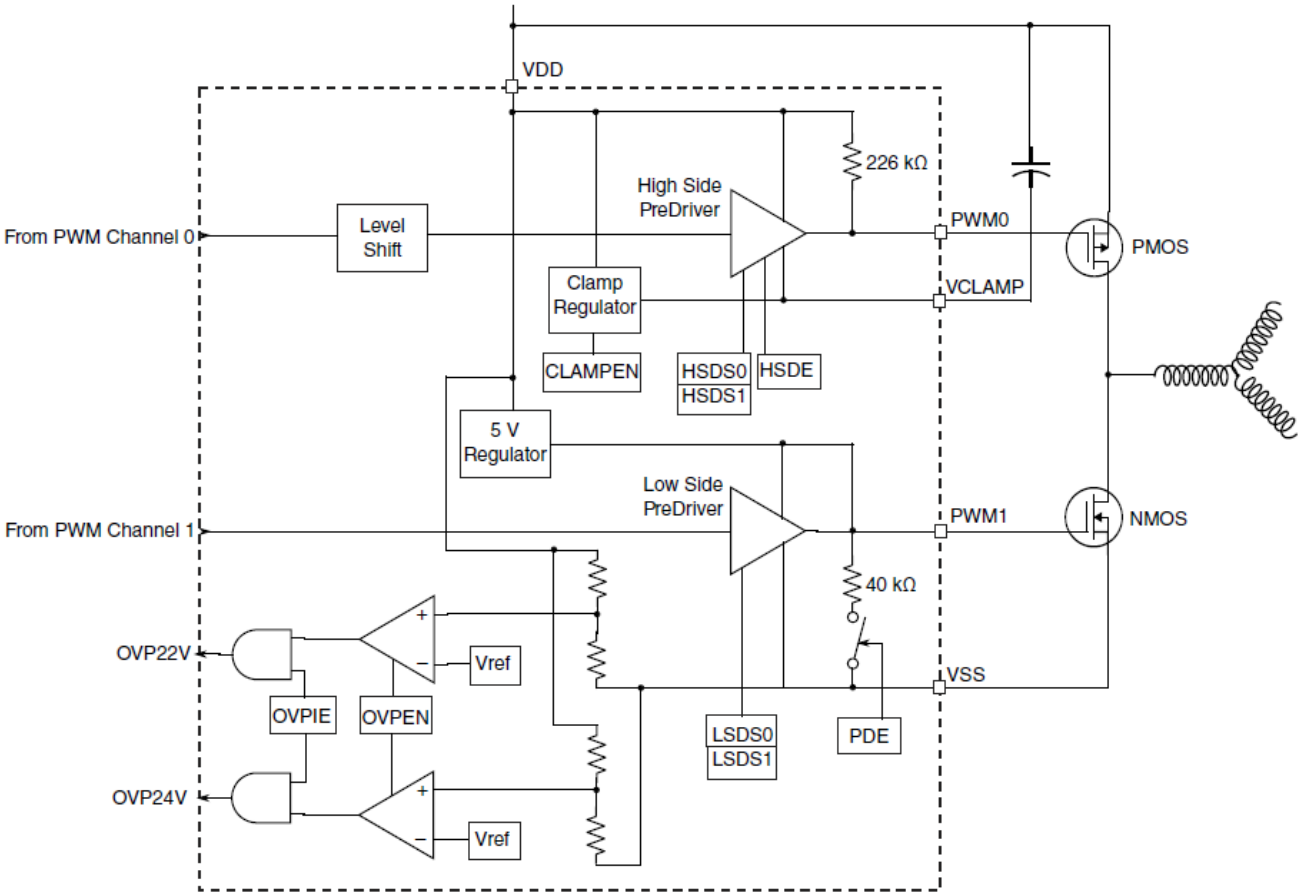

Figure 3. Pre-driver Circuit Diagram

From the above diagram, we can see there is also an OVP (over voltage protection) circuit inside pre-driver. Two comparators are used to generate 22V over-voltage and 24V over-voltage respectively. The status bits are OVP22V and OVP24V in GDU_STATREG register. If VDD(DC BUS) voltage is over 22 V, the over-voltage warning interrupt will occur(interrupt vector number is 4); If VDD voltage is over 24 V, the GDU module will put SU16 to safety mode, which means high side and low side PWM output will be in inactive status automatically. Meanwhile, VDD voltage divided by 8 is connected to ADC0 channel 7(not dominant in the diagram), user can use ADC0 to check the VDD power status in its interrupt routine.

NOTE

Suggest to turn off the pre-driver by software before SU16 enters stop mode to avoid the potential current injection on VDDX pin.

2.4 Current sensor and OCP

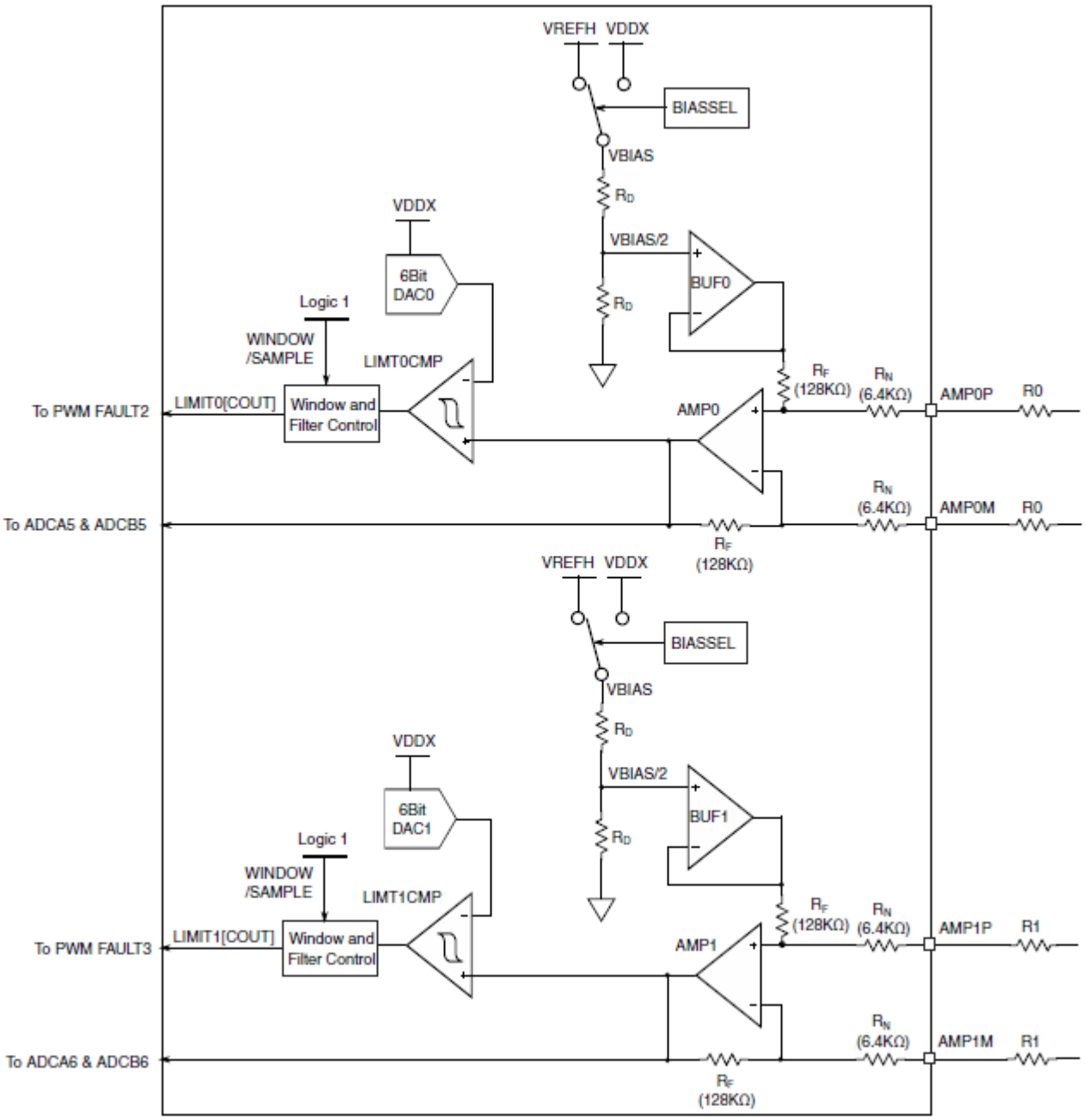

Figure 4. Current Sensor and OCP Circuit Diagram

As the *Figure 4* shows, there are two differential current sense amplifiers in GDU to sense the current flowing through the external resistor shunt as a voltage across the resistor. Typical usage is to be used to sense the two phase current or the DC bus current in BLDC motor control application. The amplifier gain is internally fixed to 20x, because gain = R_F/R_N =128 KΩ /6.4 KΩ = 20. But the gain can be reduced by adding external resistors (R1) on its plus and minus input, e.g R1=2 KΩ, gain = 15; R1= 4 KΩ, gain = 12. In order to measure both positive and negative currents, an internal bias reference must be used. This

reference is divided either VREFH or VDDX to a half (VBIAS/2) and added it to positive input of amplifier. This option control bit is GDU_SIGBIAS[BIASSEL]. The two current sensors could be enabled independently by GDU_CURCTRL[AMP0EN] and GDU_CURCTRL[AMP2EN]. And the sense data are internally routed to ADC0 channel 5 and 6.

The output of current sensor amplifier is not only connected to the ADC0 inputs, but also to the plus input of limitation comparator which is used as OCP (over current protection). The minus input of limitation comparator is driven by a GDU internal programmable 6-bit DAC. Users can configure over-current value by setting GDU_LIMITxDACCR(x=0,1) registers. The output of the comparator is connected to a digital filter circuit (configured by GDU_LIMITxFPR(x=0,1) register). At last, the output of digital filter circuit is connected to PWM fault input channel.

2.5 Phase detector

The *Figure 5* shows the block diagram of the phase detector in GDU.

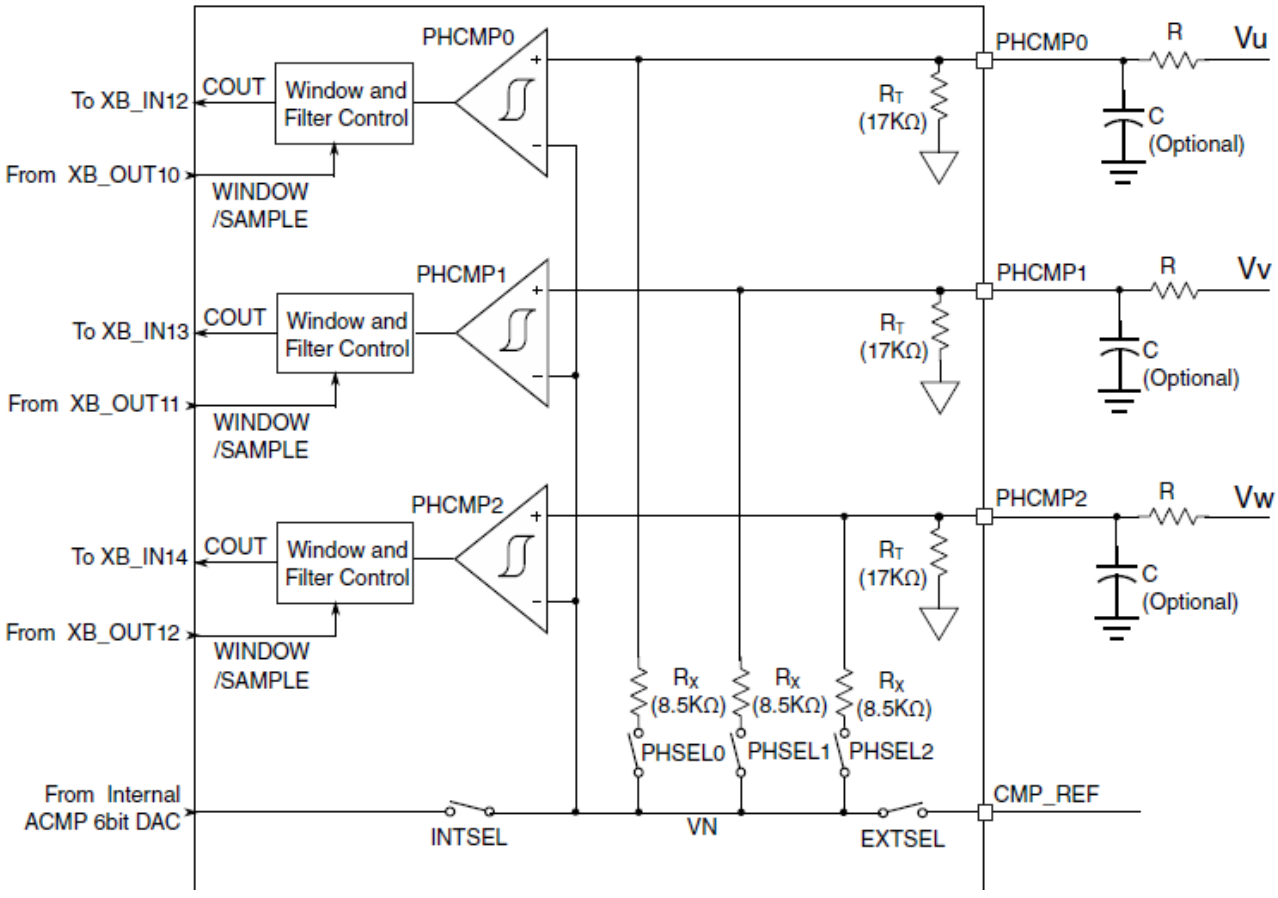

Figure 5. Phase Detector Circuit Diagram

Phase detector circuit is used to identify zero-crossing event at a back-EMF (electromotive force) signal generated at a winding of permanent magnet motor when the winding is not energized. The zero-crossing event at a back-EMF signal occurs when the signal level of the back-EMF signal equals to the voltage at the motor's common neutral connection. The comparators are provided with a virtual neutral

reference signal that is generated at the virtual resistor network circuit and tracks the signal at the motor winding's common neutral connection. The virtual neutral reference signal is generated by selectively communicating signals received from each motor winding to a virtual neutral circuit node. The virtual neutral has three different options in GDU,which is decided by GDU_PHASECTRL register. When GDU_PHASECTRL[VNEN] = 1, then virtual resistor network is enabled. It is the recommended setting. When GDU_PHASECTRL[INTSEL] = 1, virtual neutral is connected to the internal 6-bit DAC in the CMP module. When GDU_PHASECTRL[EXTSEL]= 1, virtual neutral is connected to the external VREFH pin(PTC0). The three bits of PHSEL2, PHSEL1, PHSEL0 in GDU_PHASECTRL are used to switch on/off different phases.

Phase detector comparator is used to compare the virtual neutral and phase voltage input. Its output is connected to a window/filter circuit which provides window comparing and digital filter function.The 3 array PHCMPx(x=0,1,2) registers are used to configure the window and filter mode according to user's application.

Since VDD(DC Bus) varies from 4.5 V~18 V,the phase detector are most likely to capture high voltage BEMF from three phase, in order to keep 3 comparators working under the correct operation power range, users must add external resistors on PCB for voltage divider as *Figure 6*. The typical value of internal R_T = 17 KΩ , so the recommended external resistors are 105 KΩ as 1:6 divider or 85 KΩ as 1:5 divider. Phase detector is designed to tolerant specified noise without external capacitor,so the capacitors on the *Figure 6* are just for option. They could be removed by users for cost reduction consideration.

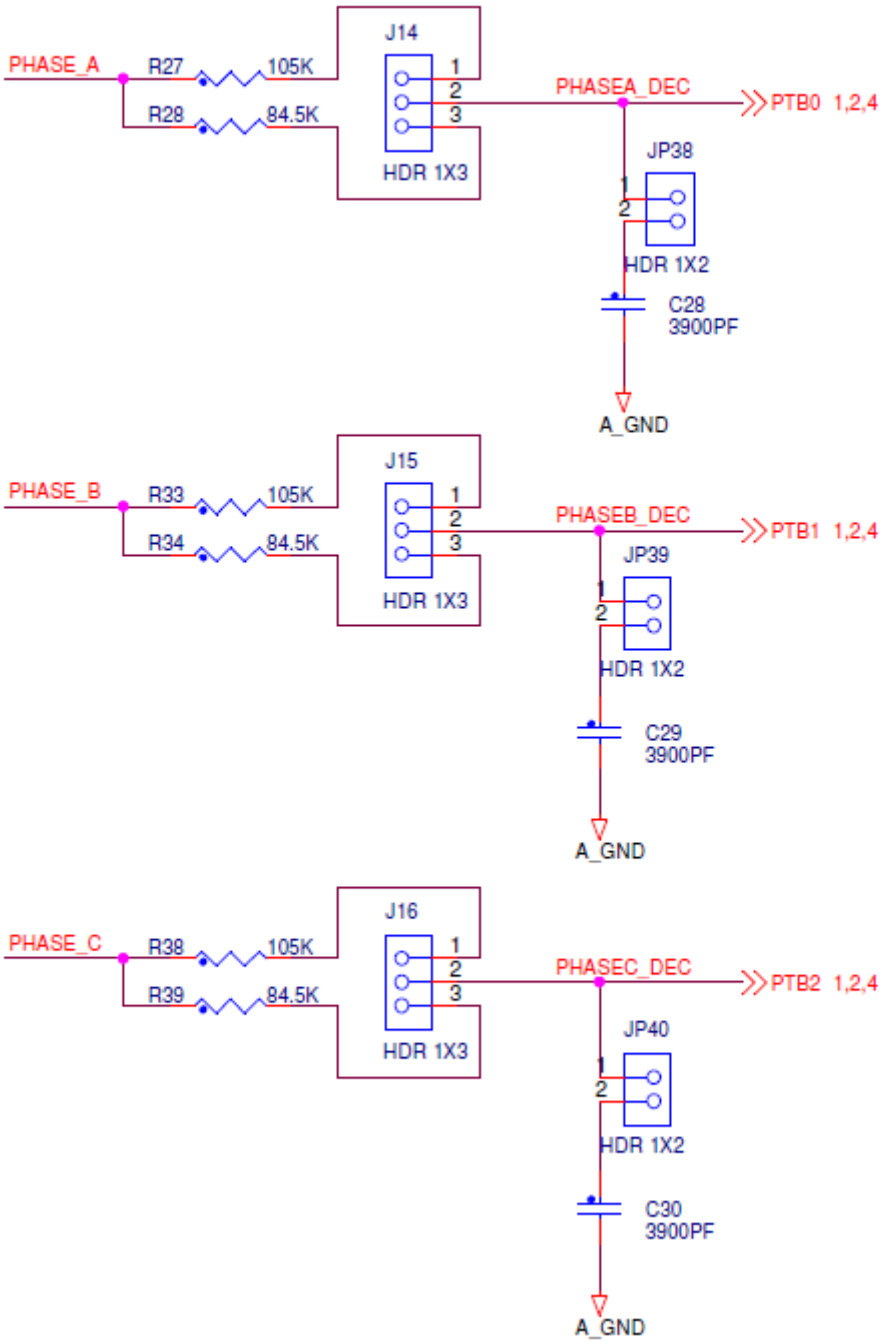

Figure 6. Phase Detector External Circuit on PCB

3 VDDX and VREFH

3.1 VDDX

VDDX is the 5 V voltage regulator output to supply power for the digital I/O domain and the analog modules domain (VDDA).

3.2 VREFH

VREFH is the accurate voltage reference output/input. It can be configured from 3.7 V to 4.9 V. An external decoupling capacitor is required on this pin (recommended value is 10uF).It is the reference voltage output for on-chip analog modules such as ADC, CMP and GDU current sensor bias reference voltage. This regulator can be enabled or disabled by configuring PMC_CTRL[VREFDN]. After POR or enabled, the flag PMC_STAT[VREFRDY] is set, once the regulator output is ready.The regulator output voltage can be trimmed from 3.7 V to 4.9 V through the PMC_VREFHCFG[T5V].
After reset, a factory trimmed value is automatically loaded to the PMC_VREFHCFG register so that VREGVREFH has a default output voltage, normally it is 4.2 V. After the write protection enable bit PMC_CTRL[GWREN] is set to 1, user can configure this voltage to other levels according to different application need.

NOTE

Since PMC_CTRL[VREFDN] = 1 after SU16 POR, internal VREFH output is disabled by default. User must connect external power source to VREFH pin (PTC0) as on-chip analog modules reference voltage or set PMC_CTRL[VREFDN] = 0 to enable and use internal VREFH regulator.

4 GDU software example

Following example code shows the GDU configuration of typical usecase in sensorless BLDC application.

```
static void GDU_Init(void)
{
	/*clamp enable, over voltage protection enable, over voltage interrupt enable*/
	GDU_CLMPCTRL = GDU_CLMPCTRL_CLAMPEN_MASK | GDU_CLMPCTRL_OVPIE_MASK |
GDU_CLMPCTRL_OVPEN_MASK;
	/*tune the parameters to manually adjust the clamp output voltage*/
	GDU_CLMPCTRL_TUNE = 4;
	/*delay about 100us after clamp enable then turn on the pre-drivers*/
	for (delayAfterClampEnable = 200; delayAfterClampEnable > 0; delayAfterClampEnable--);
	{
		asm(nop);
	}
```

```
      /*High side (HS) pre-driver Output Buffer enable,enable low side(LS) pulldown; HS and
LS select the Highest drive strength*/
      GDU_IOCTRL = GDU_IOCTRL_HSDE_MASK | GDU_IOCTRL_PDE_MASK | (3<<GDU_IOCTRL_LSDS_BITNUM)
| GDU_IOCTRL_HSDS_MASK;
      /*define different macros to select virtual neutral option*/
#ifdef GDU_PHASE_INTERNAL_VN_INTERNAL_VN
      /*virtual neutral using internal 3 resistors*/
      GDU_PHASECTRL = GDU_PHASECTRL_VNEN_MASK;
#endif

#ifdef GDU_PHASE_INTERNAL_VN_INTERNAL_DAC
     /*6-bit DAC reference are Vin1 to VREFH (default) and Vin2 to VDDX*/
     /*virtual neutral using internal ACMP DAC*/
     GDU_PHASECTRL = GDU_PHASECTRL_INTSEL_MASK;
     CMP_DACCR_VOSEL = 13;
     CMP_DACCR_DACEN = 1;
#endif

#ifdef GDU_PHASE_INTERNAL_VN_EXTERNAL_PAD
     /*virtual neutral using VREFH pin*/
     GDU_PHASECTRL = GDU_PHASECTRL_EXTSEL_MASK;
#endif

      /*OPAMP0 for DC bus current sensing enable, connect to GDU OPAMP0*/
      GDU_CURCTRL = GDU_CURCTRL_AMP0EN_MASK;
      /*OPAMP0 as sampled, filtered mode,filter sample counter:1, hysterisis: level 0*/
      GDU_LIMIT0CR0 = (1<<GDU_LIMIT0CR0_FLTCNT_BITNUM)&GDU_LIMIT0CR0_FLTCNT_MASK;
      /*OVP0 enable */
      GDU_LIMIT0CR1 = GDU_LIMIT0CR1_EN_MASK ;
      /*defined OVER_CURRENT_SCALE macro for DC bus over current value*/
      GDU_LIMIT0DACCR = OVER_CURRENT_SCALE;

#ifdef GDU_AMP_SIGBIAS_VDDX_REF
      /*defined macro to choose VDDX as current sensor bias voltage*/
      GDU_SIGBIAS |= GDU_SIGBIAS_BIASSEL_MASK;
#endif
```

```
       /*enable three phase detectors window, filter mode to identify the zero-crossing event
at a BEMF signal generated*/
       GDU_PHCMP0CR0 = (GCMP_FILT_CNT);
       GDU_PHCMP0CR1 = GDU_PHCMP0CR1_EN_MASK | GDU_PHCMP0CR1_PMODE_MASK |
GDU_PHCMP0CR1_WE_MASK;
       GDU_PHCMP0FPR = ZC_COMP_SAMP_PER_SYSU;


       GDU_PHCMP1CR0 = (GCMP_FILT_CNT);
       GDU_PHCMP1CR1 = GDU_PHCMP1CR1_EN_MASK | GDU_PHCMP1CR1_PMODE_MASK |
GDU_PHCMP1CR1_WE_MASK;
       GDU_PHCMP1FPR = ZC_COMP_SAMP_PER_SYSU;


       GDU_PHCMP2CR0 = (GCMP_FILT_CNT);
       GDU_PHCMP2CR1 = GDU_PHCMP2CR1_EN_MASK | GDU_PHCMP2CR1_PMODE_MASK |
GDU_PHCMP2CR1_WE_MASK;
       GDU_PHCMP2FPR = ZC_COMP_SAMP_PER_SYSU;


       /*enable three phase detectors*/
       GDU_PHASECTRL |= GDU_PHASECTRL_PHSEL0_MASK | GDU_PHASECTRL_PHSEL1_MASK |
GDU_PHASECTRL_PHSEL2_MASK;
}
```

5 Conclusion

This application note summarizes the features, user perspective and how to use GDU module in MC9S08SU16 device. With GDU integrated, users can save one pre-driver chip and achieve minimum number of off-chip devices comparing with traditional low power motor control and other similar application field. This document can help user to better understand GDU components and their functional implementation that make it easy for readers to use the features in their real applications.

6 Revision history

Revision number	Date	Substantive changes
0	12/2016	Initial release

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