The increased use of smartphones and other mobile devices utilizing Internet applications, social networks, video calls and email is driving an unprecedented increase in worldwide wireless network traffic, and the performance race to 4G is at its peak.

From the network operators' perspective, the key factors in building wireless networks are the ability to meet demand for high-bandwidth base stations, end user capacities and quality of service (QoS), along with significantly reducing network deployments and operating costs. The world has moved to 3G and the performance race toward 4G supporting LTE and LTE-Advanced standards at the highest bandwidth with the maximum number of users is now underway.

What matters to wireless network operators and subscribers is the performance of a wireless network. The ability of the base station to efficiently handle massive data processing at low latencies is key to meeting data throughputs and QoS. Without a high degree of integration, system knowledge and sophistication in the underlying silicon design, 4G base stations will not meet the LTE and LTE-Advanced demand for throughputs at a reasonable cost.

Our relationships with world-leading wireless OEMs who help drive requirements and an array of Freescale-pioneered core technology innovations in baseband processing create solutions that are both flexible and software upgradeable. Freescale delivers best-in-class platform solutions to meet the demand for existing and next-generation wireless network deployments.

The QorIQ Qonverge B4860 solution is our newest multistandard wireless base station system on chip (SoC) based on 28 nm process technology. Capable of handling all the baseband processing layers for 1200 LTE users and up to 1.8 Gb/s of aggregated data throughput over the air, the B4860 delivers the industry's most advanced solution while reducing overall power consumption for high-end, three sector 20 MHz LTE macro base stations.

QorIQ Qonverge B4860 Benefits

- Highest performing heterogeneous multicore base station SoC in the market today for LTE, LTE-Advanced and WCDA, with unmatched throughput and lowest latency.

- Embedded with our new e6500 dual-threaded 64-bit Power Architecture® cores and the new SC3900FP, 32 MAC/s fix-point and 16 FLOP/s floating-point StarCore flexible vector processor (FVP) cores.

- Baseband processing acceleration powered with the industry-leading multi-accelerator platform engine (MAPLE) supports all standards, including WCDMA chip rate.
- Data Path Acceleration Architecture (DPAA) for backhaul processing, incorporating acceleration for packet parsing, classification and distribution, queue management for scheduling, packet sequencing and congestion management, hardware buffer management for buffer allocation and de-allocation and engines for both backhaul and over-the-air encryption.
- All processing elements are connected through our fully cache-coherent CoreNet fabric, which enables the construction of scalable software architectures, eases multicore programming and reduces development time.
- Standard-compliant, high-speed interfaces enable glueless connections to remote radio antennas and backplane or backhaul options.
- Multisector/multicarrier capabilities, high capacities and high-speed interfaces enable cloud RAN deployment to remote radio heads using 9.8 Gb/s CPRI interfaces and 10 Gb/s Ethernet interfaces required for load balancing in baseband pooling topologies.
- Leverages the high performance and low power of the latest 28 nm process technology.
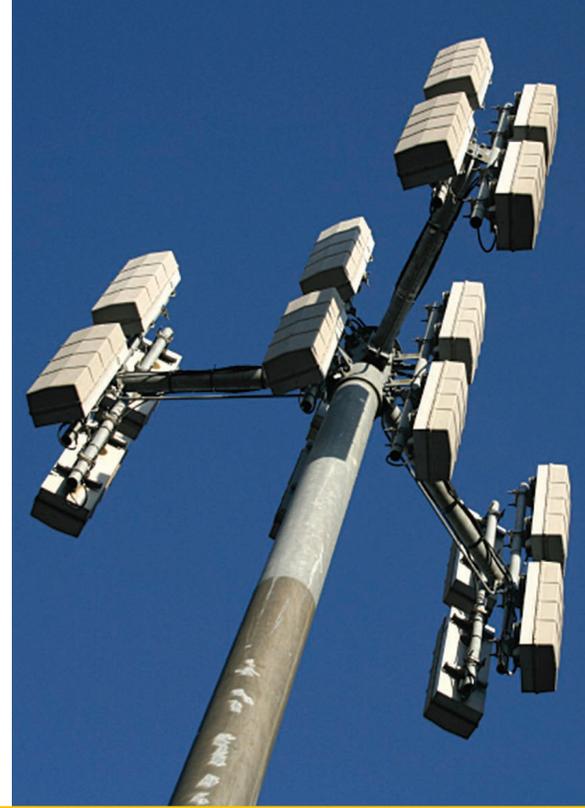
Overview

The QorIQ Qonverge B4860 SoC reduces power consumption for high-end wireless macro base stations to deliver the industry's highest performance solution. The multicore SoC includes 10 programmable cores based on a StarCore FVP and 64-bit Power Architecture cores, as well as CoreNet and MAPLE technologies. The B4860 targets broadband wireless infrastructure and builds upon the proven success of existing Freescale multicore SoCs and DSPs in wireless infrastructure markets.

The B4860 is designed to provide simultaneous support for multiple standards, as well as adapt to the rapidly changing and expanding standards of LTE (FDD and TDD), LTE-Advanced and HSPA+.

Layer 1 is implemented using a mix of StarCore SC3900FP high-performance FVP cores and the MAPLE baseband accelerator platform, which provides a highly efficient hardware implementation of standardized algorithms for each of the air interface standards in single- and multimode operations. Layer 2 and transport processing are implemented using a mix of e6500 64-bit dual-threaded Power Architecture cores, data path and security accelerators.

The B4860 is perfectly suited to meet the performance demands of wireless operators for LTE, WCDMA and LTE-Advanced macro base stations. It includes a combination of fully programmable StarCore FVP cores, Power Architecture cores and powerful baseband acceleration to provide cost-effective, best-in-class performance, power efficiency and connectivity. With four dual-threaded e6500 64-bit cores operating at up to 1.8 GHz and six SC3900FP FVP cores at up to 1.2 GHz, the B4860 provides the required programmable performance. Additionally, the MAPLE hardware accelerators target processing of baseband functions, such as FEC decoding and encoding, FFT, PDSCH and PUSCH embedded data flows, WCDMA chip rate and MiMO equalization, allowing base station manufacturers to deliver higher throughputs, lower latencies and better spectral efficiency.

While the four Power Architecture cores offer industry-leading processing capacity and a major leap in available processor performance for layers 2 and 3 in many throughput-intensive, packet-processing networking applications, raw CPU processing power is not enough to achieve multi-Gb/s data rates. To address this, the B4860 uses Freescale DPAA to significantly reduce data plane instructions per packet and enable more CPU cycles to work on value-added services rather than repetitive low-level tasks. Combined with specialized accelerators for cryptography and pattern matching, the B4860 allows the user's software to perform complex packet processing at high data rates.

The B4860 offloads performance and latency-critical layer 1 functions to MAPLE-B3, which integrates highly optimized, flexible accelerators. The smart partitioning introduced in the B4860 provides an excellent balance between OEM intellectual property, hardwired accelerators and algorithms implemented on the fully programmable StarCore FVP and allows for highly efficient power dissipation and silicon area utilization.

e6500 Power Architecture Core Features Summary

The B4860 integrates four high-performance 64-bit, Power Architecture ISA v2.06-compliant dual-threaded e6500 cores. Each is a superscalar dual-threaded, quad-issue (dual-issue per thread) processor, supporting out-of-order execution and in-order completion.

The dual-threaded e6500 subsystem includes the following features:

- Simultaneous multi threading
- 40-bit physical addressing
- Memory management unit (MMU) with 1024-entry 8-way set-associative TLB supporting 4 KB pages and 64-entry fully associative. TLB supporting variable size pages and indirect page table entries
- Hardware support for memory coherency
- Five integer units: Four simple (two per thread), one complex (integer multiply and divide)
- Two load-store units: One per thread
- AltiVec technology
  - 128-bit vector SIMD engine
- User, supervisor and hypervisor instruction-level privileges
- 32 KB program L1 cache and 32 KB data L1 cache (per core), each with data and tag parity protection
- Shared 2 MB L2 unified cache for program and data (per four cores cluster) with ECC

SC3900FP FVP Core Features Summary

The B4860 integrates six StarCore SC3900FP FVP high-performance cores. Each SC3900FP FVP core includes:

- 32-bit instruction set, expandable to 48-bit and 64-bit instructions, enabling highly orthogonal compiler-friendly code
- Data arithmetic and logic unit includes four data multiplication units, each of which can compute eight 16 x 16 multiplications, two complex multiplications, four FLOP or two 32 x 32-bit multiplications per cycle
- Very high numerical throughput for DSP operations (up to 32 multiplications 16 x 16-bit per cycle and up to 16 floating-point operations per cycle)
- Variable length execution set execution model ranging from 16-bit up to 256-bit
- Up to eight instructions executed in a single statistically scheduled clock cycle: SIMD8 (vector 8) single instruction multiple data instructions
- High throughput memory interface with up to 256-bit program access and 1024-bit data accesses per cycle
- Branch target buffer for accelerating execution of change-of-flow instructions with powerful multi-predicate model
- Multi-instruction, multidata vector operations
- MMU and OS support with address translation and memory protection
- 32 KB program L1 cache and 32 KB data L1 cache (per core), each with data parity protection
- Shared 2 MB L2 unified cache for program and data (two cores per cluster) with ECC and high bandwidth accelerator ports
- Hardware support for memory coherency between L1, L2 caches and with main memory through the CoreNet fabric

CoreNet Fabric

CoreNet fabric is our front-side interconnect standard for multicore products used by both StarCore and Power Architecture families.

CoreNet is a highly concurrent, fully cache-coherent, multi-ported fabric delivering point-to-point connectivity with flexible protocol architecture allowing pipelined interconnection between processors, platform caches, memory controllers, external interfaces and accelerators.

CoreNet is designed to improve high-speed DDR memory utilization by allowing out of order transactions, reordering, snooping and stashing to improve data bandwidth.

The B4860 multiple and parallel address paths allow for high bandwidth, which is a key performance indicator for large coherent multicore processors.

With internal fabrics delivering total bandwidth of 4.7 Tb/s, the interconnect technology virtually guarantees that cores and coprocessors are never starved for data to deliver the required processing performance.

Inter-Processor Communications

The e6500 CPU cores and SC3900 FVP cores communicate in multiple ways and use the same mechanisms on both cores. This eases the task of the software developers and increases flexibility in designing the inter-processor communication (IPC) layer.

Primary tools for IPC implementation:

- Queue manager can be used to transfer messages/tasks between cores
- Inter-core communication flows through the system interrupt controller
- The B4860 instantiates a virtual interrupt controller. It is connected to the SC3900FP FVP and e6500 cores to activate the interrupts
- The e6500 CPU cores and SC3900FP FVP cores share the same software semaphore mechanism and can use it for semaphoring
- The e6500 CPU cores and SC3900FP FVP cores can send doorbells to each other via the CoreNet fabric
- Multiple hardware semaphores are instantiated and may be used by internal and external masters

MAPLE-B3 Baseband Acceleration Platform

The B4860 SoC offloads layer 1 performance and latency-critical functions to MAPLE-B3, for highly optimized, flexible accelerator integration. The flexibility and efficiency of the MAPLE-B3 programming model enables low overhead accelerator control.

Embedded data flow (EDF) inside MAPLE-B3, controlled by a programmable system interface for processing management, accelerator scheduling and customization using integrated RISC processors, further improves system latencies, data traffic in the SoC and memory consumption. EDF enables very low processing latency due to high throughput accelerators and allows direct IQ antenna data streaming between the CPRI antenna interface.

MAPLE-B3 hardware acceleration in the B4860 supports LTE, LTE-Advanced, WCDMA, TD-SCDMA and WiMAX standards, handling forward error correction schemes including Turbo and Viterbi decoding, Turbo encoding and rate matching, MIMO MMSE equalization schemes, matrix operations, CRC insertion and check, FFT/iFFT and DFT/iDFT calculations, PUSCH and PDSCH acceleration, and UMTS path search and chip rate acceleration

Control and DPAA

The four e6500 Power Architecture cores and accelerators are allocated for L2 stack processing (MAC/RLC, PDCP, scheduler, transport and control) for a multisector LTE or LTE-Advanced base station, with an option to further accelerate MACScheduler processing utilizing the integrated AltiVec SIMD engine. The DPAA includes the following accelerators to offload backhaul/backplane packet handling and enable multicore load distribution:

- Frame manager (FMan), supporting in-line packet parsing and general classification to enable policing and QoS-based packet distribution
- Queue manager (QMan) and buffer manager (BMan), allowing offload of queue management, task management, load distribution, flow ordering, buffer management and allocation tasks from the cores
- RapidIO manager (RMAN) supports SRIO types 8, 9, 10 and 11 (inbound and outbound) and types 5 and 6 (outbound)
- Security engine (SEC 5.3), crypto-acceleration for protocols such as IPsec, SSL/TLS, 802.16, SRTP, 3GPP RLC encryption/decryption, LTE PDCP encryption/decryption and SNOW-3G, Kasumi, AES, DES and ZUC algorithms

Shared L3 Caches

The B4860 contains two 512 KB, 16-way shared L3 CoreNet platform caches (CPC) located between the CoreNet fabric and each DDR controller. The CPCs reduce average access latency to DDR and increase system performance by optimizing DDR accesses. The CPCs can be partitioned to behave as SRAM for critical code/data sections. Features include:

- 16-way cache array configurable to several modes on a per-way basis
- Unified program and data cache
- Addressable as shared SRAM
- I/O stashing
- ECC support

The e6500 CPU cores and SC3900FP FVP cores communicate in multiple ways and use the same mechanisms in both cores.

DPAA accelerators provide full transport offload including IP fragmentation/ reassembly, IPSec, classification and packet distribution up to layer 4, QoS including multilevel traffic shaping and autonomous packet forwarding.

Trust Architecture Support

Trust architecture allows developers to create systems that perform only their intended functions. The B4860 allows OEMs and operators to ensure that their software, and not an attacker's software, is executed at boot time. For this reason, the trust architecture is often referred to as "secure boot."

The system developer digitally signs the code to be executed by the CPU coming out of reset and the B4860 ensures that only an unaltered version of that code runs on the platform. The B4860 offers both boot time and runtime code authenticity checking and configurable consequences when the authenticity check fails.

Device Peripherals

The B4860 includes a high-performance peripheral set to develop a variety of base station and board topologies, including:

- Two DDR controllers at up to 1.866 GHz supporting DDR3 and DDR3L devices for both 64-bit and 32-bit data interfaces, enabling up to 8 GB of addressable memory space, including ECC support
- Eight CPRI v4.2-compliant SERDES-based antenna interfaces capable of up to 9.8 GBaud per link enabling direct antenna streaming into MAPLE-B3 and delay compensation support
- Two 4-lane serial RapidIO® controllers, compliant with RapidIO 2.1 spec for up to 5 GBaud operation per lane
- PCI Express® controller, compliant with base specification revision 2.0 with 4-lane 5 GBaud support
- Six Ethernet controllers, two operating at 10, 2.5 and 1 Gb/s through XFI/XAUI/SGMII and four operate at 2.5 and 1 Gb/s through SGMII interface, including IEEE1588v2 time sync support
- Eight Aurora debug/trace interfaces
- 16 SERDES lanes at 10 GB
- 16-bit external memory interface for connecting to flash memory (NAND and NOR) and generic memory interface
- USB 2.0
- Four I²C, SPI, four UART and eSD/eMMC controllers
- 182 32-bit timers
- 44 GPIOs

Critical Performance Parameters

The B4860 features four 64-bit Power Architecture ISA v2.06-compliant dual-thread e6500 cores. Each is a superscalar dual-thread, quad-issue (dual-issue per thread) processor, supporting out-of-order execution and in-order completion at up to 1.8 GHz and six StarCore SC3900FP FVP cores at up to 1.2 GHz. The FVP core architecture allows very high throughput of convolution-based kernels, complex arithmetic, mixed/double-precision multiplication with high memory bandwidth and MAPLE-B3 baseband acceleration platform.

- Six StarCore SC3900FP FVP cores split into three clusters of two cores each, delivering total performance of up to 230.4 GMACs of 16 x 16-bit multiply-accumulates and up to 115.2 floating-point operations per second
- Four Power Architecture e6500 64-bit cores delivering performance of 43,200 DMIPS (Dhrystone MIPS) embedded with the AltiVec SIMD engine

The MAPLE-B3 baseband acceleration platform provides the following features:

- Turbo decoding including rate de-matching and HARQ combining
- Turbo encoding with information bit encoding including rate matching
- Viterbi decoding
- FFT/iFFT and DFT/iDFT processing
- CRC check and insertion supporting
- MIMO equalization (MMSE), high-precision floating point-based algorithm acceleration supporting up to 8 x 4
- Matrix inversion and multiplication acceleration
- UMTS path searcher
- UMTS chip rate support

The accelerators in MAPLE-B3 can operate on different standards simultaneously, supporting LTE, LTE-Advanced and WCDMA users at the same time.

For backhaul and antenna connection, the B4860 high-speed interfaces deliver the following aggregated throughputs:

- CPRI antenna interface, up to 78.6 GBaud/s
- Serial RapidIO, up to 40 GBaud/s
- Ethernet, up to 20 Gb/s
- PCI Express, up to 20 GBaud/s

QorIQ Qonverge B4860 Block Diagram

| Core Complex (CPU, L2 Cache) | Basic Peripherals and Interconnect |
| Accelerators and Memory Control | Networking Elements |
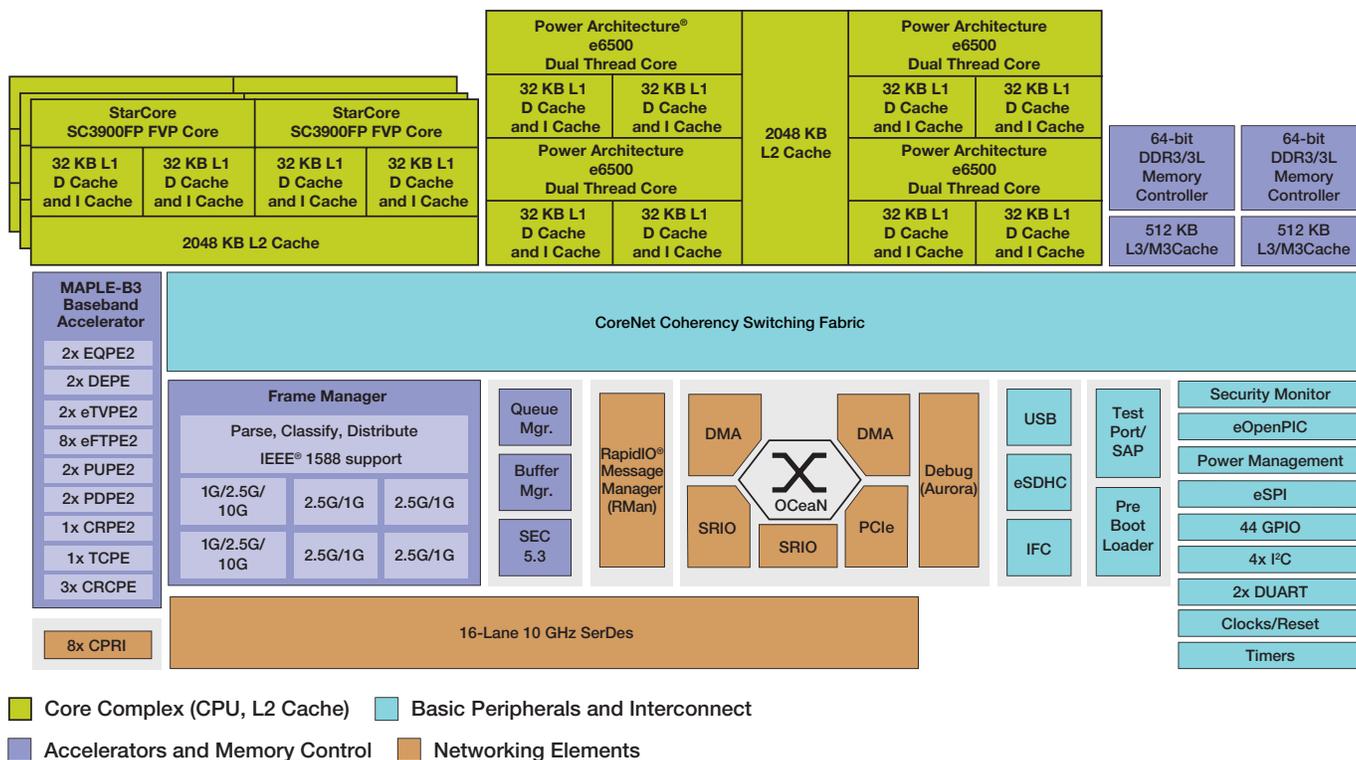
Designed to meet the demand for base station applications, the B4860 is ideal for macro base stations in the heterogeneous wireless network, supporting multiple standards such as GSM, WCDMA, TD-SCDMA, LTE and LTE-Advanced, and enabling connection to remote radio heads via fiber optic cables using the CPRI protocol capable of handling delay compensation for tens of kilometers.

Advanced Power Management

Advanced power management capabilities of the B4860 include:

- Fine grained static clock gating to individual SoC units
- Drowsy core with state retention, and nap and state retention power saving mode that allows the core to quickly wake up and respond to service requests in e6500
- Dynamic power gating of the e6500 cores
- Dynamic power gating of MAPLE processing elements
- Dynamic self refresh for unused DDR

Complete Development Tools Suite

The CodeWarrior Development Studio for B4860 helps developers overcome the challenges of creating applications for complex heterogeneous multicore SoCs by providing a wide array of tools. The IDE is based on the Eclipse platform, allowing developers to leverage the support of the Eclipse community. Within the Eclipse framework, the build, debug, simulation and analysis tools are combined, unleashing the full potential of Freescale high-performance DSPs and CPUs.

Highlights

- Feature-rich, Eclipse-based IDE
- High-performance C/C++ compilers for CPU and DSP
- Multicore debugger with multicore run control commands
  - Multicore run, start and stop commands
  - Multicore reset
  - Symmetric multiprocessor (SMP) and asymmetric multiprocessor (AMP) debugging
  - Support for debugging applications using Freescale hypervisor or LWE

- Multicore AMP/Linux® SMP debugger with multicore run-control commands
- Extensive software analysis tools including profiling and trace tools
- Royalty-free DSP SmartDSP OS with extensive driver support
- Advanced device simulation, device instruction set simulator and performance accurate simulator
- Highly advanced software analysis tools, including Nexus program and DPAA trace tools, and extended, integrated support for popular open source tools such as LTTng, OProfile and Valgrind
- Support for Linux application and kernel development
- Freescale offers the B4860QDS development boards to help customers quickly develop software with the B4860 SoC

In addition to Freescale tools and operating system, the B4860 is supported by the development tools and operating systems of our partners.

Ownership of the key intellectual properties and deep engagements with leading OEMs in the wireless access market puts Freescale in a unique position to define architectures and drive integration for performance, power and cost benefits.

Market Traction and IP Ownership

The key processing elements in any device for mobile wireless infrastructure are the programmable cores, the baseband hardware accelerators, internal interconnects and high-speed interfaces. Freescale has long been an embedded processing leader and market-proven Power Architecture technology has been used by leading wireless OEMs worldwide for many years. Significantly enhanced from generation to generation, it comes with a rich ecosystem to provide customers with seamless migration from current to higher performance products.

For more than a decade, StarCore DSP cores have been used worldwide in base station applications requiring the highest levels of performance and programmability. Now on its ninth generation, StarCore cores are used in DSP and SoC devices by many of the top wireless manufacturers in LTE, WCDMA and WiMAX deployments. Devices built with StarCore technology have earned leading results from top benchmarking firms. Recently, the SC3900FP core earned the industry's highest benchmark score, nearly twice that of its closest competitor.

Our ownership of key intellectual properties coupled with deep engagement with leading OEMs in the wireless access market puts Freescale in a unique position to define architectures and drive integration for performance, power and cost benefits. Being relatively independent from external IP providers' next-generation technologies and timelines enables us to create a portfolio of devices that help OEMs meet targets for performance and rapid market introduction for evolving wireless technologies.

For more information, visit freescale.com/QorIQQonverge