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Revisions

Rev	Description	Date
A	Original Design	4-15-09
B	Correction to Q3 pin 3, SCL_High to SDA_High. Reconnect Q4 pin 2 and Pin3. Also, replaced 6 and 30 pin Header Connector with having shorter pin high.	6-8-09
C	Replaced connector J4	7-30-09

freescale semiconductor

RASG - Proximity
2100 E. Elliot Rd
Tempe, AZ 85284

ICAP Classification: FCP: ____ FIUO: _ PUBI: ____

Designer: B. Osoinach/C.Teegarden	Drawing Title: **KITMPR121EVM**		
Drawn by: S. Mejia	Page Title: **Title Page**		
Approved: B. Osoinach	Size B	Document Number SCH-25890 PDF: SPF-25890	Rev C
	Date: Thursday, July 30, 2009	Sheet 1 of 5	

wise Specified:
are in ohms, most are 1%, 1/10 Watt. Otherwise are 5%, 1/8 Watt.
All capacitors are in uF, some are 10% or 20%
All voltages are DC
All polarized capacitors are tantalum

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
_B Denotes - Active-Low Signal
<> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

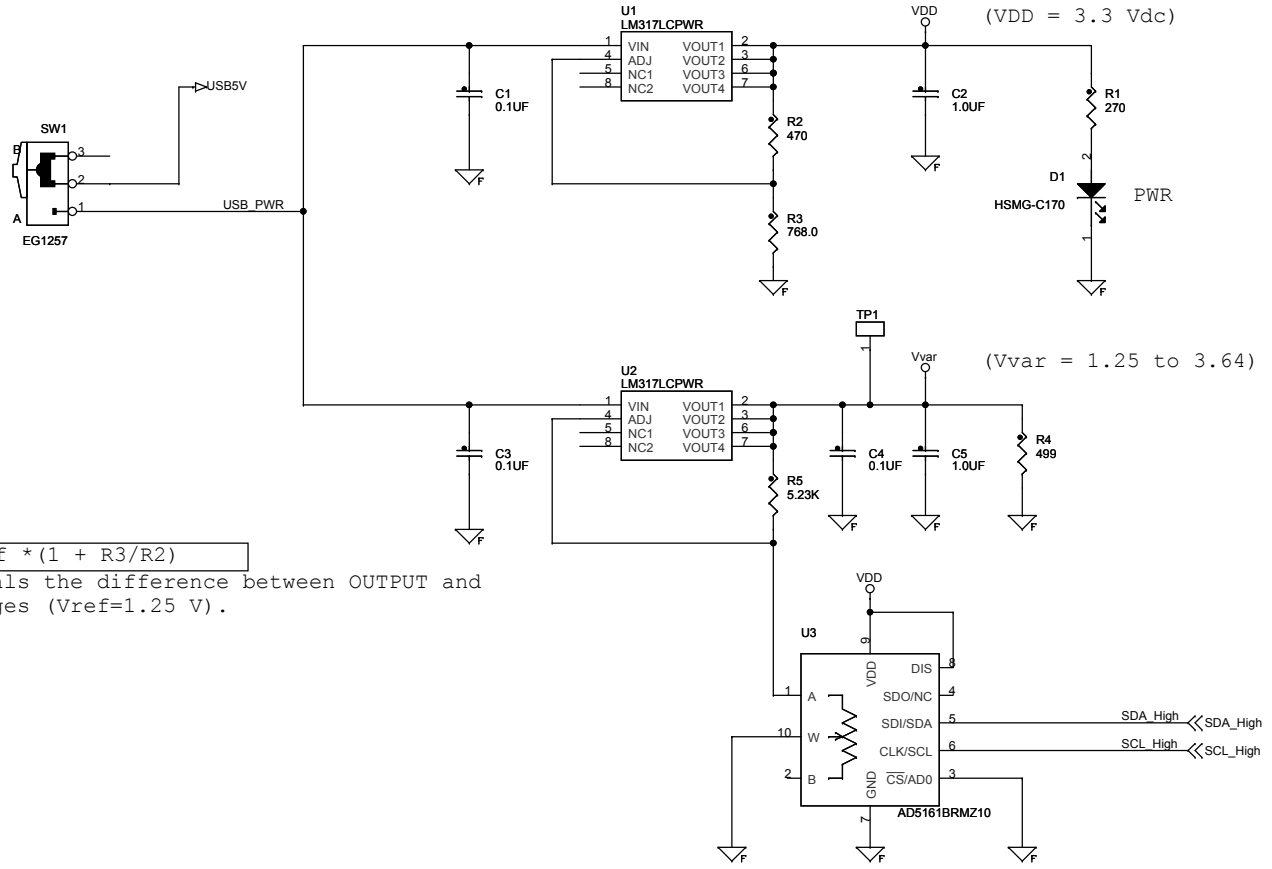
freescale semiconductor

Drawing Title: KITMPR121EVM

Page Title: NOTES

Size	Document Number	Rev
B	SCH-25890 PDF: SPF-25890	C

Date: Thursday, July 30, 2009 | Sheet 2 of 5



EXAMPLE EQUATION:

VDD = Vref *(1 + R3/R2)

Where: Vref equals the difference between OUTPUT and ADJUSTMENT voltages (Vref=1.25 V).

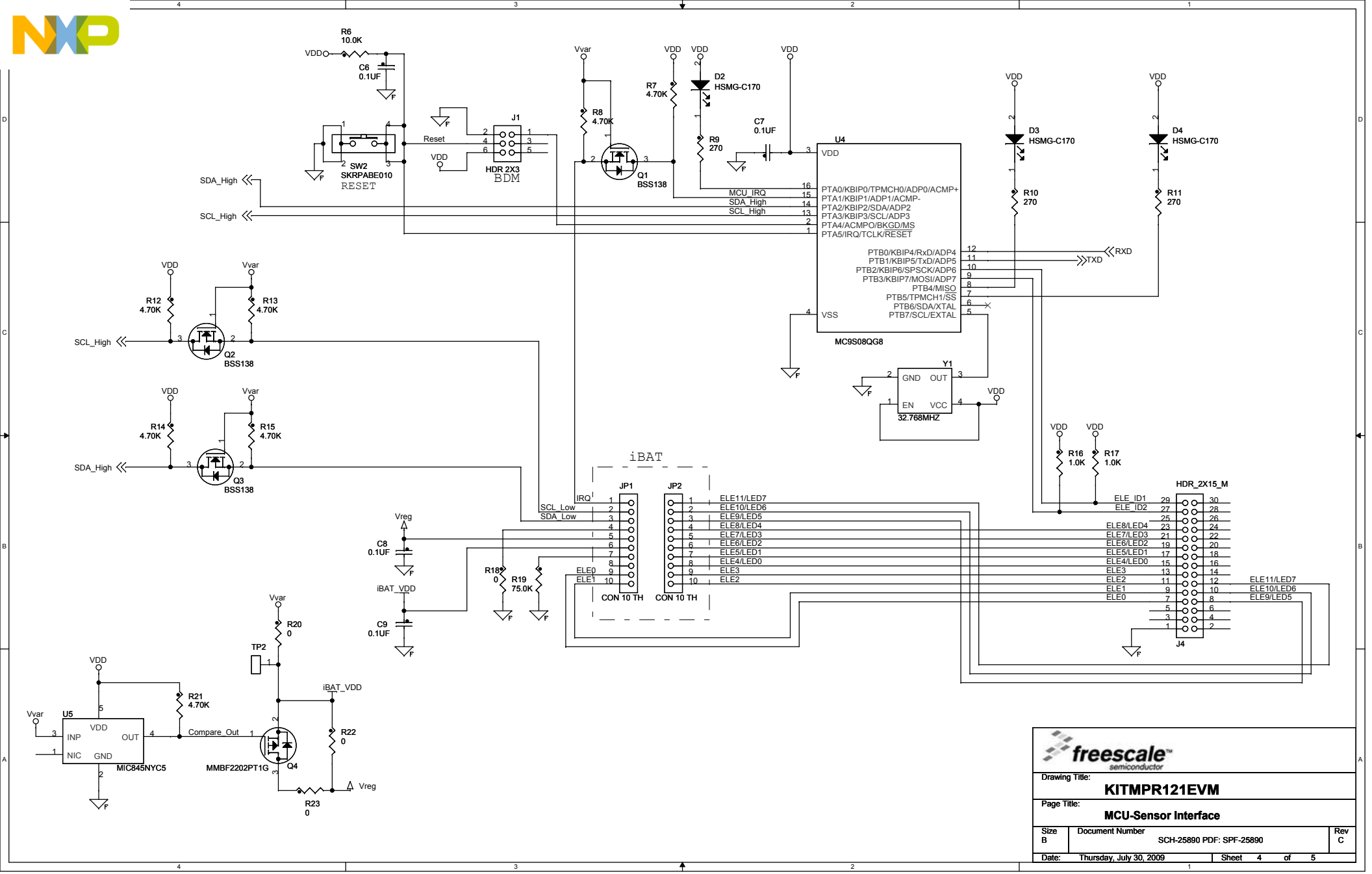
freescale semiconductor

Drawing Title: **KITMPR121EVM**

Page Title: **Voltage Settings**

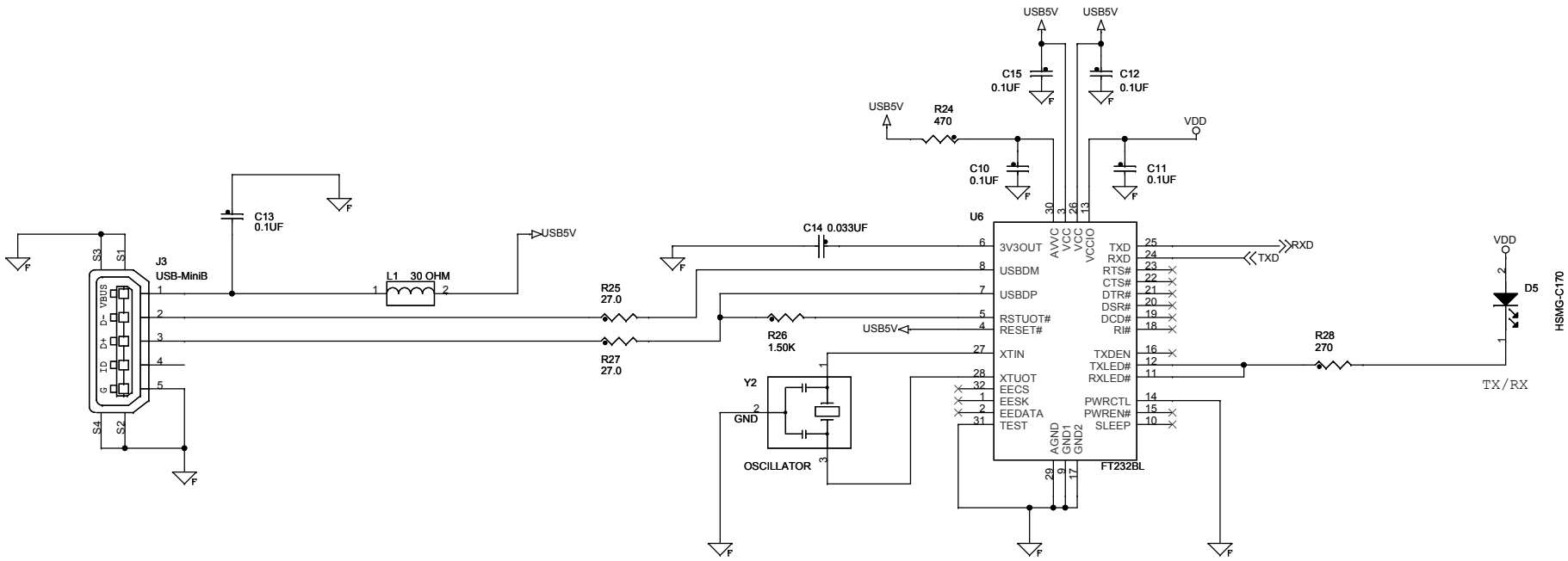
Size	Document Number	Rev
B	SCH-25890 PDF: SPF-25890	C

Date: Thursday, July 30, 2009 Sheet 3 of 5



freescale semiconductor

Drawing Title:	KITMPR121EVM
Page Title:	MCU-Sensor Interface
Size: B	Document Number: SCH-25890 PDF: SPF-25890
Rev: C	
Date: Thursday, July 30, 2009	Sheet 4 of 5



freescale semiconductor

Drawing Title:
KITMPR121EVM

Page Title:
USB Interface Circuitry

Size	Document Number	Rev
B	SCH-25890 PDF: SPF-25890	C

Date: Thursday, July 30, 2009 Sheet 5 of 5

NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 (LATEST REVISION).

2. THIS PWB MUST BE COMPLIANT WITH THE FREESCALE ECO REQUIREMENTS (DOCUMENT # 12MWS00047B) THESE REQUIREMENTS PROHIBIT THE USE OF CONTROLLED SUBSTANCES INCLUDING THOSE FOUND IN RoHS STANDARDS. DISCLOSURE OF RESTRICTED AND REPORTABLE SUBSTANCES IS ALSO REQUIRED.

3. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.

4. BASE MATERIAL - FR4 (OR EQUIVALENT RoHS COMPLIANT) LAMINATE AND PREPREG SHALL MEET IPC-4101A-94
   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.

5. COPPER FOIL WEIGHT - OUTSIDE LAYERS AND INNER LAYERS 1.0 OZ. SEE STACKUP DETAIL 'A'

6. PLATING FINISH - BOTH SIDES ENIG (EMMERSIONLESS NICKEL IMMERSION GOLD):
   76.2-203.2 MILLIMICRON (3-8 MICROINCH) OF GOLD OVER
   2,540-5,080 MILLIMICRON (100-200 MICROINCH) MINIMUM NICKEL.

7. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.

8. SOLDERMASK - GREEN COLOR (TAIYO OR EQUIVALENT), BOTH SIDES.

9. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.

10. ELECTRICAL TEST - 100% IPCD356.

11. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

12. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY FREESCALE.

13. OVERALL PCB THICKNESS 62 MILS. TOP AND BOTTOM FR4 LAYERS 10 MILS. INNER FR4-LAYER IS 40 MILS.

14. SOLDER SAMPLES TO BE PROVIDED.

15. BASIC GRID INCREMENT AT 1:1 IS .0001.

16. MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM FREESCALE.

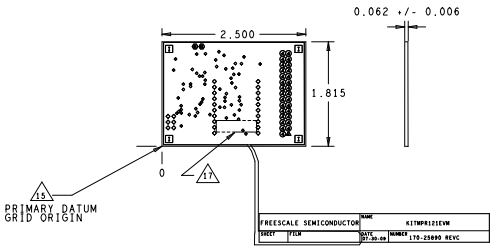
17. SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.
   - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

18. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .008"/.007"

19. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (94)

20. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ORIGINAL RELEASE	04-15-09	BO
	B	See SCH-25890, pg1 revision info	06-09-09	BO
	C	J14 replaced	07-30-09	BO



DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
⌖	15.0	+2.0/-2.0	PLATED	61
◎	40.0	+3.0/-3.0	PLATED	29
◇	40.0	+3.0/-3.0	PLATED	26
▲	40.0	+3.0/-3.0	PLATED	1
⊕	36.0	+3.0/-3.0	NON-PLATED	2
⊡	125.0	+3.0/-3.0	NON-PLATED	4

LAYER 1 COMPONENT SIDE 1 oz.
LAYER 2 SOLDER SIDE 1 oz.

DETAIL A
LAYER STACKUP
SCALE: NONE

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
.XX ±.01 ±1-30'
.XXX ±.005
✓ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS.
REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.
MATERIAL
FINISH
HEAT TREAT

PART NO. 170-25890

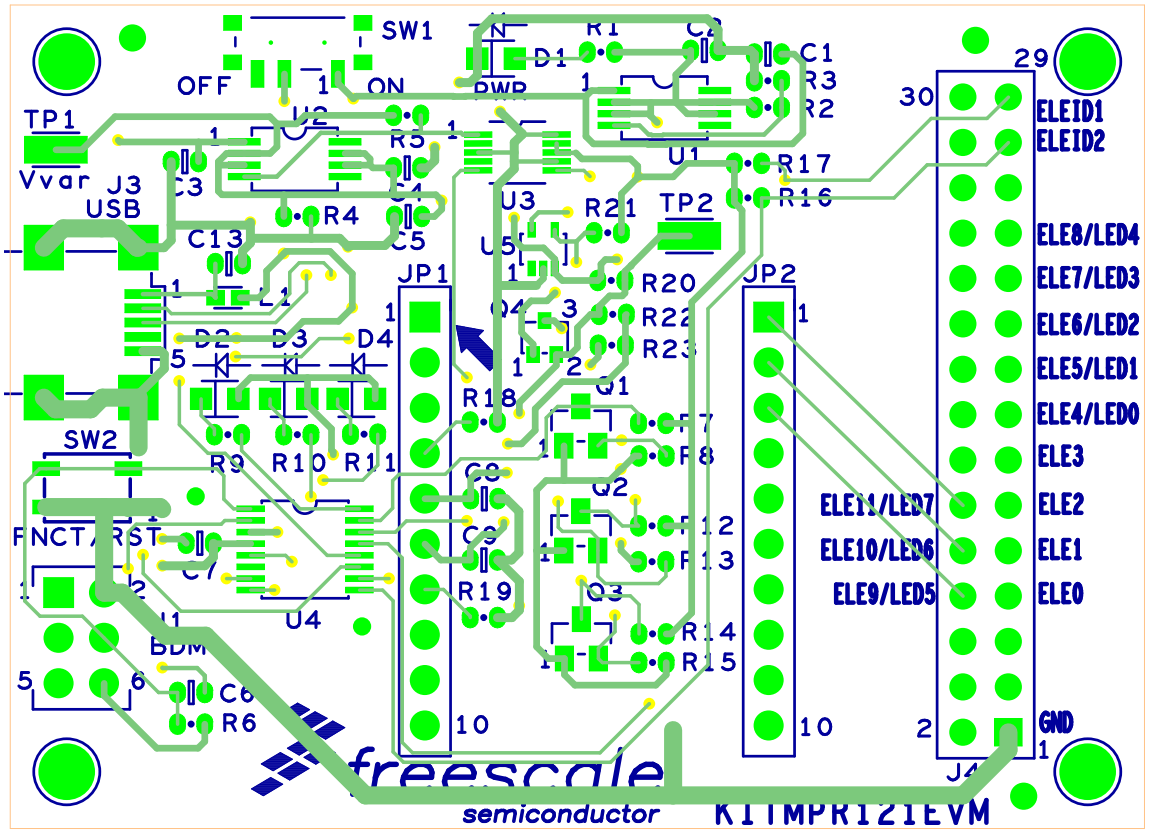
APPROVALS		DATE
DRAWN	S. MEJIA	07-30-09
CHECKED	B. Osoinac	07-30-09
DESIGN ENGINEER	B. Osoinac	07-30-09
	C. Teegarden	07-30-09

FREESCALE SEMICONDUCTOR
2100 E. Elliot Road, MD: EL 519 TEMPE, ARIZONA 85284 US

TITLE: PRINTED WIRING BOARD
KITMPR121EVM

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-25890	FAB-25890	C

SCALE: DO NOT SCALE DRAWING SHEET OF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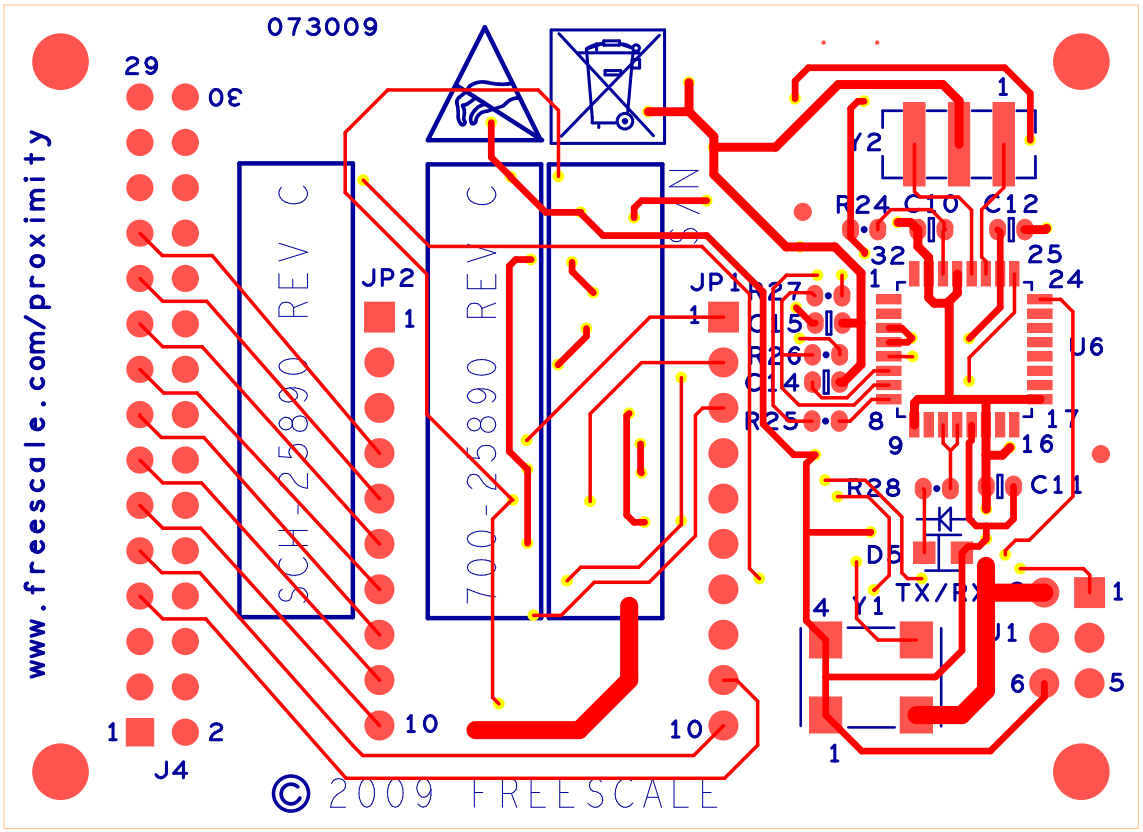
ON
TP1
Vvar
J3
USB
C13
JP1
JP2
D1
PWR
R1
C1
R3
R2
U1
R17
R16
TP2
R21
R20
R22
R23
U3
U5
Q4
Q1
Q2
Q3
R18
R19
R7
R8
R12
R13
R14
R15
C8
C9
D2
D3
D4
D5
R4
R5
C4
C5
C3
L1
SW2
R9
R10
R11
C7
U4
BDM
C6
R6
29
30
2
1
ELE1D1
ELE1D2
ELE8/LED4
ELE7/LED3
ELE6/LED2
ELE5/LED1
ELE4/LED0
ELE3
ELE2
ELE1
ELE0
ELE11/LED7
ELE10/LED6
ELE9/LED5
GND
freescale
semiconductor
KITMPR121EVM


073009
www.freescale.com/proximity
SCH-25890 REV C
700-25890 REV C
JP2
JP1
J4
Y2
Y1
U6
U1
D5
TX/RX
R24
C10
C12
C15
R26
C14
R25
R28
C11
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NSOR

Revisions

Rev	Description	Date
A	Original Design	4-15-09
B	updated text pg3	6-12-09

freescale semiconductor

RASG - Proximity
2100 E. Elliot Rd
Tempe, AZ 85284

ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Designer: B. Osoinach	Drawing Title: MPR121 DAUGHTER BOARD		
Drawn by: S. Mejia	Page Title: TITLE PAGE		
Approved: B. Osoinach	Size B	Document Number SCH-76723 PDF: SPF-76723	Rev B
	Date: Friday, June 12, 2009	Sheet 1 of 3	

wise Specified:
are in ohms, most are 1%, 1/10 Watt. Otherwise are 5%, 1/8 Watt.
All capacitors are in uF, some are 10% or 20%
All voltages are DC
All polarized capacitors are tantalum

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
_B Denotes - Active-Low Signal
<> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

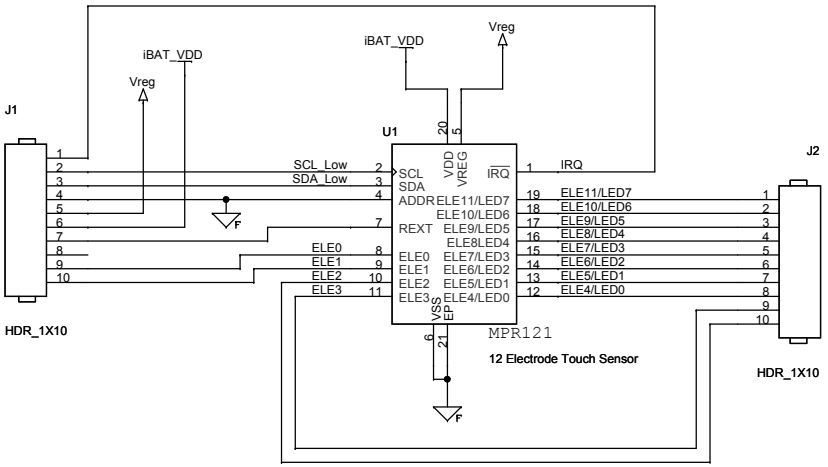
freescale semiconductor

Drawing Title: **MPR121 DAUGHTER BOARD**

Page Title: **NOTES**

Size	Document Number	Rev
B	SCH-76723 PDF: SPF-76723	B

Date: Friday, June 12, 2009 | Sheet 2 of 3



freescale semiconductor

Drawing Title:
MPR121 DAUGHTER BOARD

Page Title:
MPR121 SENSOR

Size	Document Number	Rev
B	SCH-76723 PDF: SPF-76723	B

Date: Friday, June 12, 2009 Sheet 3 of 3

NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 (LATEST REVISION).

2. THIS PWB MUST BE COMPLIANT WITH THE FREESCALE ECO REQUIREMENTS (DOCUMENT # 12MWS00047B) THESE REQUIREMENTS PROHIBIT THE USE OF CONTROLLED SUBSTANCES INCLUDING THOSE FOUND IN RoHS AND HALOGEN FREE STANDARDS. DISCLOSURE OF RESTRICTED AND REPORTABLE SUBSTANCES IS ALSO REQUIRED.

3. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.

4. BASE MATERIAL - FR4 (OR EQUIVALENT RoHS COMPLIANT) LAMINATE AND PREPREG SHALL MEET IPC-4101A-94
   MAXIMUM HALOGEN CONTENT - 0.10 ppm
   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.

5. COPPER FOIL WEIGHT - OUTSIDE LAYERS AND INNER LAYERS 1.0 OZ. SEE STACKUP DETAIL 'A'

6. OVERALL PCB THICKNESS 62 MILS. TOP AND BOTTOM FR4 LAYERS 10 MILS. INNER FR4-LAYER IS 40 MILS.

7. PLATING FINISH - BOTH SIDES ENIG (EMMERSIONLESS NICKEL IMMERSION GOLD):
   76.2-203.2 MILLIMICRON (3-8 MICROINCH) OF GOLD OVER
   2.540-5.080 MILLIMICRON (100-200 MICROINCH) MINIMUM NICKEL.

8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.

9. SOLDERMASK - GREEN COLOR (TAIYO OR EQUIVALENT), BOTH SIDES, HALOGEN FREE

10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.

11. ELECTRICAL TEST - 100% IPCD356.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY FREESCALE.

14. SOLDER SAMPLES TO BE PROVIDED.

15. BASIC GRID INCREMENT AT 1:1 IS .0001.

16. MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM FREESCALE.

17. SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.
   - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

18. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .008"/.007"

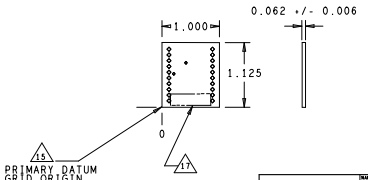
19. THE PWB WILL BE MARKED AS HALOGEN FREE BY USE OF AN INK STAMP (HF)

20. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (P6)

21. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)

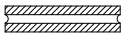
22. SOLDER STENCIL MUST BE 5MILS (0.13MM) MINIMUM THICKNESS. THICKNESS CAN BE ADJUSTED TO OPTIMIZE ASSEMBLY YIELDS.

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ORIGINAL RELEASE	04-15-09	OB
	B	Updated top and bottom silkscreen	05-28-09	OB



FREESCALE SEMICONDUCTOR		NAME	MPR121 DAUGHTER BOARD
SHEET	FILM	DATE 05-28-09	NUMBER 170-76723 REVB

DRILL CHART: TOP to BOTTOM ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
⋆	15.0	+2.0/-2.0	PLATED	2
◇	40.0	+3.0/-3.0	PLATED	20



LAYER 1 COMPONENT SIDE 1 oz.
LAYER 2 SOLDER SIDE 1 oz.

DETAIL A
LAYER STACKUP
SCALE: NONE

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
.XX ±.01 ±1-30'
.XXX ±.005
✓ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS.
REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.
MATERIAL
FINISH
HEAT TREAT

PART NO. 170-76723

APPROVALS		DATE
DRAWN	S. Mejia	05-28-09
CHECKED	B. Osoinach	05-28-09
DESIGN ENGINEER	B. Osoinach	05-28-09

FREESCALE SEMICONDUCTOR
2100 E. Elliot Road, TEMPE, ARIZONA 85284 USA

TITLE: EFIELD PRINTED WIRING BOARD
MPR121 DAUGHTER BOARD

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-76723	FAB-76723	B

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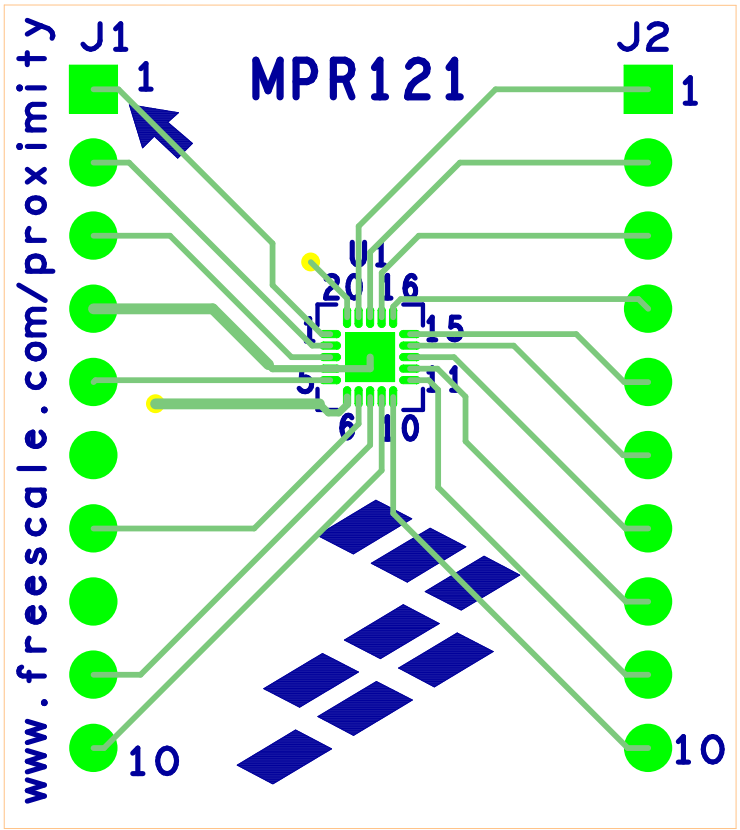
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www.freescale.com/proximity
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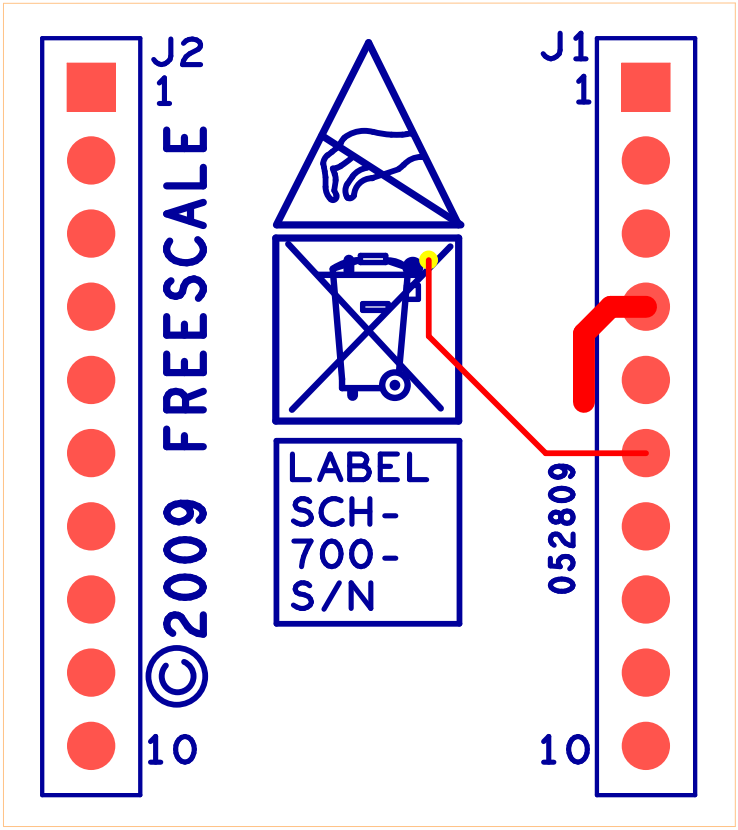
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J1
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SCH-
700-
S/N
052809

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LECTRODE

Revisions

Rev	Description	Date
A	Original Design	6-9-09

freescale semiconductor

RASG - Proximity
2100 E. Elliot Rd
Tempe, AZ 85284

ICAP Classification: FCP: ___ FIUO: _ PUBI: ___

Designer: B. Osoinach	Drawing Title: **PROXIMITY-IBAT**		
Drawn by: S. Mejia	Page Title: **TITLE PAGE**		
Approved: B. Osoinach	Size B	Document Number SCH-76753 PDF: SPF-76753	Rev A
	Date: Thursday, June 11, 2009	Sheet 1 of 3	

wise Specified:
are in ohms, most are 1%, 1/10 Watt. Otherwise are 5%, 1/8 Watt.
All capacitors are in uF, some are 10% or 20%
All voltages are DC
All polarized capacitors are tantalum

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
_B Denotes - Active-Low Signal
<> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

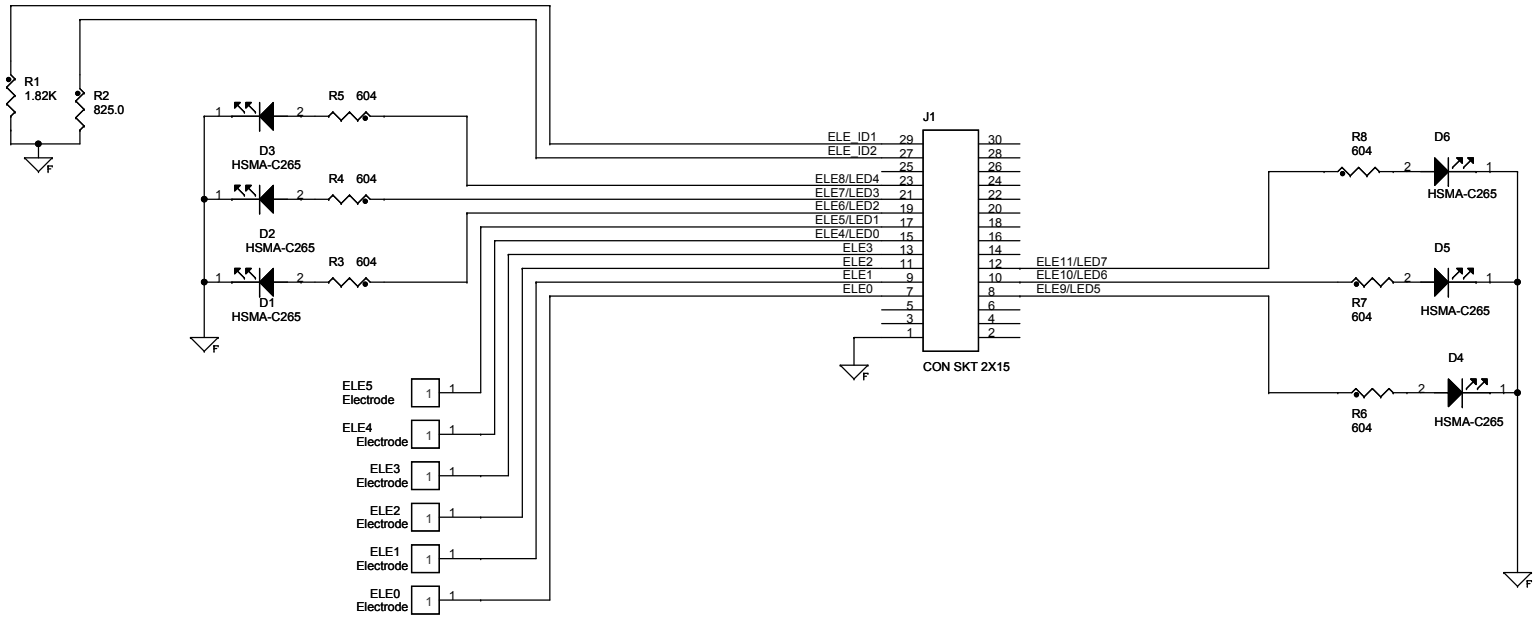
freescale semiconductor

Drawing Title: **PROXIMITY-IBAT**

Page Title: **NOTES**

Size	Document Number	Rev
B	SCH-76753 PDF: SPF-76753	A

Date: Tuesday, June 09, 2009 | Sheet 2 of 3



freescale semiconductor

Drawing Title:
PROXIMITY-IBAT

Page Title:
6 LED 6 ELECTRODE

Size	Document Number	Rev
B	SCH-76753 PDF: SPF-76753	A

Date: Friday, June 12, 2009 Sheet 3 of 3

NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 (LATEST REVISION).

2. THIS PWB MUST BE COMPLIANT WITH THE FREESCALE ECO REQUIREMENTS (DOCUMENT # 12MWS00047B) THESE REQUIREMENTS PROHIBIT THE USE OF CONTROLLED SUBSTANCES INCLUDING THOSE FOUND IN RoHS STANDARDS. DISCLOSURE OF RESTRICTED AND REPORTABLE SUBSTANCES IS ALSO REQUIRED.

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4. BASE MATERIAL - FR4 (OR EQUIVALENT RoHS COMPLIANT) LAMINATE AND PREPREG SHALL MEET IPC-4101A-94
   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.

5. COPPER FOIL WEIGHT - OUTSIDE LAYERS AND INNER LAYERS 1.0 OZ. SEE STACKUP DETAIL 'A'

6. OVERALL PCB THICKNESS 62 MILS. TOP AND BOTTOM FR4 LAYERS 10 MILS. INNER FR4-LAYER IS 40 MILS.

7. PLATING FINISH - BOTH SIDES ENIG (EMMERSIONLESS NICKEL IMMERSION GOLD):
   76.2-203.2 MILLIMICRON (3-8 MICROINCH) OF GOLD OVER
   2.540-5.080 MILLIMICRON (100-200 MICROINCH) MINIMUM NICKEL.

8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.

9. SOLDERMASK - GREEN COLOR (TAIYO OR EQUIVALENT), BOTH SIDES.

10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.

11. ELECTRICAL TEST - 100% IPCD356.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY FREESCALE.

14. SOLDER SAMPLES TO BE PROVIDED.

15. BASIC GRID INCREMENT AT 1:1 IS .0001.

16. MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM FREESCALE.

17. SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.
   - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

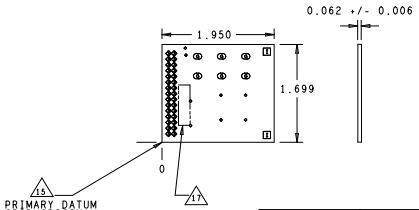
18. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .008"/.007"

19. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (PB)

20. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)

21. SOLDER STENCIL MUST BE 5MILS (0.13MM) MINIMUM THICKNESS. THICKNESS CAN BE ADJUSTED TO OPTIMIZE ASSEMBLY YIELDS.

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ORIGINAL RELEASE	06-09-09	OB



FREESCALE SEMICONDUCTOR	NAME: BASIC 6 ELECTRODE DEMO BOARD WITH LEDs	
SHEET	FILM	DATE: 06-09-09
		NUMBER: 170-76753 REVA

DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
⌖	15.0	+2.0/-2.0	PLATED	8
⌖	35.0	+3.0/-3.0	PLATED	30
⊗	87.0	+2.0/-2.0	NON-PLATED	6
⊡	125.0	+3.0/-3.0	NON-PLATED	2

LAYER 1 COMPONENT SIDE 1 oz.
LAYER 2 SOLDER SIDE 1 oz.

DETAIL A
LAYER STACKUP
SCALE: NONE

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
.XX ±.01 ±1-30'
.XXX ±.005
✓ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS.
REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.
MATERIAL
FINISH
HEAT TREAT

PART NO. 170-76753

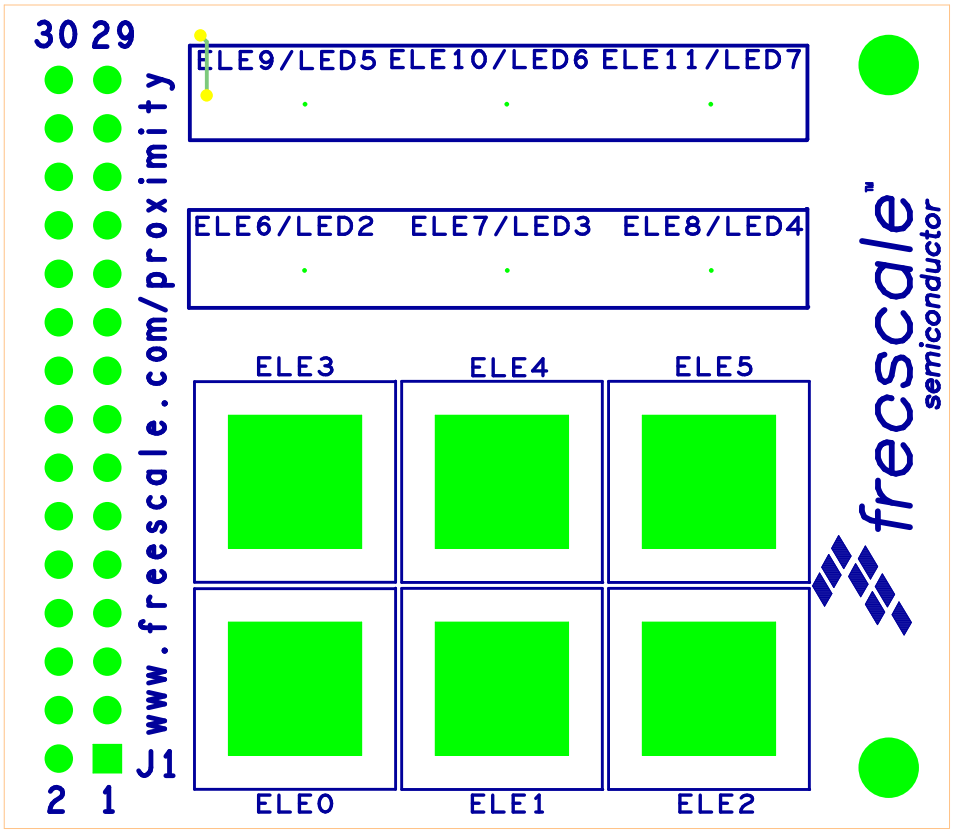
APPROVALS		DATE
DRAWN	S. Mejia	06-09-09
CHECKED	B. Osoinach	06-09-09
DESIGN ENGINEER	B. Osoinach	06-09-09

FREESCALE SEMICONDUCTOR
2100 E. Elliot Road, TEMPE, ARIZONA 85284 USA

TITLE: PROXIMITY PRINTED WIRING BOARD BASIC 6ELECTRODE DEMOBOARD LED

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-76753	FAB-76753	A

SCALE | DO NOT SCALE DRAWING | SHEET OF


30 29
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www.freescale.com/proximity
ELE9/LED5 ELE10/LED6 ELE11/LED7
ELE6/LED2 ELE7/LED3 ELE8/LED4
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ELE0
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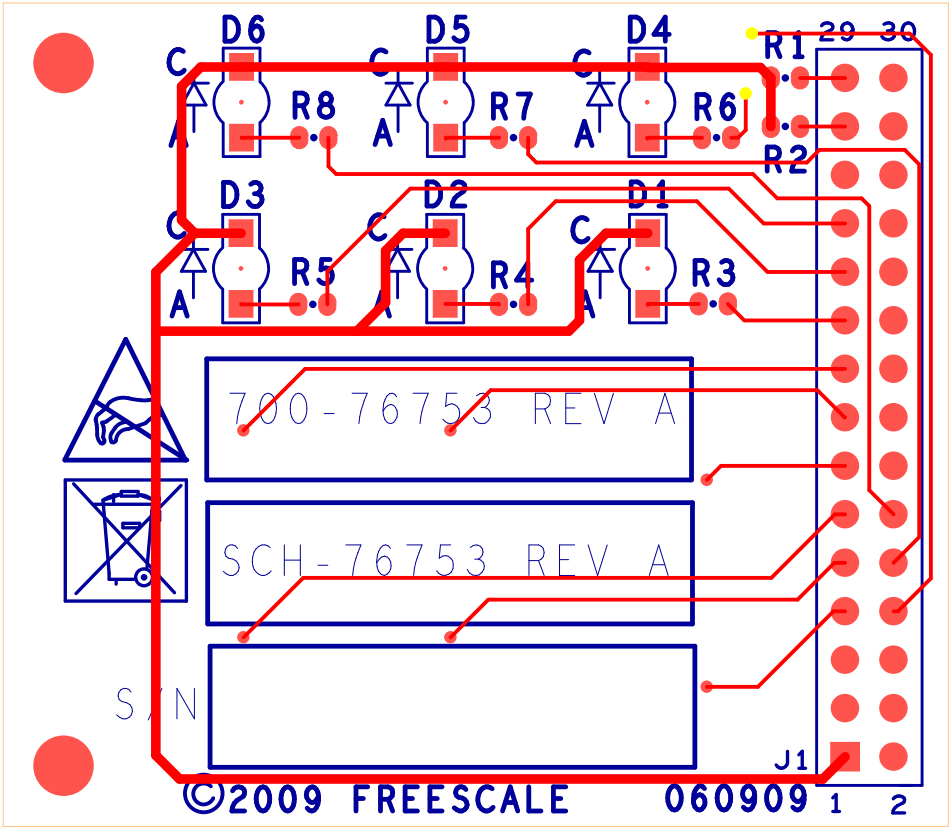
freescale
semiconductor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R5
R4
R3
700-76753 REV A
SCH-76753 REV A
S/N
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Revisions

Rev	Description	Date
A	Original Design	06-09-09

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RASG - Proximity
2100 E. Elliot Rd
Tempe, AZ 85284

ICAP Classification: FCP: ____ FIUO: _ PUBI: ____

Designer: B. Osoinach	Drawing Title: **PROXIMITY-IBAT**		
Drawn by: S. Mejia	Page Title: **TITLE PAGE**		
Approved: B. Osoinach	Size B	Document Number SCH-76724 PDF: SPF-76724	Rev A
	Date: Thursday, June 11, 2009	Sheet 1 of 3	

wise Specified:
are in ohms, most are 1%, 1/10 Watt. Otherwise are 5%, 1/8 Watt.
All capacitors are in uF, some are 10% or 20%
All voltages are DC
All polarized capacitors are tantalum

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
_B Denotes - Active-Low Signal
<> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

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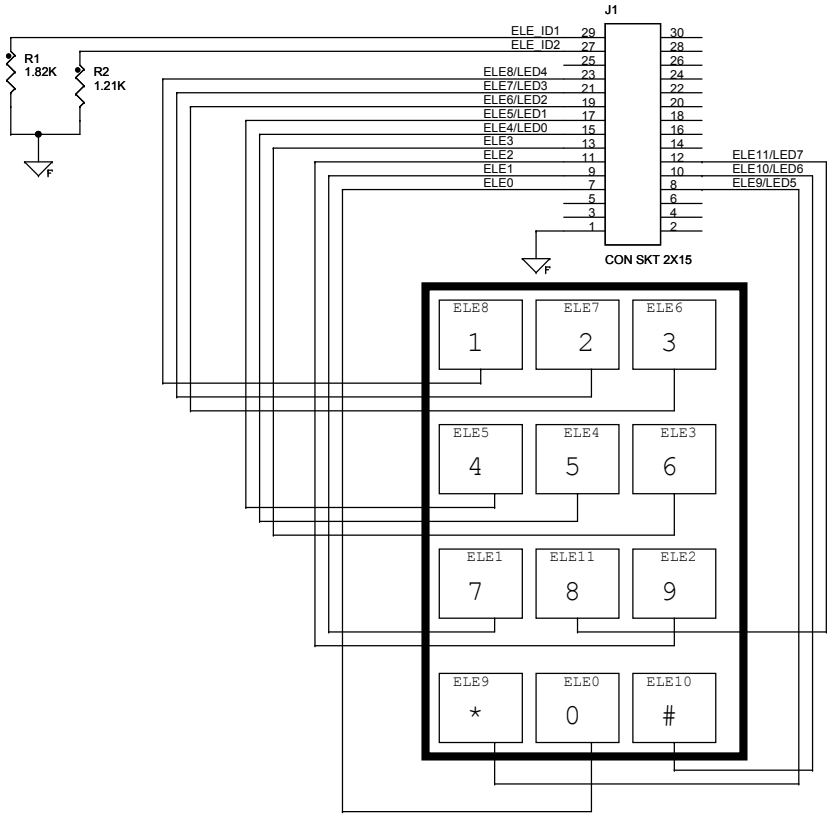
Drawing Title: **PROXIMITY-IBAT**

Page Title: **NOTES**

Size	Document Number	Rev
B	SCH-76724 PDF: SPF-76724	A

Date: Wednesday, June 10, 2009 | Sheet 2 of 3



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Drawing Title:
PROXIMITY-IBAT

Page Title:
12 ELECTRODES

Size	Document Number	Rev
B	SCH-76724 PDF: SPF-76724	A

Date: Friday, June 12, 2009 | Sheet 3 of 3

NOTES (UNLESS OTHERWISE SPECIFIED):

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 (LATEST REVISION).

2. THIS PWB MUST BE COMPLIANT WITH THE FREESCALE ECO REQUIREMENTS (DOCUMENT # 12MWS00047B) THESE REQUIREMENTS PROHIBIT THE USE OF CONTROLLED SUBSTANCES INCLUDING THOSE FOUND IN RoHS STANDARDS. DISCLOSURE OF RESTRICTED AND REPORTABLE SUBSTANCES IS ALSO REQUIRED.

3. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.

4. BASE MATERIAL - FR4 (OR EQUIVALENT RoHS COMPLIANT) LAMINATE AND PREPREG SHALL MEET IPC-4101A-94
   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.

5. COPPER FOIL WEIGHT - OUTSIDE LAYERS AND INNER LAYERS 1.0 OZ. SEE STACKUP DETAIL 'A'

6. OVERALL PCB THICKNESS 62 MILS. TOP AND BOTTOM FR4 LAYERS 10 MILS. INNER FR4-LAYER IS 40 MILS.

7. PLATING FINISH - BOTH SIDES ENIG (EMMERSIONLESS NICKEL IMMERSION GOLD):
   76.2-203.2 MILLIMICRON (3-8 MICROINCH) OF GOLD OVER
   2.540-5.080 MILLIMICRON (100-200 MICROINCH) MINIMUM NICKEL.

8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.

9. SOLDERMASK - GREEN COLOR (TAIYO OR EQUIVALENT), BOTH SIDES.

10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.

11. ELECTRICAL TEST - 100% IPCD356.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY FREESCALE.

14. SOLDER SAMPLES TO BE PROVIDED.

15. BASIC GRID INCREMENT AT 1:1 IS .0001.

16. MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM FREESCALE.

17. SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.
   - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

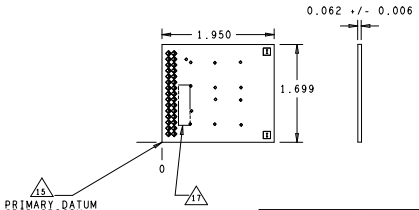
18. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .008"/.007"

19. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (P6)

20. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)

21. SOLDER STENCIL MUST BE 5MILS (0.13MM) MINIMUM THICKNESS. THICKNESS CAN BE ADJUSTED TO OPTIMIZE ASSEMBLY YIELDS.

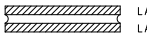
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
	A	ORIGINAL RELEASE	06-06-09	OB



FREESCALE SEMICONDUCTOR			NAME: BASIC 12 ELECTRODE DEMO BOARD
SHEET	FILM	DATE: 06-09-09	NUMBER: 170-76724 REVA

8 DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILS

FIGURE	SIZE	TOLERANCE	PLATED	QTY
⋆	15.0	+2.0/-2.0	PLATED	13
✥	35.0	+3.0/-3.0	PLATED	30
⊡	125.0	+3.0/-3.0	NON-PLATED	2



LAYER 1 COMPONENT SIDE 1 oz.
LAYER 2 SOLDER SIDE 1 oz.

DETAIL A
LAYER STACKUP
SCALE: NONE

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
.XX ±.01 ±1-30'
.XXX ±.005
✓ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS.
REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.
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PART NO. 170-76724

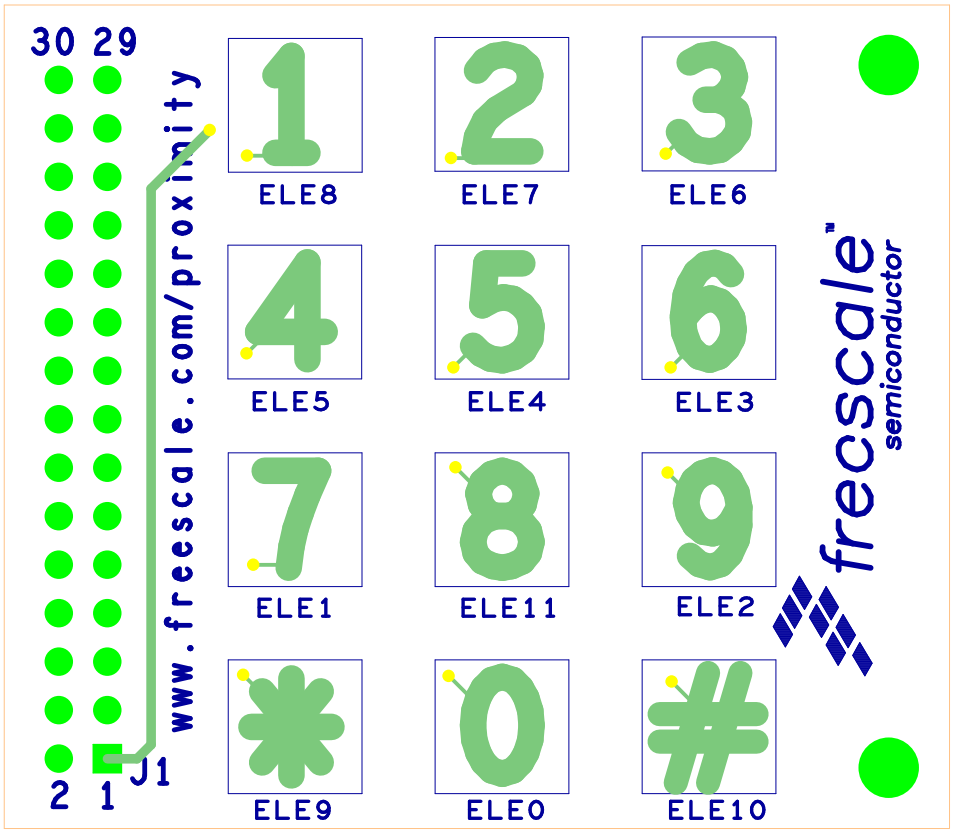
APPROVALS		DATE
DRAWN	S. Mejia	06-09-09
CHECKED	B. Osoinach	06-09-09
DESIGN ENGINEER	B. Osoinach	06-09-09

FREESCALE SEMICONDUCTOR
2100 E. Elliot Road, TEMPE, ARIZONA 85284 USA

TITLE: IBAT PRINTED WIRING BOARD
BASIC 12ELECTRODE DEMOBOARD

SIZE	CAD FILE NAME	DWG. NO.	REV
D	LAY-76724	FAB-76724	A

SCALE: DO NOT SCALE DRAWING SHEET OF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www.freescale.com/proximity
ELE8
ELE7
ELE6
ELE5
ELE4
ELE3
ELE1
ELE11
ELE2
ELE9
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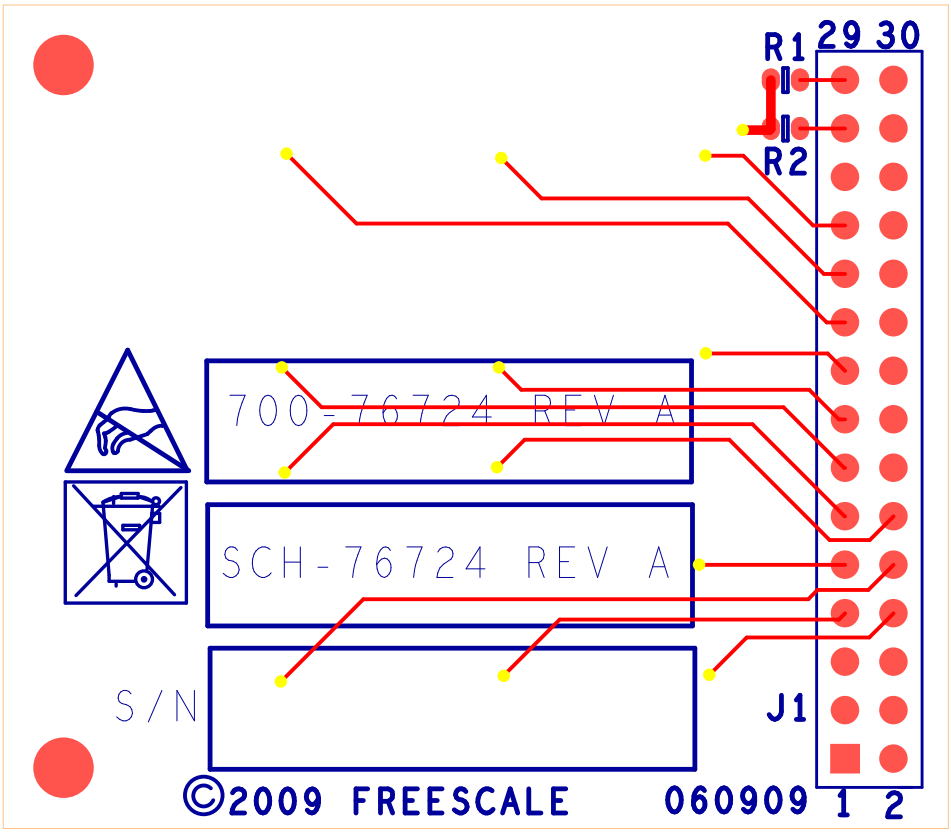
ELE10
freescale
semiconductor


R1
29 30
R2
700-76724 REV A
SCH-76724 REV A
S/N
J1
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1 2