

NX5P2924D

Logic controlled high-side power switch

Rev. 1.0 — 21 June 2022

Product data sheet

1 General description

The NX5P2924D is a high-side load switch which features a low ON resistance N-channel MOSFET with controlled slew rate that supports 2.5 A of continuous current. Designed for operation from 0.8 V to 5.5 V, it is used in power domain isolation applications to reduce power dissipation and extend battery life. An output pull-down transistor has been integrated for fast discharge of capacitive load. The enable logic includes integrated logic level translation making the device compatible with lower voltage processors and controllers. The NX5P2924D is ideal for portable, battery operated applications due to low ground current.

2 Features and benefits

- Wide supply voltage range from 0.8 V to 5.5 V
- Very low ON resistance:
 - 18 m Ω (typical) at a supply voltage of 1.2 V
 - 18 m Ω (typical) at a supply voltage of 1.8 V
- High noise immunity
- High current handling capability (2.5 A continuous current)
- Turn-on slew rate limiting
- ESD protection:
 - HBM JESD22-A114F Class 3A exceeds 5000 V
 - CDM AEC-Q100-011 revision B exceeds 1000 V
- Specified from -40 °C to +85 °C

3 Applications

- Cell phone
- Digital cameras and audio devices
- Portable and battery-powered equipment

4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
NX5P2924DUK	NX5P2924D	4D	wafer level chip-size package; 6 terminals; 0.5 mm pitch; 1.39 mm x 0.89 mm x 0.465 mm body	SOT1381-2



4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method ^[1]	Minimum order quantity	Temperature
NX5P2924DUK	NX5P2924DUKZ	WLCSP6	REEL 7" Q1 DP chips	3000	T _{amb} = -40 °C to +85 °C

[1] Standard packing quantities and other packaging data are available at www.nxp.com/packages/.

5 Functional diagram

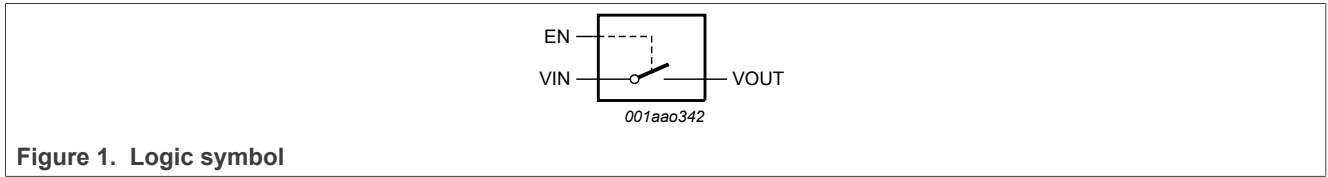


Figure 1. Logic symbol

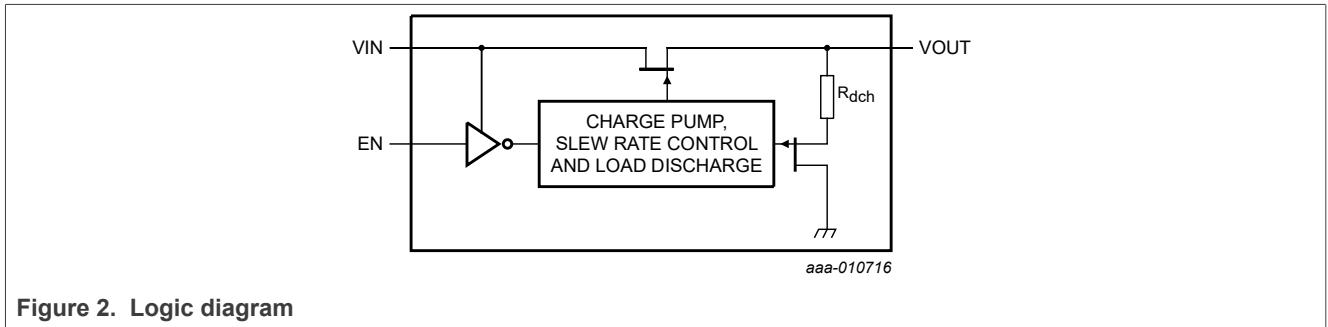


Figure 2. Logic diagram

6 Pinning information

6.1 Pinning

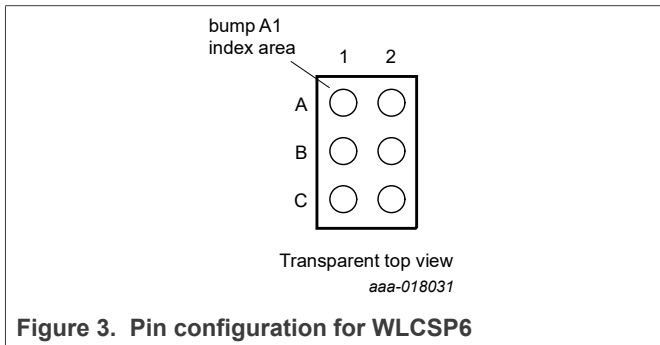


Figure 3. Pin configuration for WLCSP6

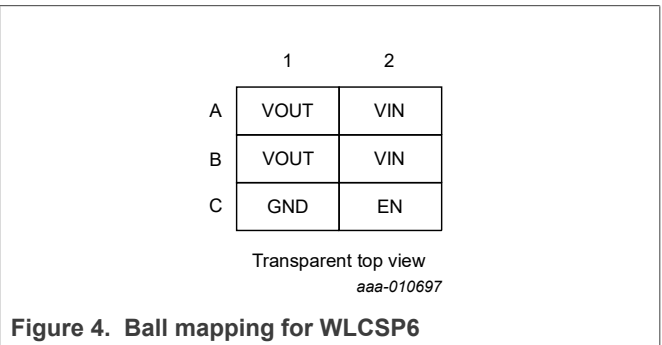


Figure 4. Ball mapping for WLCSP6

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VIN	A2, B2	input voltage
GND	C1	ground (0 V)
EN	C2	enable input (active HIGH)
VOUT	A1, B1	output voltage

7 Functional description

Table 4. Function table^[1]

Input EN	Switch
L	switch OFF
H	switch ON

[1] H = HIGH voltage level; L = LOW voltage level.

8 Application diagram

The NX5P2924D is typically used in portable, battery operated device. Pin EN enables the NX5P2924D. Slew rate controlled in-rush current reduction circuits function during switching.

The VOUT discharge circuit will be active when NX5P2924D main FET is switched off by pulling EN pin low. The circuit will discharge the VOUT voltage through approximately 1.3 kΩ resistance to GND. The discharge circuit will automatically be disconnected after VOUT drops below 10 % of the rail.

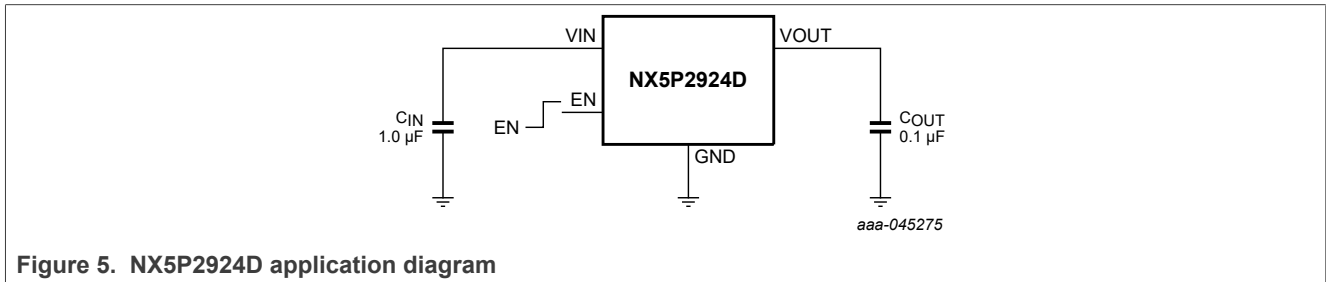


Figure 5. NX5P2924D application diagram

9 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _I	input voltage	input EN	[1] -0.5	+6.0	V
		input VIN	[2] -0.5	+6.0	V
V _{SW}	switch voltage	output VOUT	[2] -0.5	V _{I(VIN)}	V
I _{IK}	input clamping current	input EN: V _{I(EN)} < -0.5 V	-50	-	mA

Table 5. Limiting values...continued

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
I _{SK}	switch clamping current	input VIN: V _{I(VIN)} < -0.5 V	-50	-	mA
		output VOUT: V _{O(VOUT)} < -0.5 V	-50	-	mA
		output VOUT: V _{O(VOUT)} > V _{I(VIN)} + 0.5 V	-	50	mA
I _{SW}	switch current	V _{SW} > -0.5 V	-	±2500	mA
		pulsed, 100 ms pulse, 2 % duty cycle	-	±5000	mA
T _{j(max)}	maximum junction temperature		-40	+125	°C
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation		[3]	470	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[3] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed in conjunction with lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 85 °C and the use of a two layer PCB.

10 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _I	input voltage	input EN	0	5.5	V
		input VIN	0.8	5.5	V
T _{amb}	ambient temperature		-40	+85	°C

11 Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit	
R _{th(j-a)}	thermal resistance from junction to ambient		[1]	139	K/W

[1] R_{th(j-a)} is dependent upon board layout. To minimize R_{th(j-a)}, ensure that all pins have a solid connection to larger copper layer areas. In multi-layer PCBs, the second layer should be used to create a large heat spreader area below the device. Avoid using solder-stop varnish under the device.

12 Static characteristics

Table 8. Static characteristics

V_{I(VIN)} = 1.0 V to 5.5 V, unless otherwise specified; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	EN input; V _{I(VIN)} = 0.8 V	0.6	-	-	0.6	-	V
		EN input; V _{I(VIN)} = 1.0 V to 1.2 V	0.9	-	-	0.9	-	V
		EN input; V _{I(VIN)} = 1.2 V to 2.5 V	1.2	-	-	1.2	-	V
		EN input; V _{I(VIN)} = 2.5 V to 5.5 V	1.2	-	-	1.2	-	V

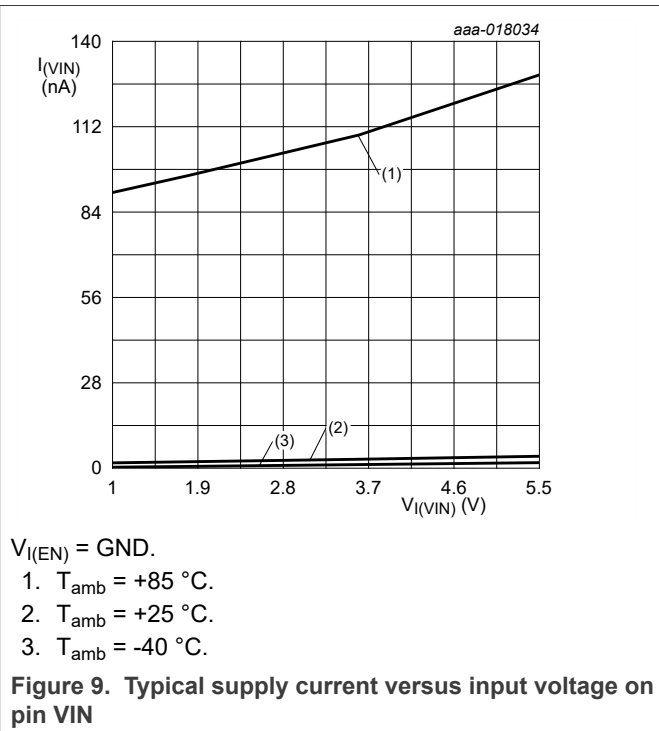
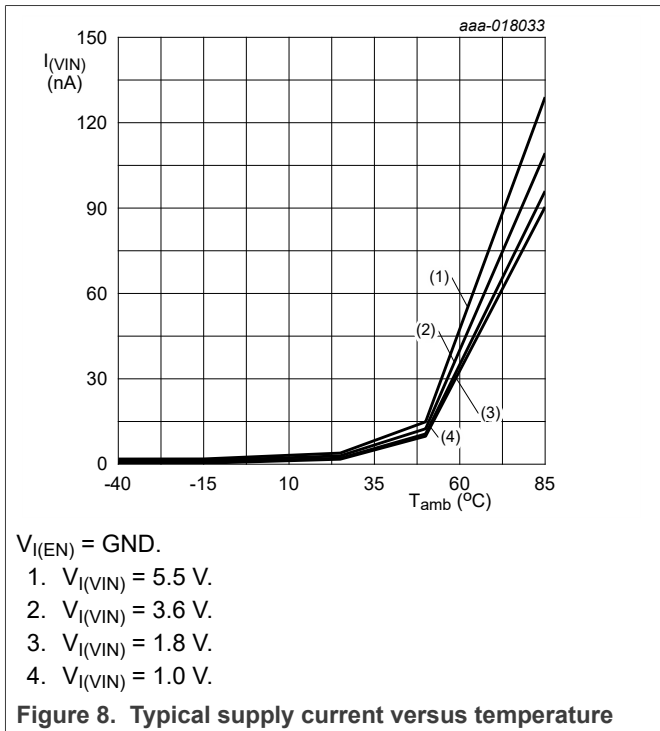
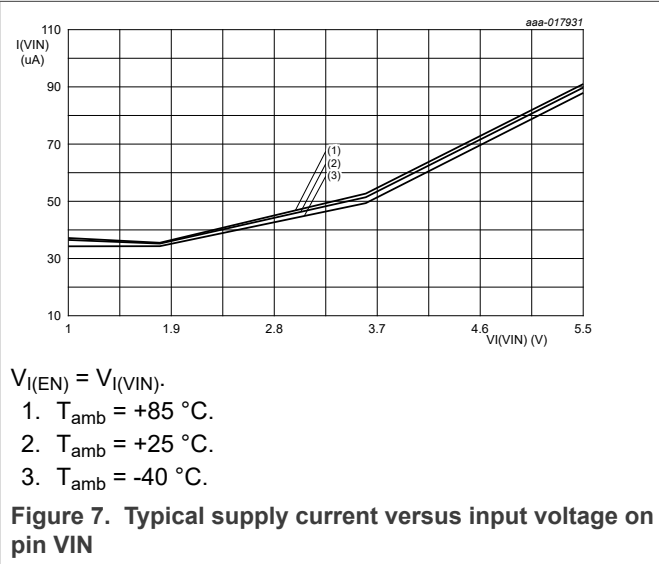
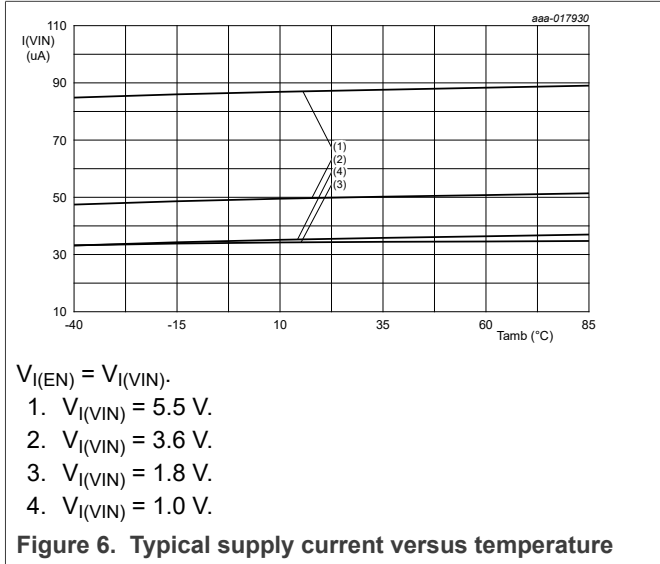
Table 8. Static characteristics...continued

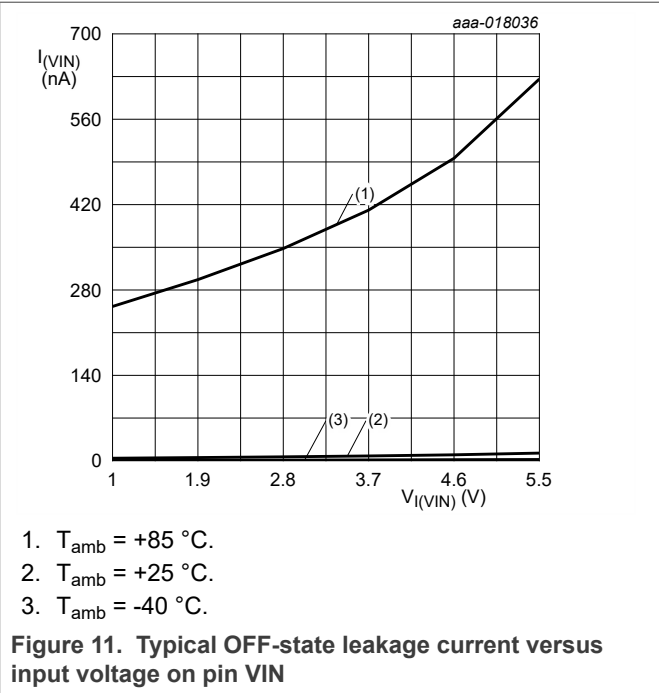
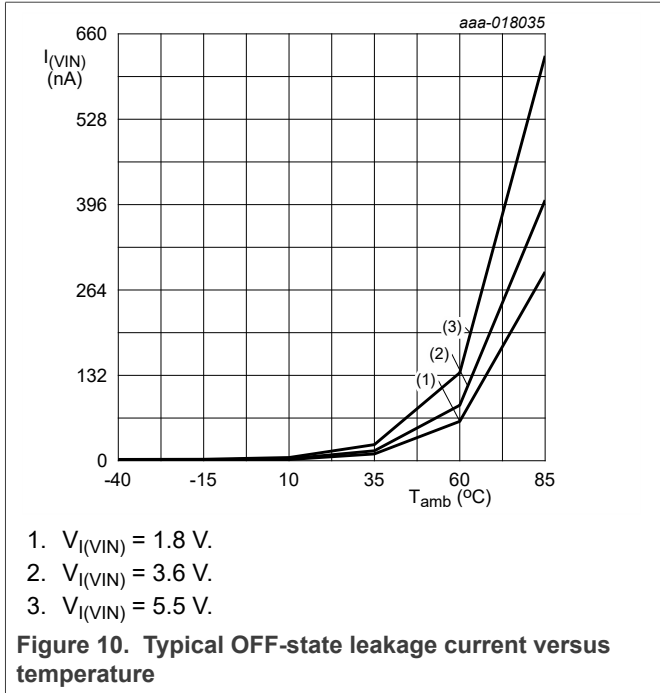
$V_{I(VIN)}$ = 1.0 V to 5.5 V, unless otherwise specified; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IL}	LOW-level input voltage	EN input; V _{I(VIN)} = 0.8 V	-	-	0.25	-	0.25	V
		EN input; V _{I(VIN)} = 1.0 V to 1.2 V	-	-	0.3	-	0.3	V
		EN input; V _{I(VIN)} = 1.2 V to 2.5 V	-	-	0.4	-	0.4	V
		EN input; V _{I(VIN)} = 2.5 V to 5.5 V	-	-	0.6	-	0.6	V
I _I	input leakage current	EN input; V _{I(EN)} = 0.9 V to 5.5 V	-	-	-	-	0.1	µA
R _{dch}	discharge resistance	VOUT output; V _{I(VIN)} = 0.8 V	-	4.00	-	-	-	kΩ
		VOUT output; V _{I(VIN)} = 1.0 V	-	1.40	-	-	-	kΩ
		VOUT output; V _{I(VIN)} = 1.2 V	-	1.30	-	-	-	kΩ
		VOUT output; V _{I(VIN)} = 1.8 V	-	1.27	1.50	-	-	kΩ
		VOUT output; V _{I(VIN)} = 3.3 V	-	1.25	1.50	-	-	kΩ
		VOUT output; V _{I(VIN)} = 5.5 V	-	1.25	1.50	-	-	kΩ
I _{DD}	supply current	VOUT open						
		EN = HIGH; V _{I(VIN)} = 1.0 V; see Figure 6 and Figure 7	-	35	-	-	50	µA
		EN = HIGH; V _{I(VIN)} = 1.8 V; see Figure 6 and Figure 7	-	35	-	-	50	µA
		EN = HIGH; V _{I(VIN)} = 3.6 V; see Figure 6 and Figure 7	-	50	-	-	70	µA
		EN = HIGH; V _{I(VIN)} = 5.5 V; see Figure 6 and Figure 7	-	85	-	-	110	µA
		EN = LOW; see Figure 8 and Figure 9	-	0.1	-	-	1.5	µA
I _{S(OFF)}	OFF-state leakage current	EN = LOW; V _{I(VIN)} = 1.8 V; V _{I(VOUT)} = 0 V; see Figure 10 and Figure 11	-	-0.5	-	-3.5	-	µA
		EN = LOW; V _{I(VIN)} = 3.6 V; V _{I(VOUT)} = 0 V; see Figure 10 and Figure 11	-	-0.5	-	-5.0	-	µA
		EN = LOW; V _{I(VIN)} = 5.5 V; V _{I(VOUT)} = 0 V; see Figure 10 and Figure 11	-	-0.5	-	-7.5	-	µA
C _I	input capacitance	EN	-	3	-	-	-	pF
C _{S(ON)}	ON-state capacitance	VIN; VOUT	-	-	0.5	-	0.5	nF

[1] All typical values are measured at V_{I(VIN)} = 3.6 V and T_{amb} = 25 °C unless otherwise specified.

12.1 Graphs





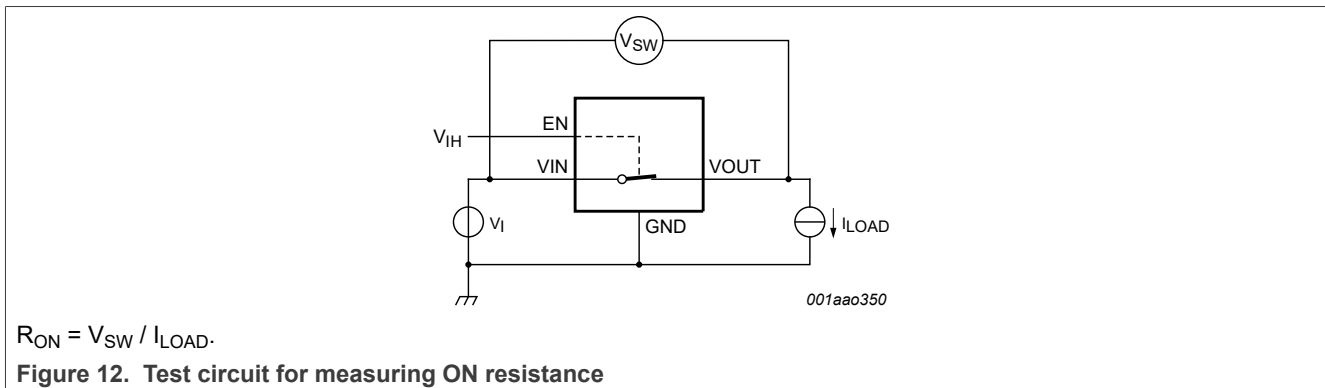
12.2 ON resistance

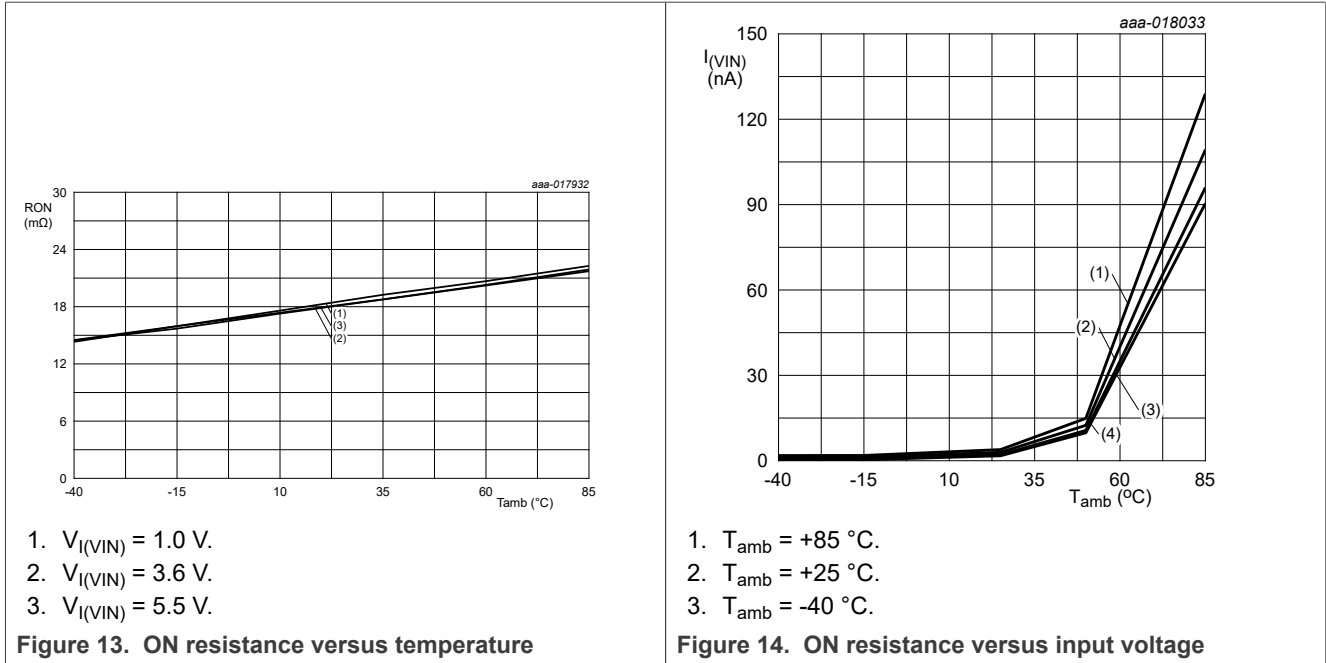
Table 9. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	$T_{amb} = 25\text{ °C}$			$T_{amb} = -40\text{ °C to }+85\text{ °C}$		Unit
			Min	Typ	Max	Min	Max	
R_{ON}	ON resistance	$V_{I(EN)} = 1.5\text{ V}$; $I_{LOAD} = 200\text{ mA}$; see Figure 12 , Figure 13 and Figure 14						
		$V_{I(VIN)} = 0.8\text{ V}$	-	21	-	-	26	mΩ
		$V_{I(VIN)} = 0.9\text{ V}$	-	19	-	-	24	mΩ
		$V_{I(VIN)} = 1.0\text{ V to }5.5\text{ V}$	-	18	-	-	23	mΩ

12.3 ON resistance test circuit and graphs





13 Dynamic characteristics

Table 10. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 16.

Symbol	Parameter	Conditions	$T_{amb} = 25 \text{ }^\circ\text{C}$			$T_{amb} = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
t_{en}	enable time	EN to VOUT; see Figure 15, Figure 1717, Figure 18 and Figure 19						
		$V_{I(VIN)} = 0.8 \text{ V}$	-	630	-	-	-	μs
		$V_{I(VIN)} = 1.0 \text{ V}$	-	530	-	270	-	μs
		$V_{I(VIN)} = 3.6 \text{ V}$	-	510	-	330	-	μs
t_{dis}	disable time	EN to VOUT; see Figure 15 and Figure 20						
		$V_{I(VIN)} = 0.8 \text{ V}$	-	90	-	-	-	μs
		$V_{I(VIN)} = 1.0 \text{ V}$	-	18	-	-	-	μs
		$V_{I(VIN)} = 3.6 \text{ V}$	-	4	-	-	-	μs
t_{on}	turn-on time	EN to VOUT; see Figure 15, Figure 1717, Figure 18 and Figure 19						
		$V_{I(VIN)} = 0.8 \text{ V}$	-	990	-	-	-	μs
		$V_{I(VIN)} = 1.0 \text{ V}$	-	940	-	520	-	μs
		$V_{I(VIN)} = 3.6 \text{ V}$	-	1290	-	830	-	μs

Table 10. Dynamic characteristics...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 16.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			T _{amb} = -40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
		V _{I(VIN)} = 5.5 V	-	1480	-	1020	-	µs
t _{off}	turn-off time	EN to VOUT; see Figure 15 and Figure 20						µs
		V _{I(VIN)} = 0.8 V	-	100	-	-	-	µs
		V _{I(VIN)} = 1.0 V	-	20	-	-	-	µs
		V _{I(VIN)} = 3.6 V	-	6	-	-	-	µs
		V _{I(VIN)} = 5.5 V	-	5	-	-	-	µs
t _{TLH}	LOW to HIGH output transition time	VOUT; see Figure 15						
		V _{I(VIN)} = 0.8 V	-	360	-	-	-	µs
		V _{I(VIN)} = 1.0 V	-	410	-	160	-	µs
		V _{I(VIN)} = 3.6 V	-	780	-	430	-	µs
		V _{I(VIN)} = 5.5 V	-	970	-	590	-	µs
t _{THL}	HIGH to LOW output transition time	VOUT; see Figure 15						
		V _{I(VIN)} = 0.8 V	-	5	-	-	-	µs
		V _{I(VIN)} = 1.0 V	-	2.2	-	-	-	µs
		V _{I(VIN)} = 3.6 V	-	2.2	-	-	-	µs
		V _{I(VIN)} = 5.5 V	-	2.2	-	-	-	µs

13.1 Waveforms, graphs and test circuit

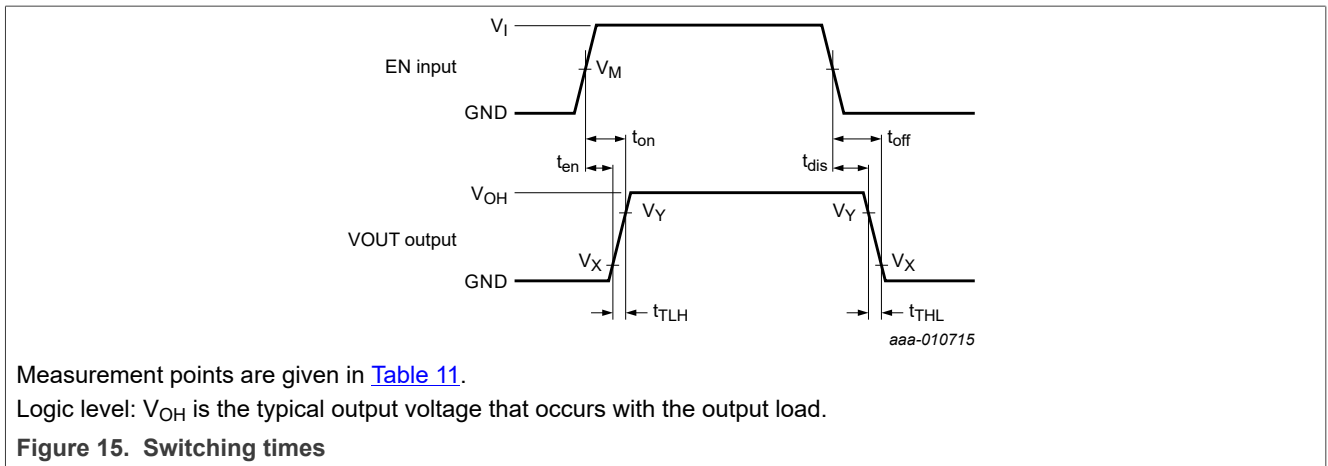
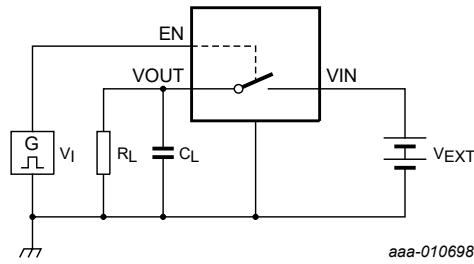


Table 11. Measurement points

Supply voltage	EN Input	Output	
V _{I(VIN)}	V _M	V _X	V _Y
1.0 V to 5.5 V	0.5 × V _{I(EN)}	0.1 × V _{OH}	0.9 × V _{OH}



Test data is given in [Table 12](#).

Definitions test circuit:

R_L = Load resistance.

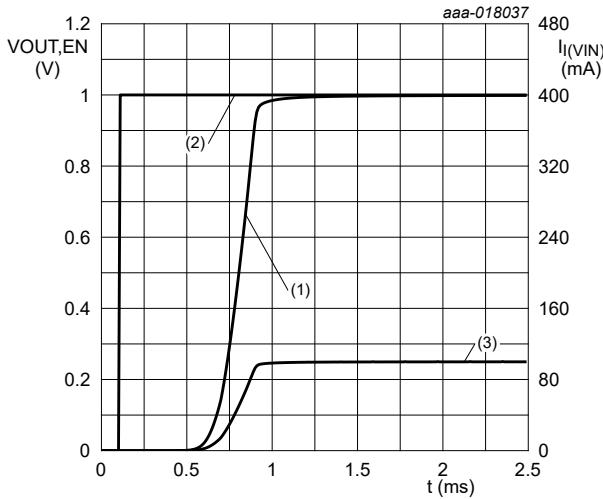
C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Figure 16. Test circuit for measuring switching times

Table 12. Test data

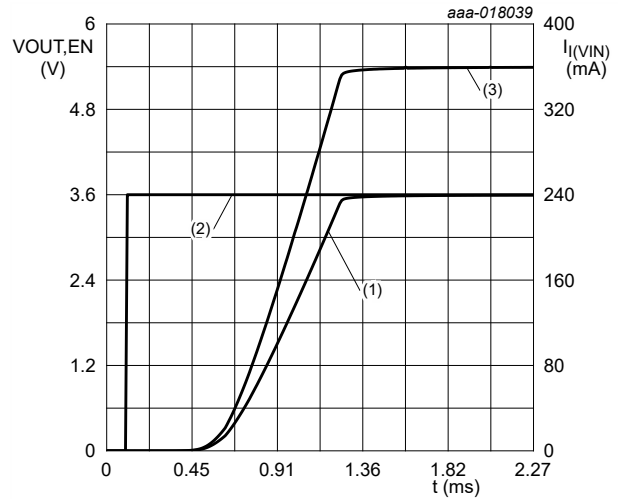
Supply voltage	Input	Load	
V_{EXT}	$V_{I(EN)}$	C_L	R_L
1.0 V to 5.5 V	1.5 V	0.1 μ F	10 Ω



$V_{I(VIN)} = 1$ V; $R_L = 10$ Ω ; $C_L = 0.1$ μ F; $T_{amb} = 25$ $^{\circ}$ C.

1. VOUT
2. EN
3. $I_{I(VIN)}$

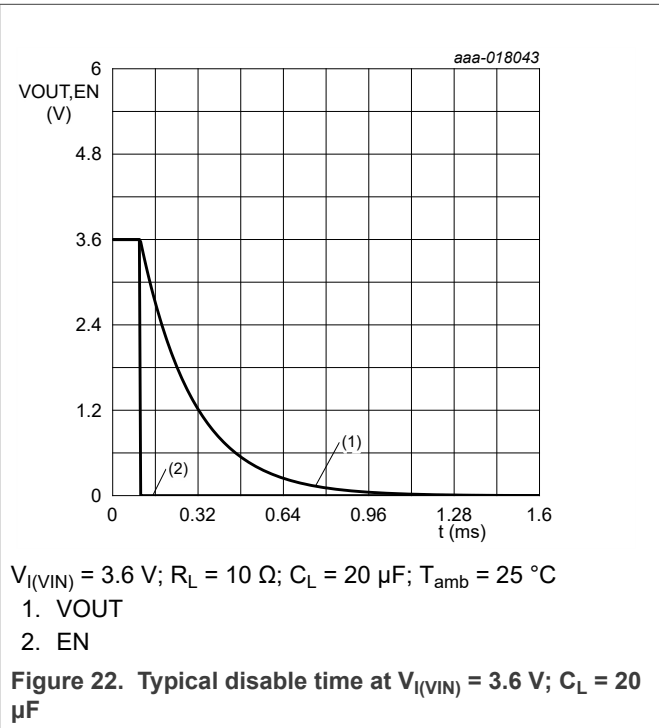
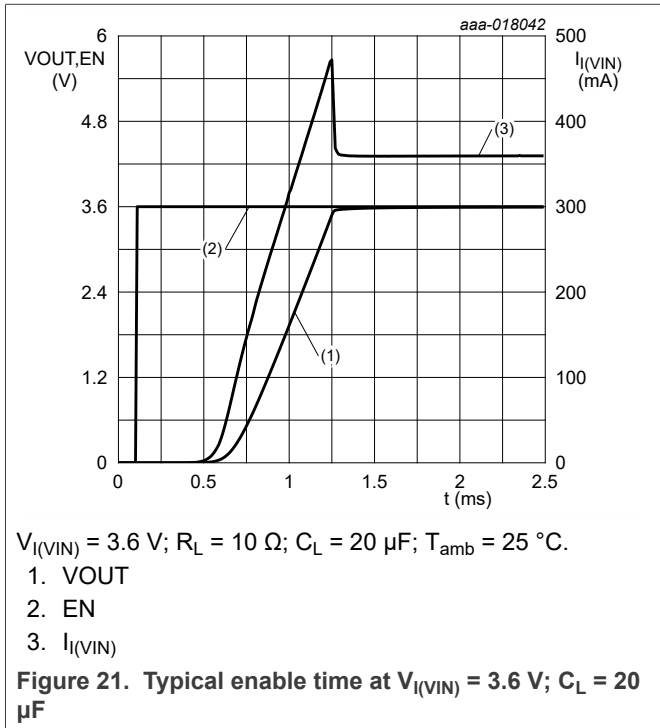
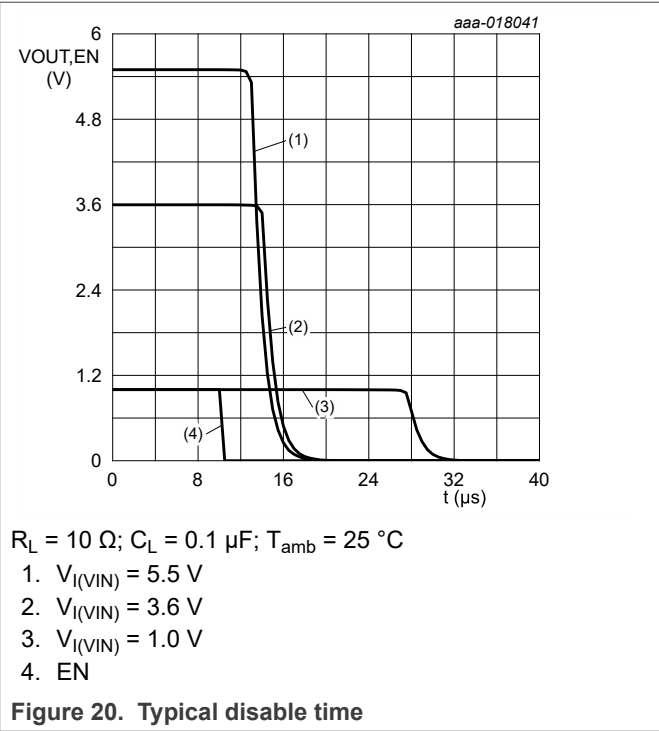
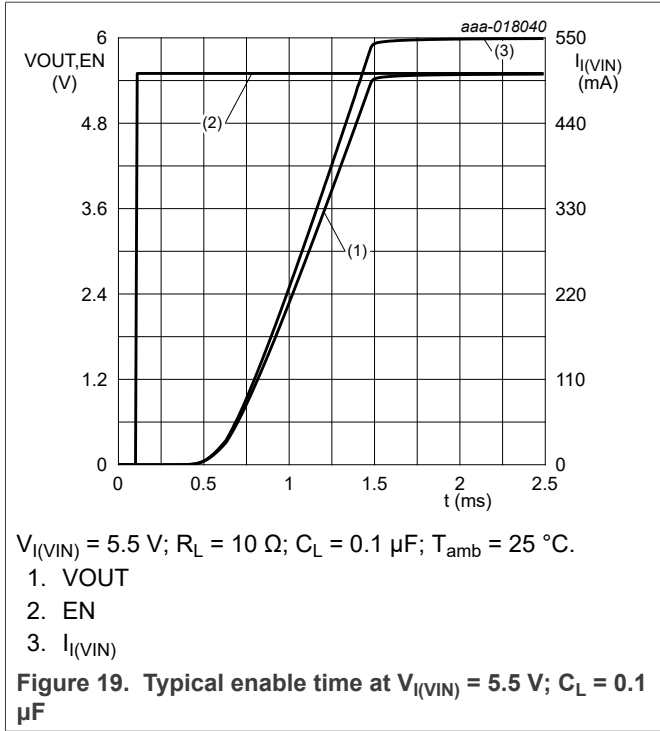
Figure 17. Typical enable time at $V_{I(VIN)} = 1$ V; $C_L = 0.1$ μ F



$V_{I(VIN)} = 3.6$ V; $R_L = 10$ Ω ; $C_L = 0.1$ μ F; $T_{amb} = 25$ $^{\circ}$ C.

1. VOUT
2. EN
3. $I_{I(VIN)}$

Figure 18. Typical enable time at $V_{I(VIN)} = 3.6$ V; $C_L = 0.1$ μ F



14 Package outline

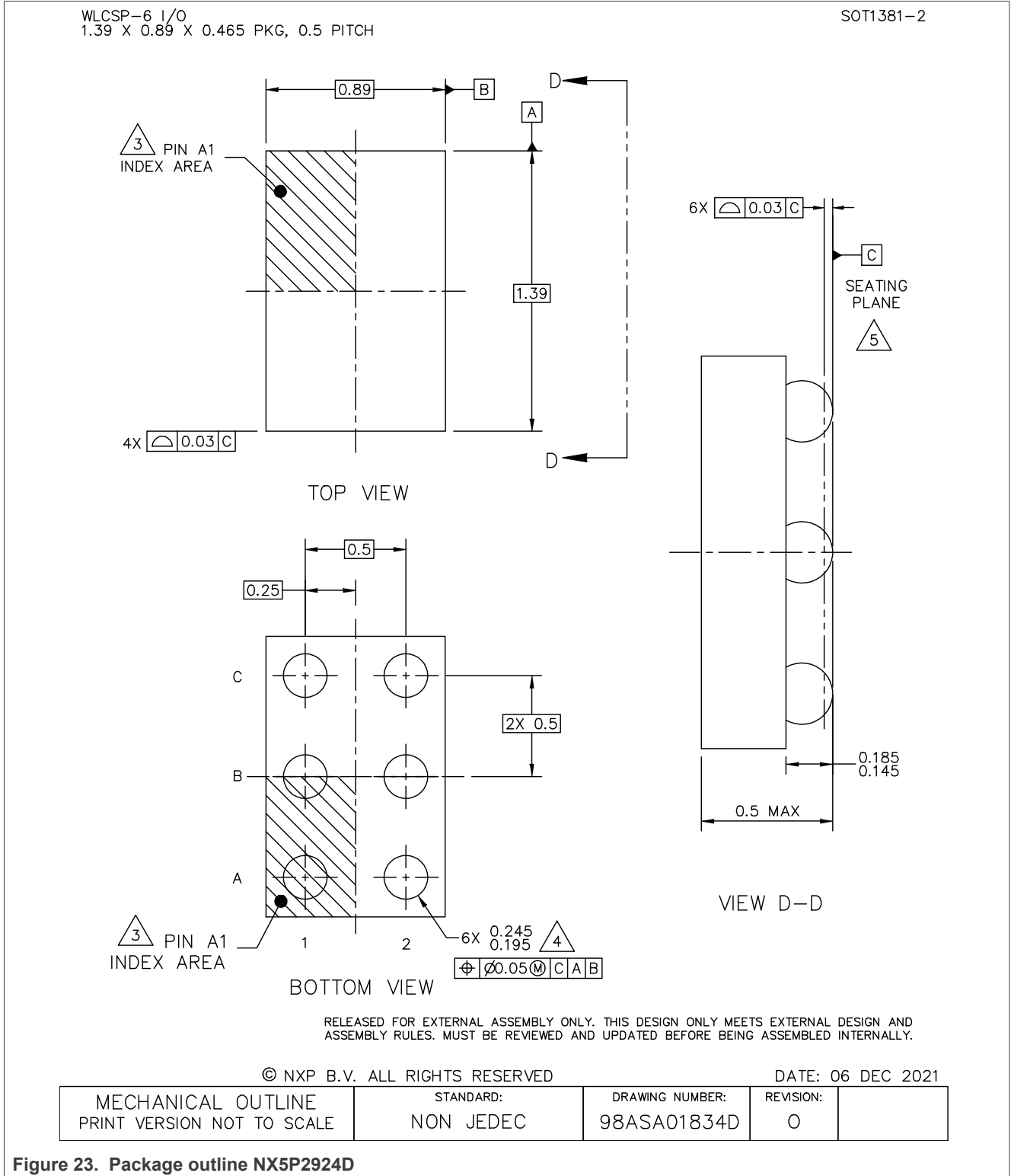


Figure 23. Package outline NX5P2924D

15 Soldering

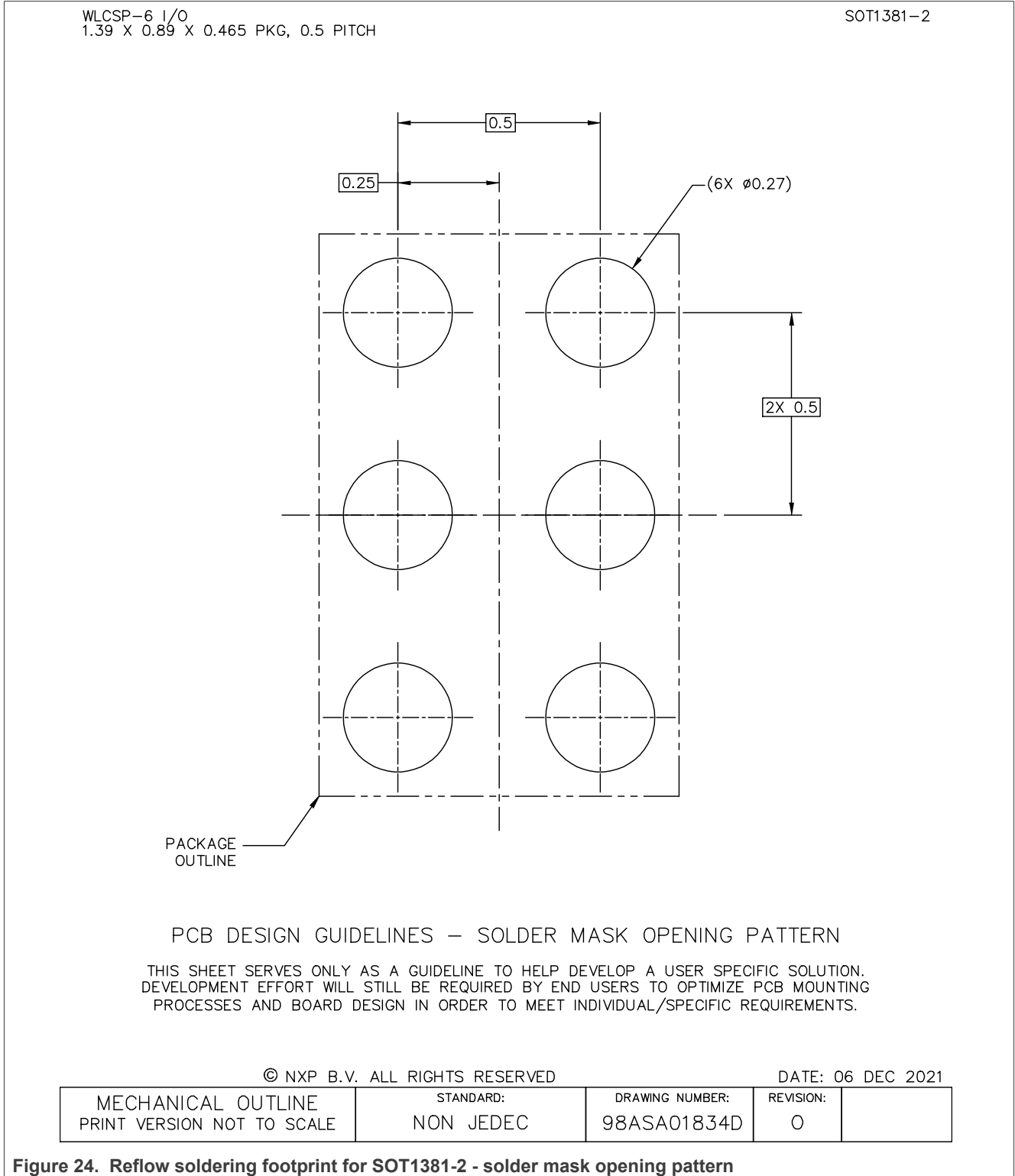
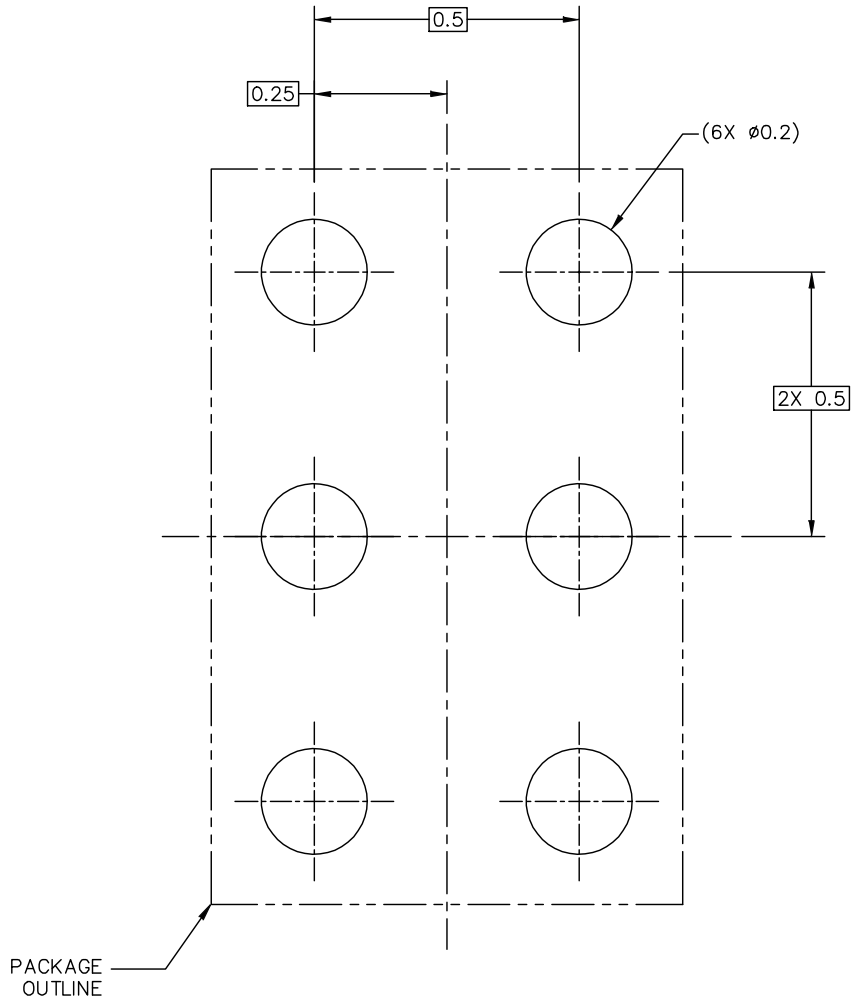


Figure 24. Reflow soldering footprint for SOT1381-2 - solder mask opening pattern

WLCSP-6 I/O
1.39 X 0.89 X 0.465 PKG, 0.5 PITCH

SOT1381-2



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 06 DEC 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01834D	REVISION: 0	
--	------------------------	--------------------------------	----------------	--

Figure 25. Reflow soldering footprint for SOT1381-2 - I/O pads and solderable area

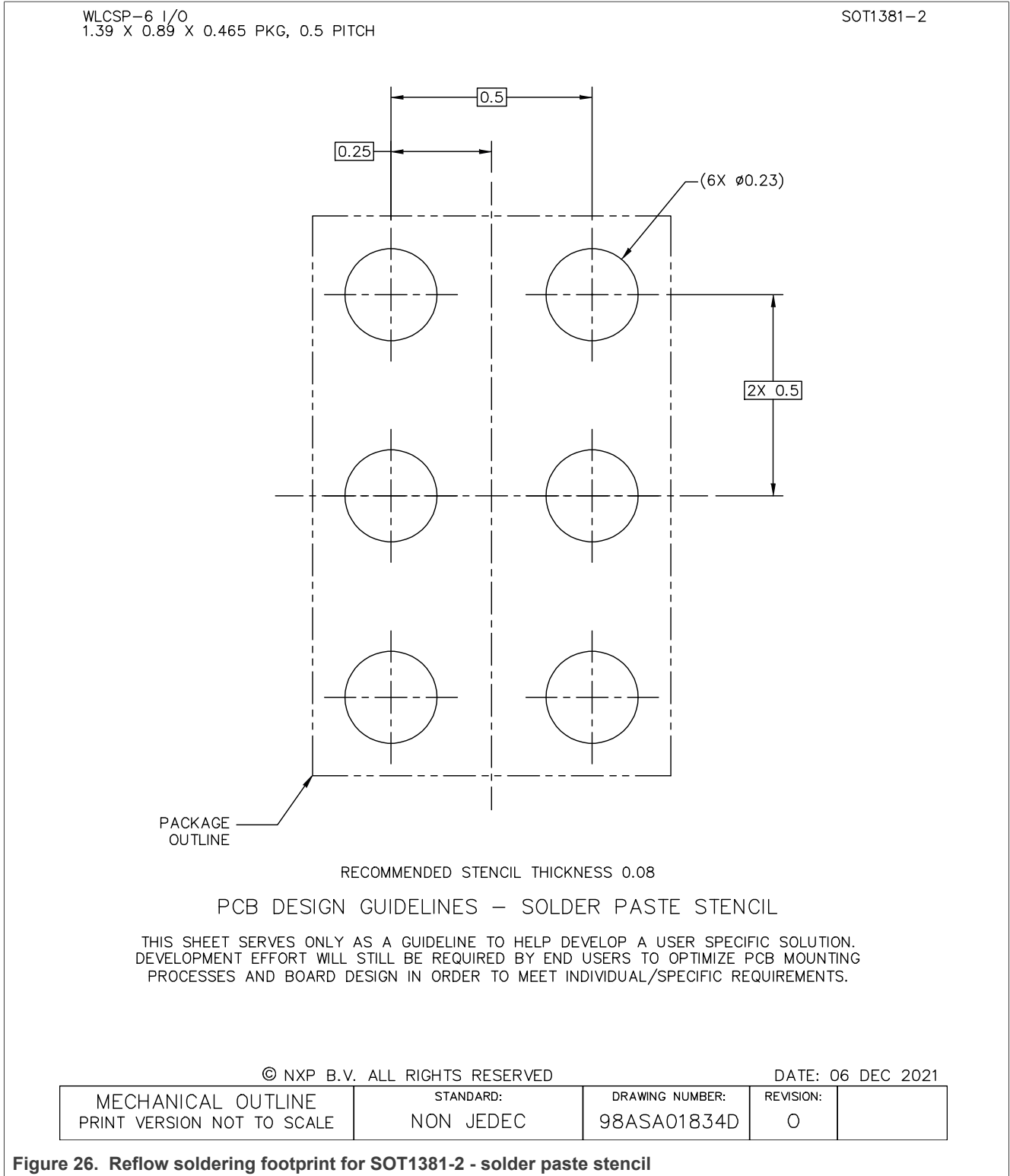


Figure 26. Reflow soldering footprint for SOT1381-2 - solder paste stencil

WLCSP-6 I/O
1.39 X 0.89 X 0.465 PKG, 0.5 PITCH

SOT1381-2

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 06 DEC 2021

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01834D	REVISION: 0	
--	------------------------	--------------------------------	----------------	--

Figure 27. Reflow soldering footprint for SOT1381-2 - notes

16 Soldering of WLCSP packages

16.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 “Wafer Level Chip Scale Package”* and in application note *AN10365 “Surface mount reflow soldering description”*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

16.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

16.3 Reflow soldering

Key characteristics in reflow soldering are:

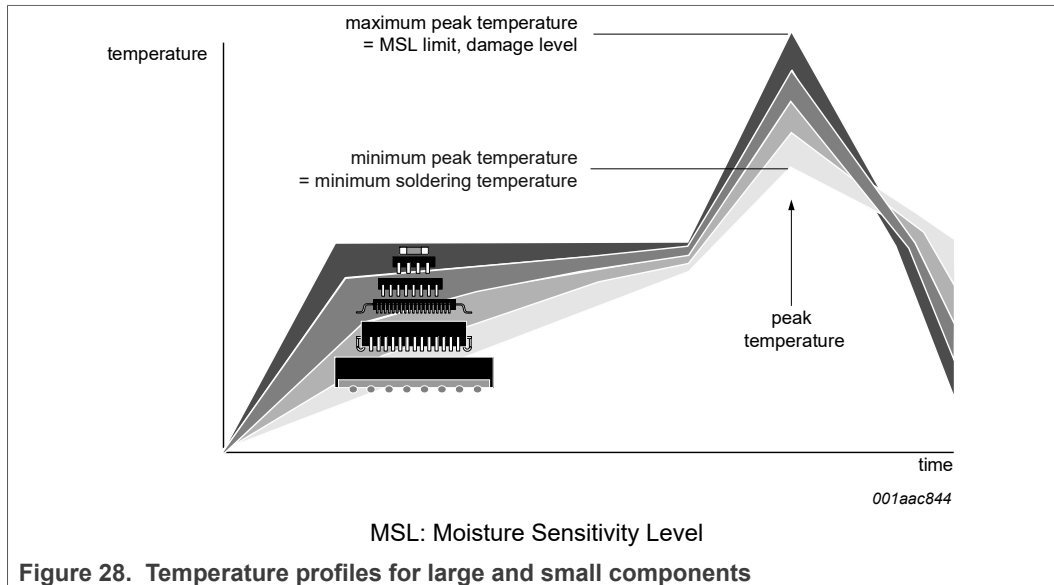
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 28](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 13](#).

Table 13. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2 000	> 2 000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 28](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

16.4 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

16.5 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

16.6 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again. Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and

all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

16.7 Cleaning

Cleaning can be done after reflow soldering.

17 Abbreviations

Table 14. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
IEC	International Electrotechnical Commission
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor

18 Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX5P2924D v.1.0	20220621	Product data sheet	-	-

19 Legal information

19.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

19.2 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

19.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

19.4 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Tab. 1.	Ordering information	1	Tab. 9.	ON resistance	7
Tab. 2.	Ordering options	2	Tab. 10.	Dynamic characteristics	8
Tab. 3.	Pin description	3	Tab. 11.	Measurement points	9
Tab. 4.	Function table	3	Tab. 12.	Test data	10
Tab. 5.	Limiting values	3	Tab. 13.	Lead-free process (from J-STD-020D)	17
Tab. 6.	Recommended operating conditions	4	Tab. 14.	Abbreviations	19
Tab. 7.	Thermal characteristics	4	Tab. 15.	Revision history	19
Tab. 8.	Static characteristics	4			

Figures

Fig. 1.	Logic symbol	2	Fig. 18.	Typical enable time at $V_I(VIN) = 3.6\text{ V}$; $CL = 0.1\ \mu\text{F}$	10
Fig. 2.	Logic diagram	2	Fig. 19.	Typical enable time at $V_I(VIN) = 5.5\text{ V}$; $CL = 0.1\ \mu\text{F}$	11
Fig. 3.	Pin configuration for WLCSP6	2	Fig. 20.	Typical disable time	11
Fig. 4.	Ball mapping for WLCSP6	2	Fig. 21.	Typical enable time at $V_I(VIN) = 3.6\text{ V}$; $CL = 20\ \mu\text{F}$	11
Fig. 5.	NX5P2924D application diagram	3	Fig. 22.	Typical disable time at $V_I(VIN) = 3.6\text{ V}$; $CL = 20\ \mu\text{F}$	11
Fig. 6.	Typical supply current versus temperature	6	Fig. 23.	Package outline NX5P2924D	12
Fig. 7.	Typical supply current versus input voltage on pin VIN	6	Fig. 24.	Reflow soldering footprint for SOT1381-2 - solder mask opening pattern	13
Fig. 8.	Typical supply current versus temperature	6	Fig. 25.	Reflow soldering footprint for SOT1381-2 - I/O pads and solderable area	14
Fig. 9.	Typical supply current versus input voltage on pin VIN	6	Fig. 26.	Reflow soldering footprint for SOT1381-2 - solder paste stencil	15
Fig. 10.	Typical OFF-state leakage current versus temperature	7	Fig. 27.	Reflow soldering footprint for SOT1381-2 - notes	16
Fig. 11.	Typical OFF-state leakage current versus input voltage on pin VIN	7	Fig. 28.	Temperature profiles for large and small components	18
Fig. 12.	Test circuit for measuring ON resistance	7			
Fig. 13.	ON resistance versus temperature	8			
Fig. 14.	ON resistance versus input voltage	8			
Fig. 15.	Switching times	9			
Fig. 16.	Test circuit for measuring switching times	10			
Fig. 17.	Typical enable time at $V_I(VIN) = 1\text{ V}$; $CL = 0.1\ \mu\text{F}$	10			

Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Ordering information	1
4.1	Ordering options	2
5	Functional diagram	2
6	Pinning information	2
6.1	Pinning	2
6.2	Pin description	3
7	Functional description	3
8	Application diagram	3
9	Limiting values	3
10	Recommended operating conditions	4
11	Thermal characteristics	4
12	Static characteristics	4
12.1	Graphs	6
12.2	ON resistance	7
12.3	ON resistance test circuit and graphs	7
13	Dynamic characteristics	8
13.1	Waveforms, graphs and test circuit	9
14	Package outline	12
15	Soldering	13
16	Soldering of WLCSP packages	17
16.1	Introduction to soldering WLCSP packages	17
16.2	Board mounting	17
16.3	Reflow soldering	17
16.4	Stand off	18
16.5	Quality of solder joint	18
16.6	Rework	18
16.7	Cleaning	19
17	Abbreviations	19
18	Revision history	19
19	Legal information	20

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.