NXP Semiconductors
Engineering Bulletin

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i.MX 8M Quad/Dual - Mask Set 1N14W to 2N14W Migration Guide

Contents

1. Introduction

This document provides information on the changes in the i.MX 8M Application Processor between mask set **1N14W** to **2N14W**.

- The part number suffix identifies the silicon revision mask set.
- Part number suffix **A** refers to mask set **1N14W**, and **B** refers to mask set **2N14W**.
- For example, the Part Number *MIMX8MQ5CVAHZAA* is updated to *MIMX8MQ5CVAHZAB* to reflect the **2N14W** mask set.

2. Changes between mask set 1N14W and 2N14W

Table 1 lists the errata fixes between mask set **1N14W** and **2N14W**.

Table 1. Errata fixes between mask set 1N14W and 2N14W

Fixed errata from mask 1N14W	Description	Software migration impact	Hardware migration impact
E11327	DDR PHY: LPDDR4 may fail when switching from PHY PLL bypass mode to PHY PLL Mission mode.	The workarounds documented in the errata are not required for mask set **2N14W**. Software patch is required to support PHY PLL bypass mode for mask set **2N14W**. The change is helpful to reduce power consumption in idle and audio use case on **2N14W**.	None
E11405	DCSS: Scaler output FIFO underrun interrupt failed to generate.	None	None
E11406	DCSS: Dolby Graphics Core input component connection is incorrect.	The workarounds documented in the errata are not required for mask set **2N14W**.	None
E11418	MIPI DSI: Incorrect CRC and payload corruption reported with DCS long write command.	The workarounds documented in the errata are not required for mask set **2N14W**. Customer's software implementing workaround may need to be updated.	None

Table 2 lists ROM improvements between mask set **1N14W** and **2N14W**.

Table 2. ROM improvement between mask set 1N14W and 2N14W

Number	Description	Software migration impact	Hardware migration impact
1	Fixed: The Boot authentication failure for NAND boot when HDMI functionality is required.	None	None
2	Fixed: The MFG mode failure when fast boot to eMMC fails and then drops into MFG mode.	None	None
3	Improved: The Serial Download Mode (SDP) allows SDP to restart itself without running SPL again.	None	None
4	Fixed: The Field Return fuse that enables the chip to run test code on the returned and locked parts.	None	None

Table 3 lists part number changes between mask set **1N14W** and **2N14W**. The mask set and part number can be identified in the part marking.

Table 3. Part number changes

Mask set 1N14W part number (suffix A)	Mask set 2N14W part number (suffix B)
MIMX8MQ5CVAHZAA	MIMX8MQ5CVAHZAB
MIMX8MQ5DVAJZAA	MIMX8MQ5DVAJZAB
MIMX8MQ6CVAHZAA	MIMX8MQ6CVAHZAB
MIMX8MQ6DVAJZAA	MIMX8MQ6DVAJZAB
MIMX8MD6CVAHZAA	MIMX8MD6CVAHZAB
MIMX8MD6DVAJZAA	MIMX8MD6DVAJZAB
MIMX8MQ7CVAHZAA	MIMX8MQ7CVAHZAB
MIMX8MQ7DVAJZAA	MIMX8MQ7DVAJZAB
MIMX8MD7CVAHZAA	MIMX8MD7CVAHZAB
MIMX8MD7DVAJZAA	MIMX8MD7DVAJZAB

Table 4 lists silicon revision changes between mask set **1N14W** and **2N14W**.

Table 4. Silicon revision changes between mask set 1N14W and 2N14W

Mask set	Silicon version register address	Value	Software migration impact	Hardware migration impact
1N14W	None	Not applicable	None	None
2N14W	0x30350040	0xFF0055AA	The software that requires silicon revision confirmation, may require update.	None

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