Freescale Semiconductor
Engineering Bulletin

DSP56300 Power-Up Sequencing Guidelines

This document provides guidelines for applying power and signals to certain DSP56300 family devices using split power supplies with different core/PLL and I/O voltage requirements, that is, the DSP56307, DSP56L307, and DSP56311. For specification details, refer to the device Technical Data sheet.

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1 Device Initialization Steps

To ensure proper operation of the device and minimize power consumption during start-up:

1. *Power-up Sequence.* Ensure that the I/O voltage source is always higher than or equal to the core/PLL voltage source.

2. *Input Signal Requirements.*

    a. $\overline{RESET}$ and $\overline{TRST}$ must be asserted during power-up and held low (asserted) until the proper conditions are met.

    b. The input clock must be applied and stabilized before $\overline{RESET}$ is deasserted (pulled high).

    c. Ensure that the PLL Initial pin (PINIT) is pulled up or down, as appropriate, to determine whether PLL is enabled or disabled before deasserting $\overline{RESET}$.

    d. Ensure that the mode pins (MOD[A–D]) are pulled up or down, as appropriate, to select the desired boot mode before deasserting $\overline{RESET}$.

    e. All inputs must be terminated (that is, not allowed to float) by CMOS levels except for the five pins with internal pull-up resistors (TMS, TDI, TCK, $\overline{TRST}$ and $\overline{DE}$).

    f. The duration of the required $\overline{RESET}$ assertion depends on the clock source:

    • For an external clock generator, the minimum $\overline{RESET}$ duration is measured while $\overline{RESET}$ is asserted, V_{CC} is valid, and the EXTAL input is active and valid.

    • For an internal oscillator, the minimum $\overline{RESET}$ duration is measured while $\overline{RESET}$ is asserted and V_{CC} is valid. Specified timing reflects the crystal oscillator stabilization time after power-up. Both the crystal specifications and those for other components connected to the oscillator affect this number, and it reflects worst case conditions.

    • When the V_{CC} is valid, but the other "required RESET duration" conditions (as specified above) are not yet met, the device circuitry is in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.

    g. Deassert $\overline{TRST}$ with or after $\overline{RESET}$.

Note: Failure to comply with any of these requirements may cause high current consumption during or after power-up or prevent the correct device initialization.

2 Board Design Recommendations

• Provide a low-impedance path from the board power supply to each V_{CC} pin on the DSP and from the board ground to each GND pin.

• Use at least a four-layer PCB with two inner layers for V_{CC} and GND.

• Use at least six 0.01–0.1 µF bypass capacitors for I/O V_{CC} and four 0.01–0.1 µF capacitors for core V_{CC}, positioned as closely as possible to the four sides of the package to connect the V_{CC} power sources to GND.

• Ensure that capacitor leads and associated printed circuit traces that connect to the chip V_{CC} and GND pins are less than 0.5 inch per capacitor lead.

• Maximum PCB trace lengths on the order of 4 inches are recommended to the address and data buses as well as the $\overline{IRQA}$, $\overline{IRQB}$, $\overline{IRQC}$, $\overline{IRQD}$, $\overline{TA}$, and $\overline{BG}$ pins.

• If multiple DSP devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.

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3 Other Considerations

- Consider all device loads as well as parasitic capacitance due to PCB traces when you calculate capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{CC} and GND circuits.

- The Port A data bus (D[0–23]), HI08, ESSI0, ESSI1, SCI, and timers all use internal keepers to maintain the last output value even when the internal signal is tri-stated. Typically, no pull-up or pull-down resistors should be used with these signal lines. However, if the DSP is connected to a device that requires pull-up resistors (such as an MPC8260), the recommended resistor value is 10 KΩ or less. If more than one DSP must be connected in parallel to the other device, the pull-up resistor value requirement changes as follows:

  — 2 DSPs = 7 KΩ or less
  — 3 DSPs = 4 KΩ or less
  — 4 DSPs = 3 KΩ or less
  — 5 DSPs = 2 KΩ or less
  — 6 DSPs = 1.5 KΩ or less

4 Reference Documentation

- *DSP56307 Technical Data sheet* (DSP56307)

- *DSP56L307 Technical Data* sheet (DSP56L307)

- *DSP56311 Technical Data* sheet (DSP56311)

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