

# Minimum/Maximum ESR Requirement for i.MX 6Dual/6Quad Analog Regulators

## 1 Introduction

Having inadequate Equivalent Series Resistance (ESR), which is essentially a measure of the total lossiness of a capacitor, can cause regulation instabilities and ripples on the output of the Analog LDO.

This document describes the required minimum and recommended maximum ESR values for the external decoupling/filtering circuits associated with the analog LDO outputs on the i.MX 6Dual/6Quad SoCs.

## 2 Minimum ESR Requirement for Analog Regulators

The analog regulators on the i.MX 6Dual/6Quad SoCs require external bulk capacitors to provide stable regulation and minimize output voltage ripple. Some customer designs have exhibited unusually high saw tooth voltage ripple on the LDO\_2P5 regulator. The root cause for this behavior was low equivalent series resistance (ESR) of the external circuit on the regulator.

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Design simulations combined with actual circuit measurements over worse-case silicon process and temperature conditions have yielded the following minimum ESR requirements for each of the analog regulators on the SoC. The ESR values below represent the required ESR for the entire external circuit (combined trace resistance, component resistance, and the external bulk capacitor ESR) seen by the regulator output.

**Table 1. Minimum ESR requirements for i.MX 6Dual/6Quad analog regulators**

Analog Regulator	LDO Regulator Output	Min External ESR	Comments
LDO_1P1	NVCC_PLL_OUT	—	One 10 uF capacitor connected to the regulator output This regulator has no minimum ESR requirement.
LDO_2P5	VDD_HIGH_CAP	85 mΩ	One 10 uF capacitor connected to the regulator output (assumed worst case value for a 10uF capacitor is 4.7 uF)
SNVS	VDD_SNVS_CAP	—	One 0.22 uF capacitor connected to the regulator output This regulator has no minimum ESR requirement.
USB	VDD_USB_CAP	—	One 10 uF capacitor connected to the regulator output This regulator has no minimum ESR requirement.

**Note:** Values based on maximum 5 mv ripple oscillation on the LDO output

**Note:** 1 mA LDO load assumed over worse case silicon process and temperature

**Note:** The *Cext* of 4.7uF is based on the worst case derated value of a typical 10uF ceramic capacitor

**Note:** The values shown in the above table are specific to the 21 x 21 mm FC-PBGA package for the i.MX 6Dual/6Quad and not directly applicable to other processor and package combinations in the i.MX 6 series

**Note:** For a typical silicon process, room temperature, larger capacitor and regulator load then the design simulations predict that the we need less ESR to maintain stability

## 2.1 Component Selection and Placement

The minimum ESR requirement for the LDO\_2P5 regulator can be achieved by using a 91mΩ 5% tolerance resistor in series with the external bulk capacitor, or by choosing a bulk capacitor that will always have at least 85 mΩ ESR. Using a 100 mΩ or 110 mΩ standard resistor value is also acceptable.

The board trace resistance can be subtracted from the minimum requirement above. Any additional resistors being added to meet the ESR requirement must be in series with the bulk capacitor between output of the regulator and the main bulk cap as shown in [Figure 1](#). The advantage of the implementation shown in [Figure 1](#) will be marginally less noise on the PCIe or other loads on this supply rail. Another acceptable configuration is shown in [Figure 2](#). Please note that all of the other connections in these figures have

parasitic resistances that are not shown. In general the goal should be to minimize the inductance and resistance in the connection to the bulk capacitor ( $C_{Bulk}$ ).

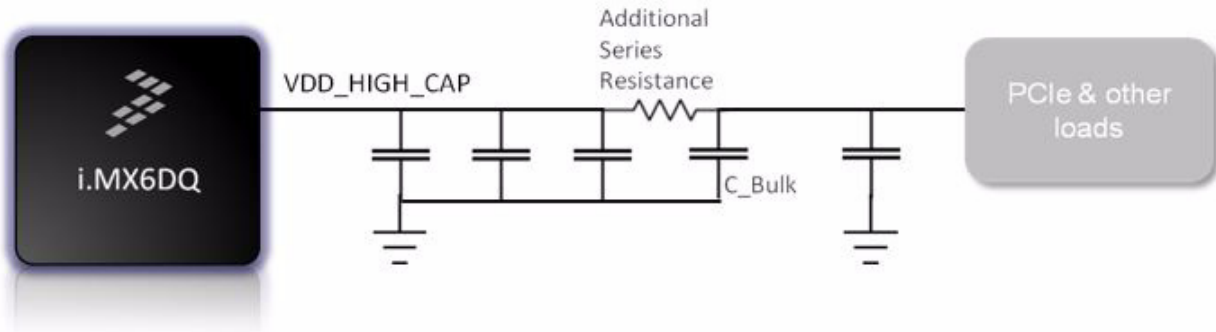


Figure 1. Additional resistor placement — option 1

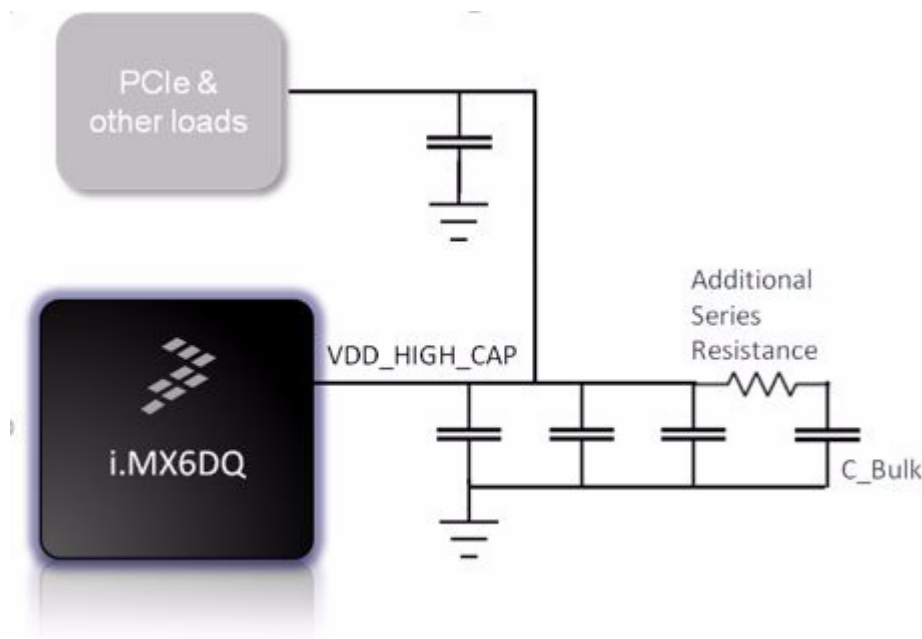


Figure 2. Additional resistor placement — option 2

A 0 ohm fail safe resistor can be placed in customer designs to accommodate varying board trace resistance. A staggering approach should be used to place the various sized decoupling capacitors, whereas the larger sized bulk capacitors are further out and the smaller high frequency decoupling capacitors (0.22 uF) are closest to the SoC power balls as possible during layout. For more details on decoupling and layout considerations, see the *Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors* (IMX6DQ6SDLHDG), available on [www.freescale.com](http://www.freescale.com).

### 3 Maximum ESR Recommendations for Analog Regulators

For maximum ESR values, slightly larger series resistance values can be used, however it is recommended not to go too high, as this will make the effective bulk capacitance ( $C_{Bulk}$ ) smaller than required. In addition, using a larger series resistance may not be practical for load regulation, as there comes a point where the load current transients will translate to voltage ripple. The aim is to stay within the specified requirement for ripple noise of less than 5%  $V_{p-p}$  of the supply voltage average value.

The maximum ESR is a more a function of the maximum load for which the LDO was designed than the maximum load in the application. The noise due to load transients depends on various factors including the resistor placement and external loads versus internal loads of the LDO.

For example: 300mA pulses into 200  $m\Omega$  of series resistance = 60mV of ripple noise on the LDO output.

As the additional series resistance increases so does the effective ripple on the output increase. This will hence limit the maximum series resistance that can be added before the ESR requirements to stabilize the regulator output.

Freescale recommends that the maximum ESR value be minimized for high frequency load regulation and decoupling; a value close to the minimum ESR requirements detailed in [Table 1](#) is ideal.

## 4 Revision history

Table 2 summarizes changes to this document since the release of the previous revision.

**Table 2. Revision history**

Revision	Change description
0	Initial release.

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