MPC5121e Functional Differences
2M34K and M36P
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There are 3 major categories of the changes being made between the two mask sets, or revisions for the MPC5121e. These categories are 1) Feature enhancements, 2) System Enhancements, and 3) Bug fixes and maintaining pin compatibility between the 2 revisions.

Additional details on each of these changes can be found in the MPC5121eRM Reference Manual, found on the MPC5121 Product Documentation Page (http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MPC5121e&nodeId=0162468rH3DgbNGrmC22FA&fpsp=1&tab=Documentation_Tab .

Feature Enhancements

Video Input

This feature is adding ITU 656 video input capability on the MPC5121e. This input has been added as an addition to the PCI and PSC pin multiplexing.

NAND Flash Controller

The NAND flash controller has been changed out to a more robust module. The interface pins have not been modified. The M36P will support MLC as well as SLC NAND type of memories.

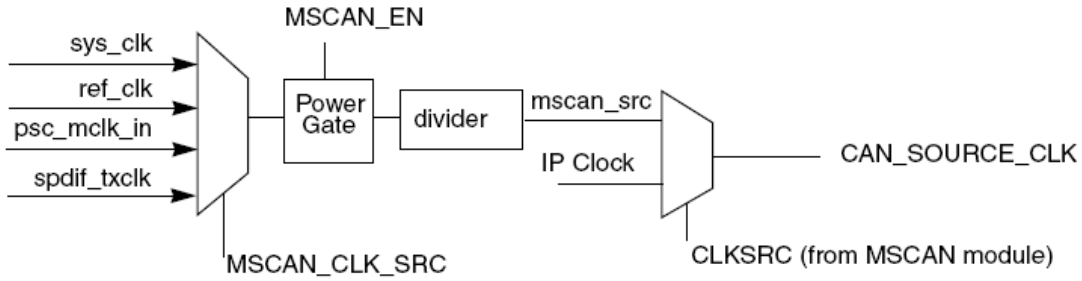
CAN Module

There are two additional CAN channels available on the new chip. These are labeled CAN 3 and 4.

System Enhancements

Can Clocking

The CAN clocking has been changed to enable greater granularity of the clock generation in support of additional CAN frequencies. The clock tree for the CAN has been implemented as follows:



SDHC Clock Source

The SDHC clock source and dividers have changed to allow for optimum performance at multiple system clock speeds.

The clock source was moved from the IP bus clock to the System bus clock. To allow for a faster clock source, additional dividers were also added.

PSC Clock MCLK_DIV

The PSC MCLK_DIV has added a feature of a divide by 1, or pass through. The diagram below shows the “mclk_div” in the clock tree.

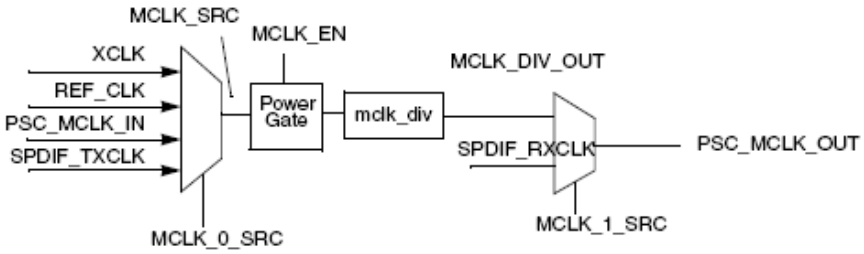


Figure 6-4. PSC (MCLK) Clock Generation[1]

Local Plus Bus

Burst Modes

The local plus has been enhanced to provide burst mode for all clock ratios and bit widths.

ALE/CS Timing

The Address Latch Enable (ALE) and Chip Select (CS) timing has been added in support of StrataFlash timings. For timing diagrams, please see the MPC5121eDS.

Watchdog Timer

The watchdog timer will derive its clock from the input crystal. The current method, the clock source is from the IP clock.

DIU

The DIU buffer output size has been increased to 512 bytes.

SPDIF

The SPDIF FIFO has been increased to 12 samples from 10.

JTAG and POR

Internal pull-ups have been added to these pins.

DRAM Priority Manager

The reset values for the DRAM Priority Manager have been changed. These changes will allow for a level of system functionality from a reset state.

Errata Fixes

The following errata have been fixed.

Module	ID	Title	Fixed M36P
PCI	30	Section 2.1, “STOP Assertion by Target Device on Last Beat of PCI Memory Write Transaction Can Cause a Hang”	
	71	Section 2.2, “Data Corruption by PCI_DMA When Using Destination Address Hold (DAHE)”	
	226	Section 2.3, “Violation of PCI Tsu Minimum Time (I/O Timing)”	**X**
	257	Section 2.4, “PCI Controller Hangs When Returning from PCI Pins Low Status”	
	281	Section 2.5, “CSB:PCI Clock Ratio of 4:1 not Supported”	**X**
	282	Section 2.6, “Interrupt Disable Bit is not Implemented as Defined by PCI 2.3”	**X**
	302	Section 2.7, “CSB Deadlock on Core Data and Instruction Reads”	**X**
	344	Section 2.8, “Four Registers of the PCI IOS Module are Not Accessible	**X**
USB	42	Section 3.1, “Read of PERIODICLISTBASE After Successive Writes May Return Wrong Data”	
	273	Section 3.2, “USB PHY – DP is in Pull-Up Mode After Reset”	**X**
	286	Section 3.4, “USB Registers Use Little-Endian Byte Ordering”	**X**
	325	Section 3.3, “USB Can Possibly Lock the AMBA Master Bus”	**X**
		USB Data Corruption	**X**
DIU	203	Section 4.1, “Malfunction if There is On to Off and/or Off to On Switch on a Plane”	**X**

Module	ID	Title	Fixed M36P
	211	Section 4.2, “BGND, BGND_WB, CURSOR_X/Y, and COLBAR_* Registers Must be Reprogrammed at Proper Time”	X
	230	Section 4.3, “Loss of Area Descriptor Data When There are Three or More AOIs in a Plane”	X
	232	Section 4.4, “One Pixel is Wrong When Back-to-Back AOIs are Used in a Plane Switching from Palette to Non-Palette Mode””	X
	253	Section 4.5, “Writeback Issue in Mode 2 Because of Late Assertion of Write Buffer Empty”	X
	285	Section 4.6, “Mode 2 Palette Mode Bug When More Than One Plane Uses Palette Mode”	X
	317	Section 4.7, “Unexpected IRQ Clean if INT Event Occurs When INT_STATUS Register is Read”	X
DMA	349	Section 9.1, “DMA Error Status bits SBE and DBE are not Set Properly”	X
PSC	298	Section 5.1, “TX Channel Switch is Possible if TX FIFO Goes Empty During Transmission”	X
	330	Section 5.3, “Under run Interrupt Doesn't Work in AC97 Mode”	X
	335	Section 5.2, “PSC Multi-Channel Mode with 2RX Lines Enabled Doesn't Work”	X
	348	Section 5.4, “SPI EOF Mode Doesn't Work Properly”	X
AXE	295	Section 6.1, “CMPF Instruction Flag Wrong”	X
LPC	288	Section 7.1, “No Concurrent Access Between e300 and DMA at Certain Clock Ratios and BPTs”	X
RTC	332	Section 8.1, “RTC is not Functional Over Specified Voltage Range”	X
	345	Section 8.2, “RTC MPE Bit in RTC Alarm and Interrupt Enable Register not Functioning Correctly”	X
SCLPC FIFO	311	Section 10.1, “SCLPC FIFO Over/Underflow Error Occur”	X
CLOCK	274	Section 11.1, “Core PLL Configuration Changes Back to Reset Configuration When Wake-Up from Deep Sleep Mode	X
PMC	308	Section 12.1, “PMC Should Support CCM During DSM”	X
	322	Section 12.2, “Multi-Time Core PLL Configuration Changing is not Supported”	X
	324	Section 12.4, “PMC Needs More Wait Cycles to Relock CORE-PLL During PRE-DIV Copy Mode”	X
	334	Section 12.3, “Arb_xlbidle When PMC is Waiting Core PLL Relock Leads to Wrong State”	X
PRIO_ MNGR	314	Section 13.1, “Register Permon_Config Can Only be Written with 4 Byte Length”	X
SATA	337	Section 14.1, “SATA Module is Non-functional”	X

Please see the Errata List for complete details of each errata.

Software Compatibility Summary

This section outlines the software changes required on 2M34K drivers to enable them to work on M36P. For the added features, new drivers need to be developed and will not be contained in this section.

Module	Description
MSCAN	The MSCAN clocking has changed and requires additional programming. Refer to chapter 5, Clocks and Low Power Modes. The driver must be modified to match the new configurations.
NAND	This module has added additional capabilities. This requires additional programming. The driver must be changed to match these changes.
SDHC	Due to the clocking changes, this drive must also be modified.
USB	Based on the Errata fix # 286, the configuration registers have been changed to Big Endian. The driver must be changed to match.

Revision History

Date	Changes
25 January 2008	Original Release
30 January 2008	Changed mask reference number from M34P to M36P. DIU and SPDIF section – grammar has been cleaned up.
8 February 2008	Add SDHC to list of changes, added “USB Data Corruption”, and PSC MCLK DIV.
28 July 2008	Add SDHC Clock Changes, add software compatibility summary.
10 December 2008	Changed references to mask set numbers from tape out 1 and tape out 2.