Mask Set Errata for Mask 2N27B

Introduction

This report applies to mask 2N27B for these products:

- COLDFIREPLUS

Errata ID	Errata Title
3863	ADC: In 16-bit differential mode, ADC may result in a conversion error when positive input is near upper rail reference voltage
2793	I2C: MCU does not wake as expected from STOP or VLPS mode on subsequent address matches if previous address is mismatched
4590	MCG: Transitioning from VLPS to VLPR low power modes while in BLPI clock mode is not supported.
6665	Operating requirements: Limitation of the device operating range
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2582	UART: Flow control timing issue can result in loss of characters
4945	UART: ISO-7816 T=1 mode receive data format with a single stop bit is not supported
3892	UART: ISO-7816 automatic initial character detect feature not working correctly
3516	[PLL] If stop mode is entered with the PLL enabled and BDM active (debugger connected), the LOCK bit is incorrectly cleared when stop mode is exited.
3517	[PLL] Setting PLLS immediately after clearing PLLCLKEN will cause the LOCK bit to clear and stay cleared even after the PLL has re-started.

e3863: ADC: In 16-bit differential mode, ADC may result in a conversion error when positive input is near upper rail reference voltage

Errata type: Errata

Description: In 16-bit differential mode, the ADC may result in a conversion error when the input voltage on the plus-side of the differential pair (DPx) exceeds approximately (VREFH*31/32). Other modes are unaffected.

Workaround: To avoid a conversion error near positive full-scale in this mode, do not allow the input voltage on the plus-side of the differential pair (DPx) to exceed (VREFH*31/32).

e2793: I2C: MCU does not wake as expected from STOP or VLPS mode on subsequent address matches if previous address is mismatched

Errata type: Errata

Description: The I2C module, acting as a slave on the I2C bus, does not wake as expected from normal STOP mode or VLPS mode on a valid address match if the previous address was not a match.

When the external I2C master sends a non-matching address, the I2C slave state machine does not look for a start bit past the first start bit on the bus. Consequently, subsequent transmissions by the I2C master with a matching address do not, on the first matching address, wake the MCU from stop mode or VLPS via the I2C interrupt.

Workaround: There are multiple workarounds:

(1) The master must continually re-transmit the MCU's slave address upon not receiving a NACK from the slave device during the slave addressing phase of the transmission. For clarification, the master must perform the following:

a) Send slave device address

b) Check for ACK bit

c) If ACK was received, continue with data transmission. Else, send repeated start signal and repeat steps a-c.

NOTE: Due to the nature of the errata, the maximum number of retransmissions needed to wake the part is nine times.

(2) When the MCU, operating as an I2C slave, is in STOP or VLPS mode: Ensure that the external I2C master sends a matching address to wake the slave MCU before it sends any transaction to other I2C slaves. The user must also ensure that MCU does not return to STOP or VLPS until after all packets to non-matching addresses have been sent.

(3) Use a pin interrupt (any pin, whether that pin is or is not being used by the active I2C module) to wake up the part before receiving I2C packets. NOTE: If using the SDA or SCL pin that the active I2C module is using, the part will wake-up on every I2C transaction on the bus.

(4) Use Wait mode instead of STOP or VLPS mode.

e4590: MCG: Transitioning from VLPS to VLPR low power modes while in BLPI clock mode is not supported.

Errata type: Errata

Description: Transitioning from VLPS mode back to VLPR (LPWUI control bit = 0) while using BLPI clock mode only, is not supported. During Fast IRC startup, the output clock frequency may exceed the maximum VLPR operating frequency. This does not apply to the BLPE clock mode.

Workaround: There are two options for workarounds

a) Exit to Run instead of VLPR. Before entering VLPR set the LPWUI bit so that when exiting VLPS mode the MCU exits to RUN mode instead of VLPR mode. With LPWUI set any interrupt will exit VLPR or VLPS back into RUN mode. To minimize the impact of the higher RUN current re-enter VLPR quickly.

or

b) Utilize MCG clock mode BLPE when transitioning from VLPS to VLPR modes.

e6665: Operating requirements: Limitation of the device operating range

Errata type: Errata

Description: Some devices, when power is applied, may not consistently begin to execute code under certain voltage and temperature conditions. Applications that power up with either VDD >= 2.0 V or temperature >= -20C are not impacted. Entry and exit of low-power modes is not impacted.

Workaround: To avoid this unwanted behavior, one or both of these conditions must be met:

a) Perform power on reset of the device with a supply voltage (VDD) equal-to or greater-than 2.0 V , or

b) Perform power on reset of the device at a temperature at or above -20 C.

e4482: PMC: STOP mode recovery unstable

Errata type: Errata

Description: Recovery from STOP mode is not guaranteed if STOP mode is used for a period of time longer than 50ms.

Workaround: There are two methods that can be used:

1. Use a different low power mode such as VLPS.

2. Periodically exit STOP mode every 50ms and wait 16us before entering STOP mode again.

e4949: Reset and Boot: Device may not exit the power on reset (POR) event correctly with fast ramp-up slew rates.

Errata type: Errata

Description: Device may not exit the power on reset (POR) event correctly when the Vdd ramp-up slew rate is greater than 17 kV/sec as VDD is raised from 0V to 1.7V.

Workaround: Keep instantaneous slew rate of VDD below 17 kV/sec.

Status: This errata will be fixed on future mask sets.

e2582: UART: Flow control timing issue can result in loss of characters

Errata type: Errata

Description: When /RTS flow control signal is used in receiver request-to-send mode, the /RTS signal is negated if the number of characters in the Receive FIFO is equal to or greater than the receive watermark. The /RTS signal will not negate until after the last character (the one that makes the condition for /RTS negation true) is completely received and recognized. This creates a delay between the end of the STOP bit and the negation of the /RTS signal. In some cases this delay can be long enough that a transmitter will start transmission of another character before it has a chance to recognize the negation of the /RTS signal (the /CTS input to the transmitter).

Workaround: For UARTs that implement an eight entry FIFO: When the FIFO is enabled, the receive watermark should be set to seven or less. This will ensure that there is space for at least one more character in the FIFO when /RTS negates. So in this case no data would be lost.

For UARTs without a FIFO (or if the FIFO is disabled): Delay might need to be added between characters on the transmit side in order to allow time for the negation of /RTS to be recognized before the next character is sent.

e4945: UART: ISO-7816 T=1 mode receive data format with a single stop bit is not supported

Errata type: Errata

Description: Transmission of ISO-7816 data frames with single stop bit is supported in T=1 mode. Currently in order to receive a frame, two or more stop bits are required. This means that 11 ETU reception based on T=1 protocol is not supported. T=0 protocol is unaffected.

Workaround: Do not send T=1, 11 ETU frames to the UART in ISO-7816 mode. Use 12 ETU transmissions for T=1 protocol instead.

e3892: UART: ISO-7816 automatic initial character detect feature not working correctly

Errata type: Errata

Description: The ISO-7816 automatic initial character detection feature does not work. The direct convention initial character can be detected correctly, but the inverse convention initial character will only be detected if the S2[MSBF] and S2[RXINV] bits are set. This defeats the purpose of the initial character detection and automatic configuration of the S2[MSBF], S2[RXINV], and C3[TXINV] bits.

Workaround: Use software to manually detect initial characters. Configure the UART with S2[MSBF] and S2[RXINV] cleared. Then check UART receive characters looking for 0x3B or 0x03. If 0x3B is received, then the connected card is direct convention. If 0x03 is received, then the connected card is inverse convention. If an inverse convention card is detected, then software should set S2[MSBF], S2[RXINV], and C3[TXINV].

e3516: [PLL] If stop mode is entered with the PLL enabled and BDM active (debugger connected), the LOCK bit is incorrectly cleared when stop mode is exited.

Errata type: Errata

Description: If stop mode is entered with the PLL enabled and BDM active (debugger connected), the LOCK bit is incorrectly cleared when stop mode is exited. This gives a false indication that the PLL has lost lock. The LOCK bit cannot be relied upon to identify if the PLL is truly locked. Once this occurs, if the PLL is then disabled and re-enabled, the LOCK bit will set correctly. In normal operation, BDM not active, the LOCK bit functions correctly.

Workaround: Perform one of the following workaround options.

Workaround Option 1

If entering stop mode with the pll enabled and BDM active (debugger connected), when exiting stop mode do not rely on the LOCK bit being set to verify the PLL is locked. The LOLS flag can be checked to ensure that it is not set to verify that PLL lock has not been lost.

-or-

Workaround Option 2

Disable and re-enable the PLL (by switching to a non-PLL mode or simply clearing PLLCLKEN if in a non-PLL mode). When the PLL is re-enabled the LOCK bit will be set correctly.

-or-

Workaround Option 3

During development, when the debugger is being used, the PLLSTEN bit can be set before entering STOP. This will keep the PLL running in STOP mode, which will also happen if BDM is active when STOP mode is entered. If the PLLSTEN bit is set then the LOCK bit will correctly remain set when STOP mode is exited. For final product production, the PLLSTEN bit should be cleared in order to reduce the power consumption in STOP mode.

e3517: [PLL] Setting PLLS immediately after clearing PLLCLKEN will cause the LOCK bit to clear and stay cleared even after the PLL has re-started.

Errata type: Errata

Description: Setting PLLS immediately after clearing PLLCLKEN will cause the LOCK bit to clear and stay cleared even after the PLL has re-started.

Workaround: Avoid disabling the PLL before immediately re-enabling it. If this cannot be avoided, add a single NOP instruction between clearing the PLLCLKEN bit and setting the PLLS bit.

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