ES_LPC11E6x

Errata sheet LPC11E6x

Rev. 1.2 — 19 January 2024 **Errata**

Document information

Information	Content
Keywords	LPC11E67JBD48; LPC11E68JBD64; LPC11E68JBD100, LPC11E6x errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

1 Product identification

The LPC11E6x devices typically have the following top-side marking for LQFP100 packages:

LPC11E6xJBD100
xxxxxx xx
xxxyywwxR[x]

The LPC11E6x devices typically have the following top-side marking for LQFP64 packages:

LPC11E6xJ
xxxxxx xx
xxxyywwxR[x]

The LPC11E6x devices typically have the following top-side marking for LQFP48 packages:

LPC11E6xJ
xx xx
xxxyy
wwxR[x]

Field ‘yy’ states the year the device was manufactured. Field ‘ww’ states the week the device was manufactured during that year.

Field ‘R’ identifies the device revision. This Errata Sheet covers the following revisions of the LPC11E6x:

Table 1. Device revision table

Revision identifier (R)	Revision description
‘A’	Initial device revision

2 Errata overview

Table 2. Errata summary table

Functional problems	Short description	Revision identifier	Detailed description
UART.1	The UART controller sets the Idle status bits for receive and transmit before the transmission of the stop bit is complete.	‘A’	Section 3.1
ROM.1	On the LPC11E6x, the ROM inadvertently reports IAP busy status for IAP erase and program operations	'A'	Section 3.2

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes table

Errata notes	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

3 Functional problems detail

3.1 UART.1

Introduction:

In receive mode, the UART controller provides a status bit (the RXIDLE bit in the UART STAT register) to check whether the receiver is currently receiving data. If RXIDLE is set, the receiver indicates it is idle and does not receive data.

In transmit mode, the UART controller provides two status bits (TXIDLE and TXDISSTAT bits in the UART STAT register) to indicate whether the transmitter is currently transmitting data. The TXIDLE bit is set by the controller after the last stop bit has been transmitted. The TXDISSTAT bit is set by the controller after the transmitter has sent the last stop bit and has become fully idle following a transmit disable executed by setting the TXDIS bit in the UART CTRL register.

The status bits can be used to implement software flow control, but their setting does not affect normal UART operation.

Problem:

The RXIDLE bit is incorrectly set for a fraction of the clock cycle between the reception of the last data bit and the reception of the start bit of the next word, that is while the stop bit is received. RXIDLE is cleared at the beginning of the start bit.

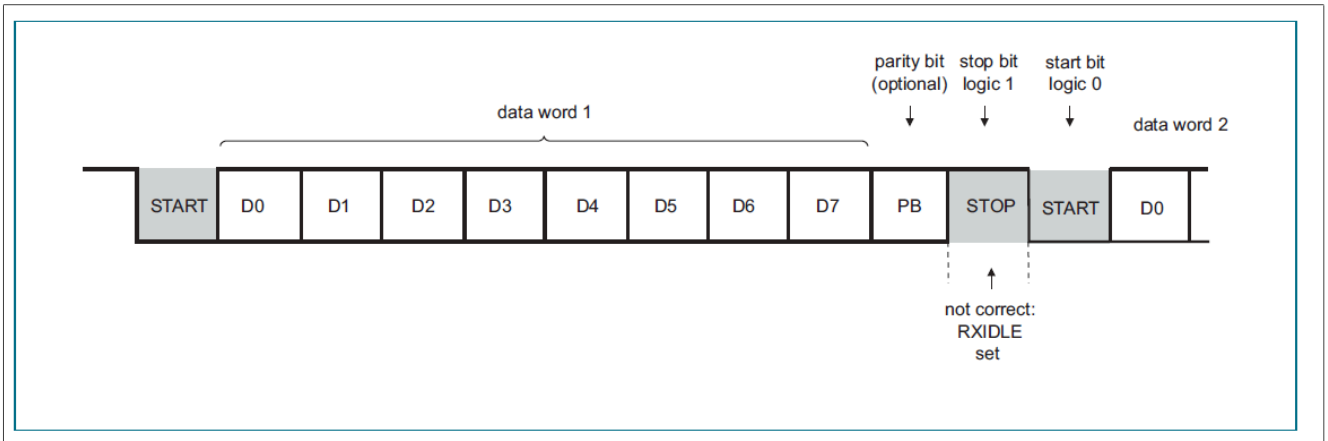

Figure 1. Incorrect setting of RXIDLE during UART receive

Both, TXIDLE and TXDISSTAT are set incorrectly between the last data bit and the stop bit while the transfer is still ongoing.

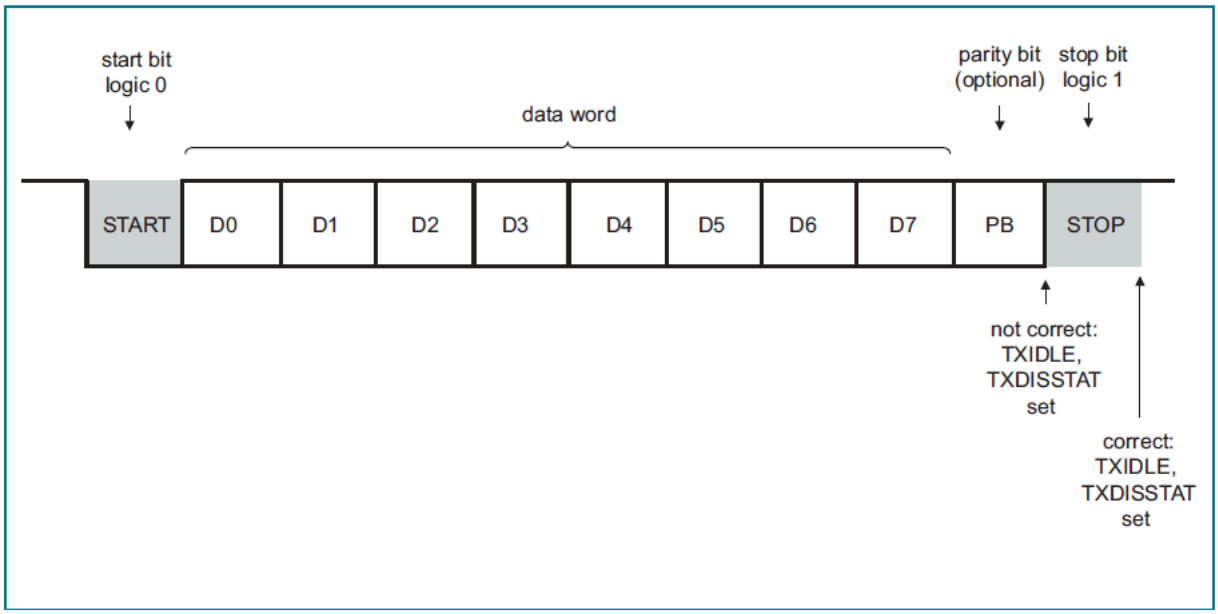

Figure 2. Incorrect setting of TXIDLE and TXDISSTAT during UART transmit

Work-around:

When writing code that checks for the setting of any of the status bits RXIDLE, TXIDLE, TXDISSTAT, check the value of the status bit in the STAT register:

- If status bit = 1, add a delay of one UART bit time (if STOPLEN = 0, one stop bit) or two bit times (if STOPLEN = 1, two stop bits) and check the value of the status bit again:
  - If status bit = 1, the receiver is idle.
  - If status bit = 0, the receiver is receiving data.
- If the status bit = 0, the receiver is receiving data.

3.2 ROM.1: On the LPC11E6x, the ROM inadvertently reports IAP busy status for IAP erase and program operations

Introduction:

On the LPC11E6x, In-Application Programming (IAP) calls are available to perform erase and write operation on the on-chip flash memory, as directed by the end-user application code. IAP status codes are available for the IAP calls.

Problem:

For IAP erase (sector and page) calls and IAP copy RAM to flash API calls, the ROM inadvertently reports that the flash programming hardware interface is busy (IAP status code 11).

Work-around:

The following software workaround can be implemented in the user application code. The example below is for IAP erase operations and utilizes the interrupt status register of the flash IP to ensure that the IAP erase operation is completed successfully:

```
 /* flash controller INT_STATUS register address for the workaround */
 #define     INT_STATUS   ((volatile unsigned *)(0x4003CFE0))
 #define     END_OF_BURN              (1<<1)
 #define     END_OF_ERASE             (1<<0)
__attribute__((section(".iap_ramfunc"))) uint32_t iap_erase_page(uint8_t
 page_start, uint8_t page_end)
        {
        volatile uint32_t dummy = 0;
        uint32_t dummy_pos = 0;
        struct sIAP IAP;
        IAP.cmd = IAP_ERASE_PAGE;                        // Erase Page
        IAP.par[0] = page_start;                        // Start page
        IAP.par[1] = page_end;                                // End page
        IAP.par[2] = SystemCoreClock / 1000; // CCLK in kHz
        while (((*INT_STATUS) & 0x8) != 0)
        {
                dummy = *(volatile uint32_t *)(0x0 + dummy_pos);
                *INT_CLR_STATUS = 0x8;

                if(((*INT_STATUS) & 0x8) != 0x8)
                {
                        break;
                }
                /* Find a flash location without ECC error */
                dummy_pos += 4;
                /* For LPC11E6x, the flash size is 0x10000 */
                if (dummy_pos >= 0x10000)
                {
                        return BUSY;
                }
        }
        IAP_Call(&IAP.cmd, &IAP.stat); // Call IAP Command
        if (IAP.stat == BUSY)
        {
                // If it returns BUSY, wait until program/erase is done
                while ((*INT_STATUS & (END_OF_BURN | END_OF_ERASE)) == 0);
                IAP.stat = 0;
                return (IAP.stat); // Command Failed
        }
        return (0);
}
```

4 AC/DC deviations detail

4.1 n/a

5 Errata notes detail

5.1 n/a

6 Revision history

Table 5. Revision history

Document ID	Release date	Description
ES_LPC11E6x v. 1.2	19 January 2024	• Added Section 3.2
ES_LPC11E6x v. 1.1	22 October 2014	• Added Section 3.1
ES_LPC11E6x v. 1	1 April 2014	• Initial version.

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