KEA128_2N45K, 0P37C

Mask Set Errata for Mask 2N45K, 0P37C

Rev. 30 January 2024 Errata

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This report applies to mask 2N45K and 0P37C for these products:

- KEA128

Table 1.

Errata ID	Errata Title
6946	Core: A debugger write to the I/O port might be corrupted during a processor write
6945	Core: Processor executing at HardFault priority might enter Lockup state if an NMI occurs during a waited debugger transaction
7914	PIT: After enabling the Periodic Interrupt Timer (PIT) clock gate, an attempt to immediately enable the PIT module may not be successful.

e6946: Core: A debugger write to the I/O port might be corrupted during a processor write

Errata type: Errata

Description: A debugger can perform memory accesses through the Cortex-M0+ processor bus matrix while the processor is running.

Because of this erratum, a debugger write to the I/O port might be corrupted if it occurs while the processor is executing a write. The processor write completes successfully. However, under specific timing conditions, the matrix might incorrectly replace the debugger write data with the value zero.

This erratum does not affect debugger writes outside the I/O port region of the memory map, or debugger reads.

Conditions:

The following timing-specific conditions must all be met:

- The processor is running (not halted in Debug state).
- The debugger performs a write within the I/O port region of the memory map.
- The processor performs a write. Implications:

The debugger might corrupt the targeted memory or configure the targeted device incorrectly.

Workaround: The debugger can work around this erratum by halting the processor in Debug state before performing writes to the I/O port region of the memory map.

e6945: Core: Processor executing at HardFault priority might enter Lockup state if an NMI occurs during a waited debugger transaction

Errata type: Errata

Description: A debugger can perform memory accesses through the Cortex-M0+ processor bus matrix while the processor is running.

Because of this erratum, the processor might erroneously enter Lockup state if a debugger- initiated access on the AHB-Lite master port is subject to wait states while the processor is running, executing at HardFault priority and taking a Non Maskable Interrupt (NMI). Under very specific timing conditions, the processor might incorrectly stack a ReturnAddress of 0xFFFFFFFE on NMI entry. On NMI return, the processor unstacks the incorrectly stacked ReturnAddress and enters Lockup state at HardFault priority.

Conditions:

The following timing-specific conditions must all be met:

- The processor is running (not halted in Debug state) and is executing at HardFault priority.
- The processor executes a single-cycle instruction at a word-aligned address.
- The debugger performs an access through the AHB-Lite master port that is subject to wait states.
- An NMI becomes pending. Implications:

The processor stops executing the code in the HardFault handler and enters Lockup state at HardFault priority as if a fault had occurred.

Workaround: The debugger can work around this erratum by halting the processor in Debug state before performing accesses outside the Private Peripheral Bus (PPB) region of the memory map.

e7914: PIT: After enabling the Periodic Interrupt Timer (PIT) clock gate, an attempt to immediately enable the PIT module may not be successful.

Errata type: Errata

Description: If a write to the PIT module enable bit (PIT_MCR[MDIS]) occurs within two bus clock cycles of enabling the PIT clock gate in the SIM_CG register, the write will be ignored and the PIT will fail to enable.

Workaround: Insert a read of the PIT_MCR register before writing to the PIT_MCR register. This guarantees a minimum delay of two bus clocks to guarantee the write is not ignored.

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