Mask Set Errata for Mask 0P06B

This report applies to mask 0P06B for these products:

- MKW39A512VFT4
- MKW38A512VFT4, MKW38Z512VFT4
- MKW37A512VFT4, MKW37Z512VFT4

Table 1. Errata and Information Summary

Erratum ID	Erratum Title
ERR003863	ADC: In 16-bit differential mode, ADC may result in a conversion error when positive input is near upper rail reference voltage
ERR007993	MCG: FLL frequency may be incorrect after changing the FLL reference clock

Table 2. Revision History

Revision	Changes
2	Initial revision

ERR003863: ADC: In 16-bit differential mode, ADC may result in a conversion error when positive input is near upper rail reference voltage

Description: In 16-bit differential mode, the ADC may result in a conversion error when the input voltage on the plus-side of the differential pair (DPx) exceeds approximately (VREFH*31/32). Other modes are unaffected.

Workaround: To avoid a conversion error near positive full-scale in this mode, do not allow the input voltage on the plus-side of the differential pair (DPx) to exceed (VREFH*31/32).

ERR007993: MCG: FLL frequency may be incorrect after changing the FLL reference clock

Description: When the FLL reference clock is switched between the internal reference clock and the external reference clock, the FLL may jump momentarily or lock at a higher than configured frequency. The higher FLL frequency can affect any peripheral using the FLL clock as its input clock. If the FLL is being used as the system clock source, FLL Engaged Internal (FEI) or FLL Engaged External (FEE), the maximum system clock frequency may be exceeded and can cause indeterminate behavior.

Only transitions from FLL External reference (FBE, FEE) to FLL Internal reference (FBI, FEI) modes and vice versa are affected. Transitions to and from BLPI, BLPE, or PLL clock modes (if supported) are not affected because they disable the FLL. Transitions between the external reference modes or between the internal reference modes are not affected because the reference clock is not changed.

Workaround: To prevent the occurrence of this jump in frequency either the MCG_C4[DMX32] bit must be inverted or the MCG_C4[DRST_DRS] bits must be modified to a different value immediately before the change in reference clock is made and then restored back to their original value after the MCG_S[IREFST] bit reflects the selected reference clock.

If you want to change the MCG_C4[DMX32] or MCG_C4[DRST_DRS] to new values along with the reference clock, the sequence described above must be performed before setting these values to the new value(s).

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