

Mask Set Errata for Mask 0N79P

This report applies to mask 0N79P for these products:

- MKE1xF512VLL16
- MKE1xF512VLH16
- MKE1xF256VLL16
- MKE1xF256VLH16

Table 1. Errata and Information Summary

Erratum ID	Erratum Title
ERR010575	BootROM: Two Bootloader GetProperty commands of RAM size and start address return value are not correct
ERR006939	Core: Interrupted loads to SP can cause erroneous behavior
ERR009004	Core: ITM can deadlock when global timestamping is enabled
ERR009005	Core: Store immediate overlapping exception return operation might vector to incorrect interrupt
ERR006940	Core: VDIV or VSQRT instructions might not complete correctly when very short ISRs are used
ERR050117	FAC: Execute-only access control feature has been deprecated
ERR050246	FlexCAN: Receive Message Buffers may have its Code Field corrupted if the Receive FIFO function is used
ERR050180	GPIO glitch possible during power up and power down
ERR010364	LPI2C: LPI2C sends a STOP condition if transmit FIFO is empty on the completion of a master-receive transfer
ERR050181	LPIT CVAL cannot be read correctly during timer running
ERR010527	LPUART: Setting and immediately clearing SBK bit can result in transmission of two break characters
ERR010180	SCG: Clock switch may hang if SCG_RCCR is written to the switch system clock source with a different divide ratio while an external reset is asserted
ERR010536	WDOG: After getting RCS assertion by polling, 4 LPO clock-time delay is the minimum requirement before the next block



Table 2. Revision History

Revision	Changes
26 May 2016	Initial revision
15 Aug 2016	The following errata were added. <ul style="list-style-type: none"> • ERR010527 • ERR010536
29 Aug 2016	The following errata were added. <ul style="list-style-type: none"> • ERR006940 • ERR009005 • ERR009004 • ERR006939 • ERR010180
2 Sep 2016	The following erratum was added. <ul style="list-style-type: none"> • ERR010575 The following erratum was revised. <ul style="list-style-type: none"> • ERR010364
15Apr2020	The following errata were added. <ul style="list-style-type: none"> • ERR050246 • ERR050180 • ERR050117 • ERR050181 The following errata were revised. <ul style="list-style-type: none"> • ERR006939 • ERR009004 • ERR009005 • ERR006940
06Jul2020	The following erratum was revised. <ul style="list-style-type: none"> • ERR050180

ERR010575: BootROM: Two Bootloader GetProperty commands of RAM size and start address return value are not correct

Description: On MKE1xF256VLL16 and MKE1xF256VLH16 parts, two Bootloader GetProperty commands of RAM size and start address return value are not correct. The RAM start address return value mentioned is 0x1FFFE000. However, the actual RAM start address is 0x1FFFC000. The RAM size return value mentioned is 16 KB. However, the actual RAM size is 32 KB. Thus, you can only access 16 KB RAM by the BootROM.

Workaround: No workaround. Only the RAM memory access by BootROM has this limitation. Other RAM access is normal.

ERR006939: Core: Interrupted loads to SP can cause erroneous behavior

Description: Arm Errata 752770: Interrupted loads to SP can cause erroneous behavior

This issue is more prevalent for user code written to manipulate the stack. Most compilers will not be affected by this, but please confirm this with your compiler vendor. MQX™ and FreeRTOS™ are not affected by this issue.

Affects: Cortex-M4, Cortex-M4F

Fault Type: Programmer Category B

Fault Status: Present in: r0p0, r0p1 Open.

If an interrupt occurs during the data-phase of a single word load to the stack-pointer (SP/R13), erroneous behavior can occur. In all cases, returning from the interrupt will result in the load instruction being executed an additional time. For all instructions performing an update to the base register, the base register will be erroneously updated on each execution, resulting in the stack-pointer being loaded from an incorrect memory location.

The affected instructions that can result in the load transaction being repeated are:

- 1) LDR SP,[Rn],#imm
- 2) LDR SP,[Rn,#imm]!
- 3) LDR SP,[Rn,#imm]
- 4) LDR SP,[Rn]
- 5) LDR SP,[Rn,Rm]

The affected instructions that can result in the stack-pointer being loaded from an incorrect memory address are:

- 1) LDR SP,[Rn],#imm
- 2) LDR SP,[Rn,#imm]!

Conditions:

- 1) An LDR is executed, with SP/R13 as the destination.
- 2) The address for the LDR is successfully issued to the memory system.
- 3) An interrupt is taken before the data has been returned and written to the stack-pointer.

Implications:

Unless the load is being performed to Device or Strongly-Ordered memory, there should be no implications from the repetition of the load. In the unlikely event that the load is being performed to Device or Strongly-Ordered memory, the repeated read can result in the final stack-pointer value being different than had only a single load been performed.

Interruption of the two write-back forms of the instruction can result in both the base register value and final stack-pointer value being incorrect. This can result in apparent stack corruption and subsequent unintended modification of memory.

Workaround: Most compilers are not affected by this, so a workaround is not required.

However, for hand-written assembly code to manipulate the stack, both issues may be worked around by replacing the direct load to the stack-pointer, with an intermediate load to a general-purpose register followed by a move to the stack-pointer.

If repeated reads are acceptable, then the base-update issue may be worked around by performing the stack pointer load without the base increment followed by a subsequent ADD or SUB instruction to perform the appropriate update to the base register.

ERR009004: Core: ITM can deadlock when global timestamping is enabled

Description: ARM ERRATA 806422

The Cortex-M4 processor contains an optional Instrumentation Trace Macrocell (ITM). This can be used to generate trace data under software control, and is also used with the Data Watchpoint and Trace (DWT) module which generates event driven trace. The processor supports global timestamping. This allows count values from a system-wide counter to be included in the trace stream.

When connected directly to a CoreSight funnel (or other component which holds ATREADY low in the idle state), the ITM will stop presenting trace data to the ATB bus after generating a timestamp packet. In this condition, the ITM_TCR.BUSY register will indicate BUSY.

Once this condition occurs, a reset of the Cortex-M4 is necessary before new trace data can be generated by the ITM.

Timestamp packets which require a 5 byte GTS1 packet, or a GTS2 packet do not trigger this erratum. This generally only applies to the first timestamp which is generated.

Devices which use the Cortex-M optimized TPIU (CoreSight ID register values 0x923 and 0x9A1) are not affected by this erratum.

Workaround: There is no software workaround for this erratum. If the device being used is susceptible to this erratum, you must not enable global timestamping.

ERR009005: Core: Store immediate overlapping exception return operation might vector to incorrect interrupt

Description: Arm Errata 838869: Store immediate overlapping exception return operation might vector to incorrect interrupt

Affects: Cortex-M4, Cortex-M4F

Fault Type: Programmer Category B Rare

Fault Status: Present in: r0p0, r0p1 Open.

The Cortex-M4 includes a write buffer that permits execution to continue while a store is waiting on the bus. Under specific timing conditions, during an exception return while this buffer is still in use by a store instruction, a late change in selection of the next interrupt to be taken might result in there being a mismatch between the interrupt acknowledged by the interrupt controller and the vector fetched by the processor.

Configurations Affected

This erratum only affects systems where writeable memory locations can exhibit more than one wait state.

Workaround: For software not using the memory protection unit, this erratum can be worked around by setting DISDEFWBUF in the Auxiliary Control Register.

In all other cases, the erratum can be avoided by ensuring a DSB occurs between the store and the BX instruction. For exception handlers written in C, this can be achieved by inserting the appropriate set of intrinsics or inline assembly just before the end of the interrupt function, for example:

ARMCC:

```
...
__schedule_barrier();
__asm{DSB};
__schedule_barrier();
}
```

GCC:

```
...
__asm volatile ("dsb 0xf" ::: "memory");
}
```

ERR006940: Core: VDIV or VSQRT instructions might not complete correctly when very short ISRs are used

Description: Arm Errata 776924: VDIV or VSQRT instructions might not complete correctly when very short ISRs are used

Affects: Cortex-M4F

Fault Type: Programmer Category B

Fault Status: Present in: r0p0, r0p1 Open.

On Cortex-M4 with FPU, the VDIV and VSQRT instructions take 14 cycles to execute. When an interrupt is taken a VDIV or VSQRT instruction is not terminated, and completes its execution while the interrupt stacking occurs. If lazy context save of floating point state is enabled then the automatic stacking of the floating point context does not occur until a floating point instruction is executed inside the interrupt service routine.

Lazy context save is enabled by default. When it is enabled, the minimum time for the first instruction in the interrupt service routine to start executing is 12 cycles. In certain timing conditions, and if there is only one or two instructions inside the interrupt service routine, then the VDIV or VSQRT instruction might not write its result to the register bank or to the FPSCR.

Workaround: A workaround is only required if the floating point unit is present and enabled. A workaround is not required if the memory system inserts one or more wait states to every stack transaction.

There are two workarounds:

1) Disable lazy context save of floating point state by clearing LSPEN to 0 (bit 30 of the FPCCR at address 0xE000EF34).

2) Ensure that every interrupt service routine contains more than 2 instructions in addition to the exception return instruction.

ERR050117: FAC: Execute-only access control feature has been deprecated

Description: The FAC feature is no longer recommended for use.

Workaround: Do not program the XACCn registers to use the FAC feature.

ERR050246: FlexCAN: Receive Message Buffers may have its Code Field corrupted if the Receive FIFO function is used

Description: If the Code Field of a Receive Message Buffer is corrupted it may deactivate the Message Buffer, so it is unable to receive new messages. It may also turn a Receive Message Buffer into any type of Message Buffer as defined in the Message buffer structure section in the device documentation.

The Code Field of the FlexCAN Receive Message Buffers (MB) may get corrupted if the following sequence occurs.

- 1- A message is received and transferred to an MB (i.e. MBx)
- 2- MBx is locked by software for more than 20 CAN bit times (time determines the probability of erratum to manifest).
- 3- SMB0 (Serial Message Buffer 0) receives a message (i.e. message1) intended for MBx, but destination is locked by the software (as depicted in point 2 above) and therefore NOT transferred to MBx.
- 4- A subsequent incoming message (i.e. message2) is being loaded into SMB1 (as SMB0 is full) and is evaluated by the FlexCAN hardware as being for the FIFO.
- 5- During the message2, the MBx is unlocked. Then, the content of SMB0 is transferred to MBx and the CODE field is updated with an incorrect value.

In case a customer does use Rx FIFO only or dedicated MB only, (i.e. either Rx MB or Rx FIFO is used) the problem doesn't occur. In case a customer does use the Enhanced Rx FIFO and dedicated MB at the same application, the problem does not occur also. So bottom line the problem does only occur if the FlexCAN is programmed to receive in the Legacy FIFO and dedicated MB at the same application.

Workaround: This defect only applies if the Receive FIFO (Legacy Rx FIFO) is used. This feature is enabled by RFEN bit in the Module Control Register (MCR). If the Rx FIFO is not used, the Receive Message Buffer Code Field is not corrupted.

If available on the device, use the enhanced Rx FIFO feature instead of the Legacy Rx FIFO. The Enhanced Rx FIFO is enabled by the ERFEN bit in the Enhanced Rx FIFO Control Register (ERFCR).

The defect does not occur if the Receive Message Buffer lock time is less than or equal to the time equivalent to 20 x CAN bit time.

The recommended way for the CPU to service (read) the frame received in a mailbox is by the following procedure:

1. Read the Control and Status word of that mailbox.
2. Check if the BUSY bit is deasserted, indicating that the mailbox is not locked. Repeat step 1) while it is asserted.
3. Read the contents of the mailbox.

4. Clear the proper flag in the IFLAG register.
5. Read the Free Running Timer register (TIMER) to unlock the mailbox

In order to guarantee that this procedure occurs in less than 20 CAN bit times the MB receive handling process in software (step 1 to step 5 above) should be performed as a 'critical code section' (interrupts disabled before execution) and should ensure that the MB receive handling occurs in a deterministic number of cycles.

ERR050180: GPIO glitch possible during power up and power down

Description: During power up and power down, specific groups of pins can be inadvertently pulled high while Vdd rises up to or decays below the Vpor level. The specific groups must have an internal or external pull-up resistor on at least one pin in the group for the glitch to occur. There are 50 pins in total that can have this behavior during power up and power down, including

Group A: PTA0, PTA1, PTA6, PTA7, PTA15, PTA16, PTB0, PTB1, PTB2, PTB3, PTB8, PTB9, PTB10, PTB11, PTB13, PTB14, PTB15, PTB16, PTC8, PTC9, PTE2, PTE6, PTE10, PTE11;

Group B: PTC0, PTC1, PTC2, PTC3, PTC14, PTC15, PTC16, PTC17;

Group C: PTA2, PTA3, PTB12, PTC6, PTC7, PTD2, PTD3, PTD4;

Group D: PTA12, PTA13, PTB17, PTD0, PTD1, PTE0, PTE1, PTE7;

Group E: PTE5, PTE9.

In Group C, PTD3/NMI has an internal pull-up resistor (typical 40kOhm) enabled during power up and power down, while in other groups, there is no such internal pull-up resistor enabled by default.

Workaround: Use one or more of the following workarounds.

1. Do not use pins in the affected groups for critical active-high output functions.
2. Avoid using external pull-up resistors on pins within Group A/B/D/E if any of these pins are used for critical active-high output functions.
3. A pull-down resistor added to a pin within the impacted pin group can reduce the glitch strength for all pins in the group, as the pull-down resistor acts as a voltage divider. Given that the maximum voltage of the glitch is Vpor, pull-up resistor is Rpu, pull-down resistor is Rpd, then the reduced glitch magnitude on the given pin would be: $Vpor * Rpd / (Rpu + Rpd)$. For example, given the typical 40kOhm internal pull-up resistor on the PTD3/NMI pin, a 10kOhm pull-down resistor on any of the impacted pins in Group C will attenuate the magnitude of the glitch on these pins to: $2.0V * 10k / (40k + 10k) = 0.4V$.

ERR010364: LPI2C: LPI2C sends a STOP condition if transmit FIFO is empty on the completion of a master-receive transfer

Description: If the transmit FIFO is empty at the end of a master receive transfer and the AUTOSTOP (MCFGR1[AUTOSTOP]) bit in the Master Configuration Register 1 is clear, the LPI2C master sends a STOP condition before the next repeated START condition.

Workaround: Use software or DMA to queue up the subsequent transfer in the transmit FIFO before the completion of the master-receive transfer.

ERR050181: LPIT CVAL cannot be read correctly during timer running

Description: Customer reported a LPIT CVAL reading issue, that CVAL cannot be read correctly during timer running.

The root cause per IP owner feedback is:

The LPIT implements a functional clock domain for the counter and a bus clock domain for the register interface. The CVAL register increments on each clock cycle, but reading the register value is not synchronized when it changes clock domains. This can result in the CVAL register not being read correctly (eg: read returns some bits from previous cycle and some bits from next cycle).

Workaround: While the timer is running, CVALn register reads may not return the real value. If the timer value needs to be read, read it during an LPIT interrupt service routine.

ERR010527: LPUART: Setting and immediately clearing SBK bit can result in transmission of two break characters

Description: When the LPUART transmitter is idle (LPUART_STAT[TC]=1), two break characters may be sent when using LPUART_CTRL[SBK] to send one break character. Even when LPUART_CTRL[SBK] is set to 1 and cleared (set to 0) immediately.

Workaround: To queue a single break character via the transmit FIFO, set LPUART_DATA[FRETSC]=1 with data bits LPUART_DATA[T9:T0]=0.

ERR010180: SCG: Clock switch may hang if SCG_RCCR is written to the switch system clock source with a different divide ratio while an external reset is asserted

Description: SCG: Clock switch may hang if SCG_RCCR is written to the switch system clock source with a different divide ratio while an external reset is asserted. For example, if SCG is in the FIRC mode and then configured to the SIRC mode, by writing the RCCR to switch system clock with a different divide ratio, during which the external reset is asserting, then the clock switch may hang.

Workaround: To recover the clock switch another reset must be issued.

ERR010536: WDOG: After getting RCS assertion by polling, 4 LPO clock-time delay is the minimum requirement before the next block

Description: WDOG cannot be unlocked if the unlock magic word are executed immediately after the RCS assert.

Workaround: After getting RCS assertion by polling, 4 LPO clock-time delay is the minimum requirement before next block.

How to Reach Us:**Home Page:**nxp.com**Web Support:**nxp.com/support

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

While NXP has implemented advanced security features, all products may be subject to unidentified vulnerabilities. Customers are responsible for the design and operation of their applications and products to reduce the effect of these vulnerabilities on customer's applications and products, and NXP accepts no liability for any vulnerability that is discovered. Customers should implement appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREENCHIP, HITAG, I2C BUS, ICODE, JCOP, LIFE VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, AltiVec, C-5, CodeTEST, CodeWarrior, ColdFire, ColdFire+, C-Ware, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, Ready Play, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, SMARTMOS, Tower, TurboLink, and UMEMS are trademarks of NXP B.V. All other product or service names are the property of their respective owners. AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, μ Vision, Versatile are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

© 2020 NXP B.V.

