MC9328MX21 and MC94MX21

Chip Errata for Masks: 1L45X, 2L45X, 0M55B, 1M55B, M55B

Table 1 provides silicon errata information that relates to the masks 1L45X, 2L45X, 0M55B, 1M55B, and M55B of the MC9328MX21 and MC94MX21 (i.MX21) applications processor.

Table 1. Silicon Errata to MC9328MX21 and MC94MX21

Erratum Number	Erratum Description	Details/Impact, Workaround, and Fix Status	Mask
1.	**Module:** EIM **Failure:** EIM Cellular RAM support fails	**Details:** For Infineon Cellular RAM HYE18P32160AC(-/L) 12.5, burst writes can work with the following constraints: 1. EW bit does not work correctly—When the EW bit is set, failures are found when WSC= 7 and Cellular RAM is set up for LAT2. It does work when WSC=9 and Cellular RAM is set for LAT3. This greatly effects burst writes and reads. EW=0 always works (as NOR flash end current burst). 2. After performing a sync access (like burst read), the Infineon Cellular RAM expects another rising clock edge when CS goes high to terminate burst—If the Cellular RAM is left idle after a burst read and NO rising clock edge is detected, it is *stuck* in sync mode not allowing internal refresh cycles to occur—this will cause Cellular RAM to lose data. This appears to be more of an Infineon issue as Micron asserts the extra rising edge clock is not needed. Also, Infineon stated that in their next generation Cellular RAM this extra rising edge clock is not required. 3. *BCS bits do not shift the burst clock correctly*—Only BCS bit 0 (LSB) effects the shifting of burst clock, other bits do not effect burst clock phase (though they still effect LBA assertion time). 4. Only async writes are possible to Cellular RAM BCR and RCR—In addition, when switching modes or re-programming the RCR/BCR, the system must first be placed back into async mode.	1L45X 2L45X 0M55B 1M55B M55B

Table 1. Silicon Errata to MC9328MX21 and MC94MX21 (continued)

Erratum Number	Erratum Description	Details/Impact, Workaround, and Fix Status	Mask
1. *Continued*	**Module:** EIM **Failure:** EIM Cellular RAM support fails	5. When D cache is enabled and EIM is doing async writes to the Cellular RAM, the EIM will hold CS asserted (low) for >10us—This causes a problem for Cellular RAM because it cannot perform an internal refresh operation. The work around is to set CSA to 1 to force CS assertion between writes to allow time for Cellular RAM to refresh or to place EIM and Cellular RAM in sync mode of operation (burst writes) whenever D cache is enabled. **Workaround:** 1. Cellular RAM is basically Mobile SDRAM with the exception of a NOR flash interface. MX21 has an SDRAM controller. System designers are advised to use Mobile SDRAM for its higher performance(133 MHz) and lower cost. 2. Recommend not to enable burst write and treat Cellular RAM as NOR flash burst interface. **Fix Status:** No fix solution is planned.	1L45X 2L45X 0M55B 1M55B M55B
2.	**Module:** PCMCIA **Failure:** Inverted PC_POE causes possible system boot up failure when PCMCIA buffer is used.	**Details/Impact:** The PC_POE pin may cause system boot up failure when PCMCIA interface buffer is connected directly. This is due to PC_POE pin (muxed with NFCLE) driven low during initial boot (with/without NAND Flash) which enables the external buffer and results in data bus contention. This multiplexed signal can be re-programmed to perform the PC_OE function after the system starts up, therefore, only boot time is affected. **Workaround:** Add a logic gate on board between the PC_POE signal and the PCMCIA buffer such that the buffer is disabled at boot time. An additional GPIO is required to control the gate ON/OFF. **Fix Status:** No fix solution is planned.	1L45X 2L45X 0M55B 1M55B M55B

Table 1. Silicon Errata to MC9328MX21 and MC94MX21 (continued)

Erratum Number	Erratum Description	Details/Impact, Workaround, and Fix Status	Mask
3.	**Module:** PCMCIA **Failure:** Cannot fully support CF/CF+ specification.	**Details:** The PCMCIA controller only supports up to 2 Kbytes of total space to map the attribute memory, common memory, or I/O space. However, the CF/CF+ specification and operating systems such as WinCE/PPC, require them to locate at a separate space and beyond the 2 Kbyte range. **Impact:** CF/CF+ cannot be supported on WinCE/PPC. Possible difficulty in building drivers in other OS. **Workaround:** CF/CF+ card support: No workaround available to support WinCE OS. For other OS, basic functionality can be fulfilled by allocating 1 Kbyte to attribute memory and 1 Kbyte to I/O memory or common memory. **Fix Status:** CF/CF+ support problem is fixed in masks 0M55B, 1M55B, and M55B. PCMCIA Base registers 0–4 are enhanced to hold base addresses PBA[14:4] in the same programmable bits position. Memory windows such as common memory space, I/O space, True IDE or attribute memory space can be defined in an extended 32K space. Please refer to *MC9328MX21 Mask Differences Between 2L45X and M55B Reference Manual Addendum for MC9328MX21RM,* for further information on PCMCIA changes.	1L45X 2L45X
4.	**Module:** PCMCIA **Failure:** Not fully compliant with PCMCIA Ver. 2.1.	**Details:** A total of 26 address lines are needed to fully support the PCMCIA standard. The i.MX21 processor does not support this many address lines. **Impact:** PCMCIA cards cannot be supported. **Workaround:** No workaround is available. **Fix Status:** No fix solution is planned.	1L45X 2L45X 0M55B 1M55B M55B
5.	**Module:** SSI **Failure:** AC97 Mode cannot be supported.	**Details/Impact:** In AC97 variable mode, the AC97 controller is required to process the SLOTREQ automatically and source data from the transmit FIFO. However, the SLOTREQ bits are not handled and no variable mode operation is possible. **Workaround:** No workaround is available. **Fix Status:** No fix solution is planned.	1L45X 2L45X 0M55B 1M55B M55B

Table 1. Silicon Errata to MC9328MX21 and MC94MX21 (continued)

Erratum Number	Erratum Description	Details/Impact, Workaround, and Fix Status	Mask
6.	**Module:** SSI **Failure:** SSI does not wait for frame sync to receive data when RE is enabled in sync mode.	**Details/Impact:** When TE has been enabled and RE is enabled in the middle of a valid frame, the SSI starts to receive data immediately without synchronizing with the next frame sync event. This causes the receiver section to remain out-of-sync with the frame timing and results in incorrect data received. **Workaround:** System designer is advised to: 1. Wait for the TLS (Transmit Last Slot) interrupt before enabling the receiver, Or 2. Disable the transmitter, then enable both transmitter and receiver simultaneously. **Fix Status:** This erratum is corrected in masks 0M55B, 1M55B, and M55B.	1L45X 2L45X
7.	**Module:** GP Timer **Failure:** The GP timer counter is reset even in freerun mode whenever the compare register is written.	**Details/Impact:** The counter is enhanced to reset automatically in restart mode. However, the change also influences freerun mode. The counter is now reset whenever the compare register is written. Applications are affected that allow compare values to change from time to time. **Workaround:** If more than one compare event is needed in freerun mode, use software comparisons instead. **Fix Status:** This erratum is corrected in masks 0M55B and 1M55B.	1L45X 2L45X
8.	**Module:** EIM **Failure:** RW assertion incorrectly influenced by RWN bit in EIM module when RWA = 0 and RWN ≥ 1.	**Details:** In EIM Chip select control register, there are two bits controlling the RW assertion and deassertion (negation) time: RWA and RWN. It is found that RWN incorrectly influences the assertion of the RW signal when RWA = 0 and RWN ≥ 1. The RW signal assertion is delayed 1/2 HCLK later. The RW signals acts as though RWA is set to 1, even though RWA bit is cleared in software. Other settings work correctly. **Impact:** Minimal. A slight timing delay is introduced to RW signal assertion. **Workaround:** No workaround is available. **Fix Status:** No fix solution is planned.	1L45X 2L45X 0M55B 1M55B M55B

Table 1. Silicon Errata to MC9328MX21 and MC94MX21 (continued)

Erratum Number	Erratum Description	Details/Impact, Workaround, and Fix Status	Mask
9.	**Module:** Power **Failure:** Standby current at QVDD and NVDD is higher than the typical value specified in data sheet.	**Details/Impact:** Standby current at QVDD and NVDD is higher than the typical value specified in data sheet. **Workaround:** No workaround is available. **Fix Status:** Standby current has been improved on subsequent masks. Please refer to the MC9328MX21 data sheet for power figures.	1L45X
10.	**Module:** BMI **Failure:** BMI Tx_Water_Mark bit = 0000 fails.	**Details/Impact:** When setting BMI Tx_Water_Mark bit to 0000, TxF_EMPTY status bit will always be set. This makes detecting 16 empty slots in FIFO impossible and user will not be able to check if the last data has been transmitted. Therefore, variable burst transfer cannot be supported. **Workaround:** System designer is advised to define data transfer with a fixed burst length for reliable communication. **Fix Status:** No fix solution is planned.	1L45X 2L45X 0M55B 1M55B M55B
11.	**Module:** SDRAMC **Failure:** SDRAM Power Down mode failing to support both CSD0 and CSD1 simultaneously.	**Details:** Memory access may fail at the following condition: 1. Both CSD0 and CSD1 are used, and 2. Both Power-down time-out bits of SDCTL0 and SDCTL1 are programmed to non-zero. **Impact:** As SDRAM cannot be put to power down mode, a slightly higher operating power may result. This issue does not affect self refresh mode operation and no difference in sleep mode power will be seen. **Workaround:** It is advised to program Powerdown Timout bits of SDCTL0 and SDCTL1 to ZERO when using both CSD0 and CSD1. This issue does not happen when single CSD0 or CSD1 is used. **Fix Status:** No fix solution is planned.	1L45X 2L45X 0M55B 1M55B M55B
12.	**Module:** NAND Flash Memory Controller **Failure:** Cannot support NAND Flash memory requiring CE_B pin held low during tR (data transfer from cell to register) period.	**Details/Impact:** NAND Flash controller drives the NF_CE signal high in tR period. For NAND Flash memory that requires CE_B to be held low during the tR period, memory access failure may result. **Workaround:** This can be accomplished through the use of an external AND gate, where the $\overline{\text{NFCE}}$ and NFRB signals of the i.MX21 are inputs to the AND gate and the output is connected to the CE_B input of the NAND Flash device. **Fix Status:** No fix solution is planned.	1L45X 2L45X 0M55B 1M55B M55B

Table 1. Silicon Errata to MC9328MX21 and MC94MX21 (continued)

Erratum Number	Erratum Description	Details/Impact, Workaround, and Fix Status	Mask
13.	**Module:** SDIO Controller **Failure:** Multiple block transfer support fails if no BUSY signal is detected.	**Details/Impact:** After sending the first block of data, the SDIO controller operation will stop if there is no BUSY signal detected. Therefore, multiple block transfers without any BUSY signal responding from card cannot be supported. **Workaround:** No workaround is available for multiple block transfers. It requires card manufacturers to modify their firmwire to use single block transfers if not currently supported. **Fix Status:** Multiple block transfers are supported in the following cases: • multi-block reads • operation in 1-bit mode • busy signal is supported • 4-bit mode, when fast DMACLK (HCLK) is not used, see below Multiple block transfer are not supported when all of the following conditions apply: • multi-block writes, and • there is no busy signal between blocks, and • 4-bit bus width, and • when DMACLK (HCLK) is faster than MMCCLK/0.216. For example, 20 MHz SDIO, cannot use DMACLK (HCLK) faster than 92.6 MHz, thus HCLK cannot be 133 MHz during SDIO 4-bit multi-block reads.	1L45X 2L45X 0M55B 1M55B M55B
14.	**Module:** NAND Flash Controller (NFC) **Failure:** NAND Flash warm reset delay	**Details:** When the boot mode is set to NAND Flash boot-up, after the reset_in signal is asserted, the processor needs to wait about 10 seconds before continuing the boot-up process. **Impact:** During the NAND Flash boot-up process, there is a waiting loop that checks the transfer of boot code completion (bit 15 of NAND FLASH Operation and Configuration register 2, NAND_Flash_Config2). However, the bit will not set immediately because the NAND Flash controller will not transfer the whole code during reset_in assertion time. It is required to wait 10 seconds for the NAND Flash controller to reset when a soft reset (Reset_In or Watchdog reset) occurs. **Workaround:** No Workaround is available **Fix Status:** Fixed in 1M55B and M55B	0M55B

Table 1. Silicon Errata to MC9328MX21 and MC94MX21 (continued)

Erratum Number	Erratum Description	Details/Impact, Workaround, and Fix Status	Mask
15.	**Modules:** SDRAMC **Failure:** Cannot support SDRAMs with less than 1kilobyte page size.	**Impact**: Not able to support single chip 4M x 16-bit (8Mbyte total size) SDRAM devices or devices with a page size of less than 1 kilobyte. A page size is defined as the number of bits in a row in the SDRAM device. **Workaround:** Must use SDRAM devices with 1 kilobyte or greater page sizes. **Fix Status:** No fix solution is planned.	1L45X 2L45X 0M55B 1M55B M55B
16.	**Modules:** SDRAMC **Failure:** Cannot support SDRAMs with column address sizes of 10.	**Impact**: Not able to support single chip 32M x 16-bit (64Mbyte total size) SDRAM devices or devices with a column address size of 10. **Workaround:** For 64 Mbyte SDRAM devices the configuration of 16M x 32 or two 16M x 16-bit must be used to form a 32-bit data bus, where either configuration contains only 9 column addresses. **Fix Status:** No fix solution is planned.	1L45X 2L45X 0M55B 1M55B M55B

Table 1. Silicon Errata to MC9328MX21 and MC94MX21 (continued)

Erratum Number	Erratum Description	Details/Impact, Workaround, and Fix Status	Mask

17.	**Modules:** Power Management
	
	Failure: Increased current consumption in sleep mode.
		Impact:
		When putting the i.MX21 processor in sleep mode, the current consumption is greater than what is specified in the i.MX21 data sheet.
		
		Details:
		An internal oscillator (ring oscillator) is inadvertently active which causes an approximate 800µA increase in the current consumption in sleep mode. Some of the 1M55B production material had this oscillator off by default. However, some material will have this oscillator turned on initially resulting in higher sleep current. Therefore, the ring oscillator must be turned off initially by the user's software.
		
		Workaround:
		Important: Read bit 31 at address: 0x10027810.
		If bit 31 is set (1), then apply the workaround. Otherwise, if the bit is cleared (0) then do not use the workaround.
		Note: Attempting to disable ring oscillator when it is already off will cause the part not to go into sleep mode. Therefore, reading address 0x10027810, bit 31, is necessary to determine the type of material being used.
		Use the following program during the chip initialization process:
		1. Turn on clock to internal module responsible for register access to ring oscillator register: Address: 0x10027024, set (1) bit 21.
		2. Add a small delay to allow clock to register to turn on.
		3. Disable ring oscillator: Address 0x10029000, set (1) bit 4.
		
		Example:
		`(p_uint32_t) (0x10027024) |= 0x00200000;`
		`{`
		`  //delay`
		`}`
		`(p_uint32_t) (0x10029000) |= 0x00000010;`
		
		Fix Status:
		Corrected in the latest 1M55B silicon.
			1M55B

Table 1. Silicon Errata to MC9328MX21 and MC94MX21 (continued)

Erratum Number	Erratum Description	Details/Impact, Workaround, and Fix Status	Mask
18.	**Module:** NFC / System Boot **Failure:** NFC (Nand Flash Controller) fails to correct two single-bit errors if they occur on consecutive pages, on data read accesses.	**Details:** In cases when there are single-bit errors in two consecutive page reads, then the error in the second page is not corrected by the NFC. **Impact:** NFC error correction logic is faulty on read accesses and errors in consecutive pages are not fixed. Thus, software must correct the errors in place of the hardware. Special care must be given when booting from a Nand Flash for both 512 bytes, and 2 Kbytes page boot options—see details under Workaround. **Workaround:** In general, when reading from Nand Flash, SW must turn off the code correction in HW (ECC) and perform the correction in SW (done by performing error check and correction at the end of each page). When booting from Nand Flash, the Nand Flash Controller (NFC) copies the first 2Kbytes to internal RAM and jumps to the beginning of the code. This is done with no option for SW intervention/modification, so the aforementioned general guideline could not be applied. **Note:** If the NAND flash requires Error Correction on the initial block, then the following procedure is required. Otherwise, apply the S/W ECC after boot up: Due to the nature of this bug, any single-bit error (if found) in the first 512 bytes (first page) is corrected properly, therefore, "special" boot loader code must be placed in those first 512 bytes. The loader code, once executed, must then perform the following: 1. Turn off error correction in HW. 2. Re-load pages 2, 3, and 4 (which comprise the remaining 1.5 Kbytes of code). 3. For every page read, perform error correction in SW. 4. Continue normal execution. **Fix Status:** No fix solution is planned.	1L45X 2L45X 0M55B 1M55B M55B

Table 1. Silicon Errata to MC9328MX21 and MC94MX21 (continued)

Erratum Number	Erratum Description	Details/Impact, Workaround, and Fix Status	Mask
19.	**Module:** DMA **Failure:** The DMA DISR register may be cleared accidentally when trying to clear any interrupt in the DISR register	**Details:** When doing single or multiple DMA transfers the action of clearing a single DMA bit from the DISR register can result in clearing the whole DISR register. **Impact:** If the DISR register cleared accidentally, then an interrupt for DMA transfers does not take place. This can be an issue when there are multiple DMA channels transferring data at the same time. The Interrupt Service routine can miss interrupt notifications that DMA transfers have happened. **Workaround:** Do not access the DISR register to clear DMA transfer interrupts. Instead clear the interrupt of each DMA being used by setting the SMOD bits of the DMA CCR register for the DMA channel being used. **Software Example:** `// pointer to 32bit program register DMA_CCR0` `volatile unsigned int * P_32_DMA_CCR0 ;` `int  tmp ;` `// save the old value of CCR` `tmp = *(P_32_DMA_CCR0+(0x40*channelID)) ;` `//Force DMA channel's source mode as reserved "11" to clear the DISR bit for the selected channel` `* (P_32_DMA_CCR0+(0x40*channelID)) = tmp	(0x3<<10);`  `// restore the old value back into CCR` `* (P_32_DMA_CCR0+(0x40*channelID)) = tmp;`	1L45X 2L45X 0M55B 1M55B M55B
20.	**Module:** UART, GPT, PWM, SDHC, CSPI, LCDC, CSI **Failure:** The module may fail when it is used with a high MPLL frequency.	**Details:** Clock control bits related to PERCLK[1:4] in PCCR0 and PCCR1 registers toggle causes the clock delay that makes the cross clock (PERCLK[1:4] and IPG_CLK) domain logic's behavior not as expected. **Workaround:** Follow up the recommended PLL setting (Table 6-7 in the reference manual) or keep the clock control bits related to PERCLK[1:4] in PCCR0 and PCCR1 registers no change when using MPLL > 288 MHz. **Fix Status:** No fix solution is planned.	

Table 1. Silicon Errata to MC9328MX21 and MC94MX21 (continued)

Erratum Number	Erratum Description	Details/Impact, Workaround, and Fix Status	Mask
21.	**Module:** LCDC **Failure:** LSCLK is missing.	**Details:** In 4 bpp, 8 bpp, 18 bpp, and TFT modes, LSCLK is missed in these conditions: • One clock cycle before every OE_ACD assert timing • Every VSYNC rising timing • Every VSYNC falling timing **Impact:** If the user connects LSCLK directly with LCD panel and the LCD panel allows missing clock, there is no issue. However, if the user adds a serializer between LSCLK and LCD panel, the serializer may not work correctly because of the missing clock and the LCD panel may have noise. **Workaround:** Connect LSCLK directly with the LCD panel, if the LCD panel allows it. **Fix Status:** No fix solution is planned.	

Revision History

Rev. 6 of this document adds errata 20 and 21.

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