Mask Set Errata for Mask 2M44C

Introduction

This mask set errata applies to the mask 2M44C for these products:

- MC9RS08KA2
- MC9RS08KA1

MCU Device Mask Set Identification

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 2M44C. All standard devices are marked with a mask set number and a date code.

MC9S08KA2 Startup

SE136-KA2START

Description

The MC9RS08KA2 may not commence execution of code consistently under certain power-up conditions. The behavior is dependent upon the power supply voltage starting point and ramp rate. These depend on several variables, including voltage and temperature and show some part-to-part variation.

This issue will be fixed in the next version of silicon.

Case 1 If there is a pullup on PTA0 when V_{DD} of the MC9RS08KA2 is driven with a very slow and nonlinear power-up sequence, the part can enter a non-functional static condition where the MCU is not executing code.

An example waveform is shown in Figure 1.

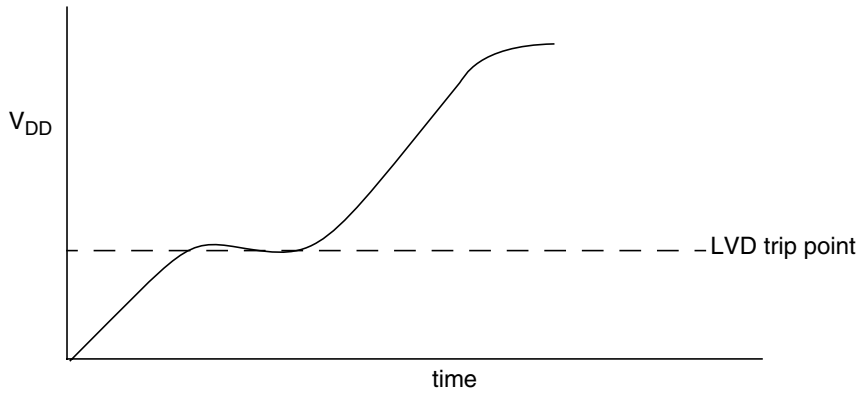

Figure 1. Observed Slow and Nonlinear V_{DD} Ramp

Case 2 It has been observed that when V_{DD} of the MCU is driven with a voltage ramp of 1.5 V/ms to 2.0 V/ms from a residual voltage on V_{DD} between 0.2 to 0.5 V, the MCU begins to execute code and enters one of two states.

a) If LVD is enabled (default), the part will repeatedly start to run code followed by a reset from the LVD.

b) If LVD is disabled by the user code, the code will run only for a short time and then stall.

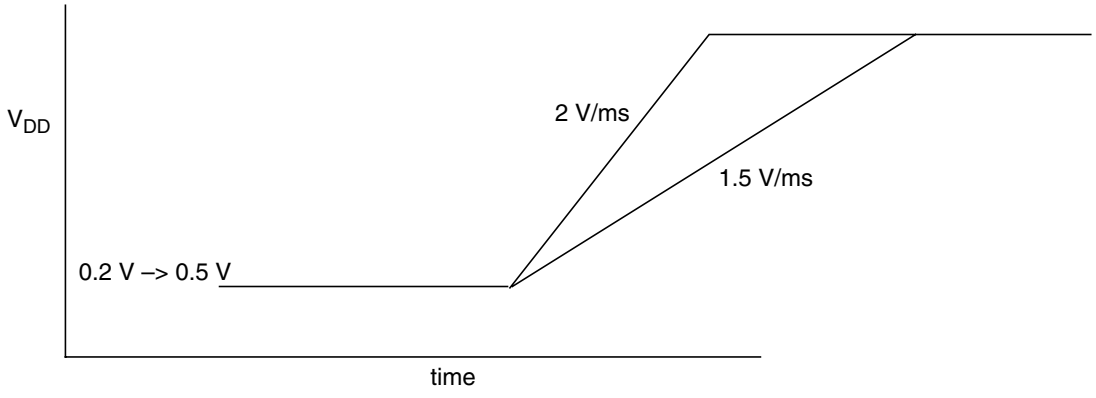

Figure 2. Observed V_{DD} Ramp Conditions that Cause Inconsistent Startup

Workarounds

There are two suggested workarounds. The first is to ensure that PTA0 is low until the voltage on V_{DD} is above a level of 2.4 V. This can be accomplished with a pulldown on the pin or a small capacitor to slow the rise of the PTA0 pin during power up.

The second workaround is to not allow a residual voltage between 0.2 to 0.5 V on V_{DD} followed by a ramp of V_{DD} from 1.5 V/ms to 2 V/ms. The addition of a discharge resistor in parallel with the bypass capacitors will allow the V_{DD} to be discharged. The specific component values to use depend upon the circuit's operation during V_{DD} ramp conditions.

A faster rise time on V_{DD}, faster than 2 V/ms, can prevent both of the issues.

ICS V1 Can Cause a Very Short Clock Pulse

SE128A-ICSV1

Description

The ICS module V1 — when configured with the FLL enabled and with BDIV set to divide-by one — can sometimes produce a very short clock pulse. This short clock pulse can cause the device to malfunction. The short clock pulse is caused when the digitally controlled oscillator (DCO) crosses a filter value boundary when compensating for output frequency error. The filter value is not in the memory map and cannot be read by user code.

- When operating from the internal reference clock, certain trim values can cause the error more often. The trim value for any particular clock frequency is unique to each device.
- The temperature coefficient of the DCO is such that the unique reference frequency causing the error, either internally or externally generated, will not be constant over temperature.

Workarounds

- If using FLL enabled with internal reference (FEI) or FLL enabled with external reference (FEE) modes, operate the device with a bus frequency equal to or below 5 MHz. This is accomplished by setting BDIV divide-by value to two or higher (BDIV[1,0] bit field value of 01, 10 or 11).
- Use the ICS in any of the modes with the FLL disabled. This includes: FLL bypassed internal (FBI), FLL bypassed internal low power (FBILP), FLL bypassed external (FBI), FLL bypassed external low power (FBELP) modes. (Not all devices have EXTAL and XTAL pins available to run the device with an external reference.)
