Mask Set Errata for Mask 0M80N

Introduction

This report applies to mask 0M80N for these products:

- MC9S08QB8
- MC9S08QB4

SE184-FLVD-STOP3: False low voltage detect when exiting stop3

Errata type:	Silicon
Affected component:	SoC level behavior
Description:	If the low voltage detect (LVD) is enabled (LVDE = 1) but not in stop mode (LVDSE = 0), on some devices the low voltage detect flag (LVDF) will occasionally be set when exiting stop3 mode. If the LVD interrupt is enabled (LVDIE = 1) the interrupt vector will be fetched. If the LVD reset is enabled, the part will reset, and the LVD bit in the System Reset Status (SRS) register will be set. The correct operation of the device is to wake and execute the code immediately after the STOP instruction. If the LVD is not enabled (LVDE = 0) or if LVD is also enabled during stop mode (LVDSE = 1) then this issue will not occur. If the LVD is enabled during stop mode the stop3 current will increase.
Workaround:	A software level change to reliably eliminate the issue is to use only the LVD interrupt (LVDE = 1, LVDIE = 1, and LVDRE = 0). Inside the LVD interrupt service routine, a short state of health check can be made to verify the supply level before proceeding. In this routine, the LVDF should be cleared and then read to determine whether a true low voltage event is present. If the LVDF is set when it is read, then a true LVD condition exists and the MCU can be reset by forcing the execution of an illegal op-code.

SE156-ADC-COCO: COCO bit may not get cleared when ADCSC1 is written to

Errata type:	Silicon

Affected component: ADC

Description: If an ADC conversion is near completion when the ADC Status and Control 1 Register (ADCSC1) is written to (i.e., to change channels), it is possible for the conversion to complete, setting the COCO bit, before the write instruction is fully executed. In this scenario, the write may not clear the COCO bit, and the data in the ADC Result register (ADCR) will be that of the recently completed conversion.

If interrupts are enabled, then the interrupt vector will be taken immediately following the write to the ADCSC1 register.

Workaround: It is recommended when writing to the ADCSC1 to change channels or stop continuous conversion, that you write to the register twice. The first time should be to turn the ADC off and disable interrupts, and the second should be to select the mode/channel and re-enable the interrupts.

SE157-ADC-INCORRECT-DATA: Boundary case may result in incorrect data being read in 10- and 12-bit modes

Errata type: Silicon

Affected component: ADC

Description: In normal 10-bit or 12-bit operation of the ADC, the coherency mechanism will freeze the conversion data such that when the high byte of data is read, the low byte of data is frozen, ensuring that the high and low bytes represent result data from the same conversion.

In the errata case, there is a single-cylce (bus clock) window per conversion cycle when a high byte may be read on the same cycle that subsequent a conversion is completing. Although extremely rare due to the precise timing required, in this case, it is possible that the data transfer occurs, and the low byte read may be from the most recently completed conversion.

In systems where the ADC is running off the bus clock, and the data is read immediately upon completion of the conversion, the errata will not occur. Also, in single conversion mode, if the data is read prior to starting a new conversion, then the errata will not occur.

The errata does not impact 8-bit operation.

Introducing significant delay between the conversion completion and reading the data, while a following conversion is executing/pending, could increase the probability for the errata to occur. Nested interrupts, significant differences between the bus clock and the ADC clock , and not handling the result register reads consecutively, can increase the delay and therefore the probability of the errata occuring.

Workaround: Using the device in 8-bit mode will eliminate the possibility of the errata occuring.

Using the ADC in single conversion mode, and reading the data register prior to initiating a subsequent conversion will eliminate the possibility of the errata occuring.

Minimizing the delay between conversion complete and processing the data can minimize the risk of the errata occuring. Disabling interrupts on higher priority modules and avoiding nested interrupts can reduce possible

contentions that may delay the time from completing a conversion and handling the data. Additionally, increasing the bus frequency when running the ADC off the asynchronous clock, may reduce the delay from conversion complete to handling of the data.

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