MSE9S08SG32_0M07J
Rev. 2, 1/2008

Mask Set Errata for Mask 0M07J

Introduction

This mask set errata applies to the mask 0M07J for these products:

- MC9S08SG32

MCU Device Mask Set Identification

The mask set is identified by a 5-character code consisting of a version number, a letter, two numerical digits, and a letter, for example 0M07J. All standard devices are marked with a mask set number and a date code.

Ganged Output Drive Control Register is not one-time writable

SE147-GNGC

Description

The ganged output drive control register (GNGC) is intended to be a write once register that enables the ganged output to take over up to 8 pins, enabling them as outputs and tying their data, drive strength, and slew rate control to PTC0 control bits. In normal usage, these pins would be shorted externally to be able to drive higher mA currents to an external component (i.e., H-bridge).

For this maskset, the ganged port control register can be written more than once.

In the scenario of code runaway, it might be possible to overwrite this register, relinquishing control of certain pins back to their respective control bits (i.e., PTCD_PTCD1, PTCDD_PTCDD1, PTCDS_PTCDS1, etc). In this scenario, depending on what is in those control bits for the shorted pins, it is possible to end up with shorted output trying to drive different logic levels. This may result in a large current short, that could lead to damage of the MCU.

Workaround

Assuming user code avoids improperly configuring pins, this condition would be caused by code runaway. As such, proper precautions need to be taken to protect against code runaway and minimize any stresses on the part or application failures.

The COP/watchdog timer should be used to reset the part in the instance of code runaway. And, the LVD should be used to ensure device integrity with proper operating voltage.

Additionally, stress to the MCU can be minimized by configuring any shorted ganged ports as inputs when not controlled by the ganged output. This way, if runaway code affects the GNGC register, any outputs will be driving inputs, as opposed to outputs.

ICS Internal Reference Can Remain Enabled in Stop3 Mode

SE143-ICS

Description

When transitioning from FEI or FBI modes to FEE or FBE modes, the internal reference clock may remain active in stop3 mode if the STOP instruction is executed soon after the IREFST bit in the ICSSC register clears. This can lead to elevated stop3 I_{DD}.

Workarounds

To ensure the internal reference clock is disabled before entering stop3, wait three internal reference clock periods after the IREFST bit has cleared before entering stop3. On a device with a trimmed internal reference, one period will be between 25.6 µs and 32 µs, therefore waiting 100 µs is adequate for all trimmed devices.

Or

To ensure the internal reference clock is disabled before entering stop3, transition into FEE mode and wait until the LOCK status bit indicates the FLL has attained lock before entering stop3 or transitioning into FBE mode and entering stop3.

TPM — TPM2CH1 Pin Reassignment Error

SE137-TPM

Description

An error was discovered in the logic that is used to reassign the TPM2CH1 output function to the PTA7 pin instead of the default PTB4 pin. When the T2CH1PS control bit in the SOPT2 control register is 0 (its default reset value), PTB4, PTA7, and TPM2CH1 pin functions operate as expected. When T2CH1PS is set to 1, TPM2CH1 output pin functions control (appear on) PTA7 as expected, but TPM2CH1 output functions also appear on the PTB4 pin so PTB4 is not free to be used for other functions. The usual reason for selecting T2CH1PS = 1 would be to move the timer 2 channel 1 pin functions from the PTB4 pin to the PTA7 pin so PTB4 can be used for one of the other shared pin functions on PTB4 (MISO function for the SPI module). In less common cases, the reassignment may be done to simplify printed circuit board layout and the PTB4 pin might not be needed in the system.

Workarounds

If TPM2CH1 is not used, is used in input capture mode (MS2B = MS2A = 0), is used as a software output compare (EDG2B = EDG2A = 0), or is assigned to PTB4 (T2CH1PS = 0), no workaround is needed.

If T2CH1PS = 1 and TPM2CH1 is configured for PWM (MS2B or CPWMS = 1) or hardware output compare (MS2B:MS2A = 0:1 and EDG2B:EDG2A not equal 0:0), the TPM2CH1 output pin signals appear on both PTB4 and PTA7 so alternate pin functions on PTB4 are not available.

Unexpected Flash Block Protection Errors

SE133-FLASH

Description

If a portion of the nonvolatile memory (NVM) is block protected, unexpected flash block protect violation (FPVIOL) errors can result. These errors can occur during an attempt to program or erase locations in areas of the NVM that are not block protected. Software methods can be used to avoid this potential problem. The problem is more likely to be seen on devices that have multiple nonvolatile blocks, including devices with two or more separate flash blocks or with flash plus EEPROM. If block protection is not enabled, no errors occur.

This error is related to logic that compares current block protection settings to an internally latched address. This internal address is written (latched) at reset, at the end of most flash commands, and whenever there is a write to a location in NVM. If a read access to the partially protected NVM is performed immediately before the write to unprotected memory that starts a new flash command, the erroneous address that was previously in the internal latch can cause a false indication of a protection violation. A short sequence of instructions can be performed before starting normal flash commands to ensure that the address in the internal latch is not a protected address.

Workarounds

The preferred workaround starts a command to a known unprotected address (which internally latches the known-unprotected address), forces an access error to abort that command, and then clears the resulting error flags before starting any new flash command. This workaround assumes the H:X index register points to the location or sector you want to program or erase, and accumulator A has the data value you plan to write to that location. Start your program or erase routine with the following instructions.

```
STA     ,X      ;latch the unprotected address from H:X
NOP             ;brief delay to allow the command state machine to start
STA     ,X      ;intentionally cause an access error to abort this command
PSHA            ;temporarily save data value
LDA     #$30    ;1's in PVIOL and ACCERR bit positions
STA     FSTAT   ;clear any error flags
PULA            ;restore data value
STA     ,X      ;STEP 1 write data to start new command
```

The only new instructions compared to the normal routine for flash commands are the first three instructions, which take three bytes of code space and five bus cycles. These instructions may be located anywhere in memory, including in the protected area of the flash memory.

ICS V2 Can Cause a Very Short Clock Pulse

SE128B-ICSV2

Description

The ICS module V2 — when configured with the FLL enabled and with BDIV set to divide-by one — can sometimes produce a very short clock pulse. This short clock pulse can cause the device to malfunction, causing illegal address or illegal opcode resets. The short clock pulse is caused when the digitally controlled oscillator (DCO) is switching between certain input values as it continually reacts to the output frequency error.

- When operating from the internal reference clock, certain trim values can cause the error more often. The trim value for any particular clock frequency is unique to each device.
- The temperature coefficient of the DCO is such that the unique reference frequency causing the error, either internally or externally generated, will not be constant over temperature.

Workaround

- If using FLL enabled with internal reference (FEI) or FLL enabled with external reference (FEE) modes, operate the device with a bus frequency equal to or below 10 MHz. This is accomplished by setting BDIV divide-by value to two or higher (BDIV[1,0] bit field value of 01, 10 or 11).
- Use the ICS in any of the modes with the FLL disabled. This includes: FLL bypassed internal (FBI), FLL bypassed internal low power (FBILP), FLL bypassed external (FBI), FLL bypassed external low power (FBELP) modes. (Not all devices have EXTAL and XTAL pins available to run the device with an external reference.)