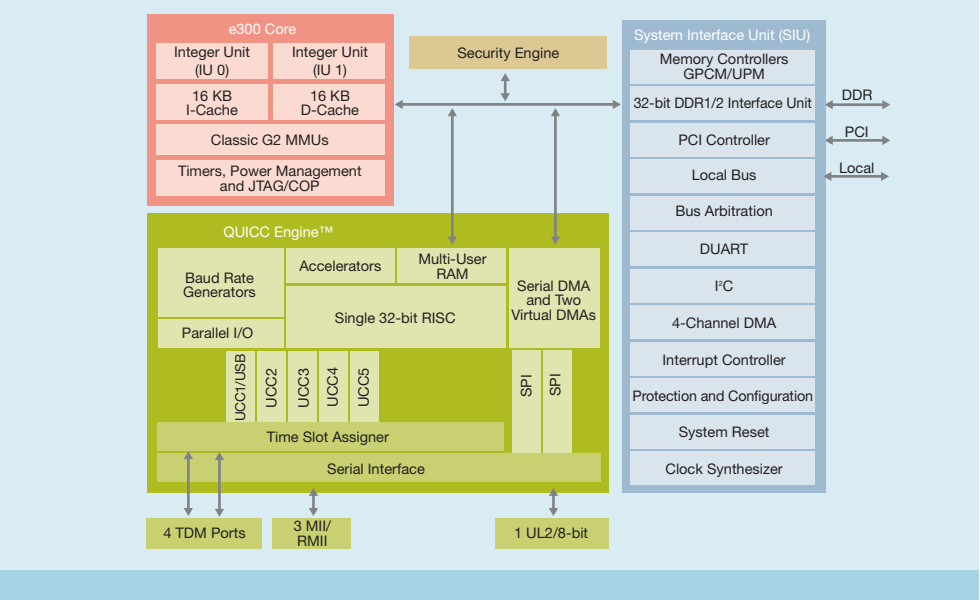
MPC8323E Family PowerQUICC™ II Pro

The cost-effective MPC8323E communications processor family that includes the MPC8323E, MPC8323, MPC8321E and MPC8321 meets the requirements of several small office/home office (SOHO), access, IP services and industrial control applications. It provides better CPU performance, additional functionality and faster interfaces than current PowerQUICC™ II processors while addressing important time to market, price, power consumption and board space requirements.

MPC8323E Block Diagram



Core Complex

The MPC8323E family incorporates a unique configuration of the e300 (MPC603e-based) core. This configuration has been designed to include dual integer units as well as a modified multiply instruction. These architectural enhancements enable more efficient operations to be executed in parallel, resulting in a significant performance improvement. The e300 core complex also includes 16 KB of L1 instruction and data caches and on-chip memory management units (MMUs).

QUICC Engine™ Technology

A new single-RISC version of the QUICC Engine subsystem communications engine forms the heart of the networking capability of the MPC8323E. The QUICC Engine subsystem contains several peripheral controllers and a single 32-bit reduced instruction set computing (RISC) controller. Unique microcode packages provide support for NAT, Firewall, IPSec and Advanced Quality of Service (QoS). Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs).

Each of the five UCCs can support a variety of communication protocols:

- 10/100 Mbps Ethernet
- Asynchronous transfer mode (ATM) support up to OC-3 speeds
- Serial ATM
- Multi-physical layer (PHY) ATM
- Time division multiplexing (TDM)

In addition, the QUICC Engine subsystem can also support a Universal Test and Operations PHY Interface for ATM (UTOPIA) level 2 for up to 31 multi-PHY. UCC can also support USB 2.0 (full/low speed).

Hardware Security Engine

The security engine on the MPC8323E and MPC8321E allows CPU-intensive cryptographic operations to be off-loaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, Advanced Encryption Standard (AES), Secure Hash Algorithm (SHA)-1 and MD-5 algorithms.

System Interface Unit

The MPC8323E family also includes a 32-bit double data rate (DDR1/DDR2) memory controller, a 32-bit peripheral component interconnect (PCI) controller, a 16-bit local bus and four direct memory access (DMA) channels.

In summary, the MPC8323E family provides users with a highly integrated, fully programmable communications processor for use in many SOHO, access, IP services and industrial control applications. This helps ensure that a cost-effective system solution can be quickly developed and will offer flexibility to acommodate new standards and evolving system requirements.

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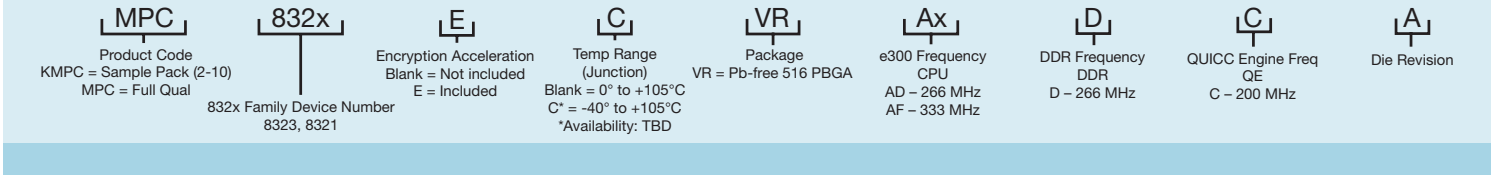

MPC8323E PowerQUICC™ II Pro Family	MPC8323E	MPC8323	MPC8321E	MPC8321
Core	e300	e300	e300	e300
I-Cache/D-Cache	16/16	16/16	16/16	16/16
Floating Point Unit	No	No	No	No
Core Frequency	266/333	266/333	266/333	266/333
QUICC Engine™ Subsystem	Single RISC	Single RISC	Single RISC	Single RISC
Memory Controller	32-bit DDR1/DDR2	32-bit DDR1/DDR2	32-bit DDR1/DDR2	32-bit DDR1/DDR2
Local Bus	16-bit; up to 66 MHz	16-bit; up to 66 MHz	16-bit; up to 66 MHz	16-bit; up to 66 MHz
PCI Interface	32-bit; up to 66 MHz	32-bit; up to 66 MHz	32-bit; up to 66 MHz	32-bit; up to 66 MHz
Ethernet	(3) 10/100; MII/RMII	(3) 10/100; MII/RMII	(3) 10/100; MII/RMII	(3) 10/100; MII/RMII
USB 2.0	Full/low speed	Full/low speed	Full/low speed	Full/low speed
Integrated Security	Yes	No	Yes	No
DUART	Yes	Yes	Yes	Yes
I^2C Controller	Yes	Yes	Yes	Yes
SPI	Dual	Dual	Dual	Dual
Interrupt Controller	Yes	Yes	Yes	Yes
ATM	Yes	Yes	No	No
Package	516-PBGA	516-PBGA	516-PBGA	516-PBGA

Typical Application

- Residential gateways
- SOHO networking
- VPN routers
- Access points
- DSLAM line cards
- Industrial control
- Test and measurement equipment

MPC8323E Features

- High-performance, low power and cost-effective communications processor
- The e300 core built on Power Architecture™ technology with dual integer units enables more efficient operations to be conducted in parallel, resulting in significant performance improvement
- The single-RISC QUICC Engine communications module offers a future-proof solution for next-generation designs by supporting programmable protocol termination and network interface termination to meet evolving protocol standards
- Single platform architecture supports the convergence of IP packet networks and ATM networks
- DDR1/DDR2 memory controller—one 32-bit interface at up to 266 MHz
- Peripheral interfaces such as 32-bit, 66 MHz PCI, 16-bit, 66 MHz local bus interface and USB 2.0 (full/low speed)
- Security engine provides acceleration for control and data plane security protocols
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration

QUICC Engine Technology

- Single 32-bit RISC controller for flexible support of communications peripherals
- Serial DMA channel for receive and transmit on all serial channels
- Five UCCs supporting the following interfaces (not all of them simultaneously):
  - ATM protocol through UTOPIA interface supporting 31 multi PHYs
  - HDLC/transparent up to 70 Mbps full duplex
  - QUICC multi-channel controller (QMC) for 64 time division multiplexing (TDM) channels

The UCCs are similar to the PowerQUICC II peripherals: serial communications controller (SCC) (BISYNC, UART and HDLC bus) and fast serial communications controller (FCC) (fast Ethernet, HDLC, transparent and ATM).

Learn More: For current information about Freescale products and documentation, please visit **www.freescale.com**.

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