BUILT ON Power

QorIQ Multicore Processor Development

QorIQ P5020 Development System

Overview

The QorIQ P5020DS is a flexible development system based on the dual-core 32/64-bit moded P5020 device. The board, with its 2.0 GHz P5020 and rich I/O mix, is intended for evaluation of the QorIQ P5020/P5010 processor in networking, telecom and industrial applications, where its high-performance, high-efficiency core and integration make it very well suited as a control plane processor.

The P5020 development system, which exercises most capabilities of the P5020 processor, can serve as a reference for the customer's own hardware development, as a debug tool to check behaviors on the board compared to behaviors seen on customer boards or be used for software development and performance evaluation prior to completion of the customer's own board.

The P5020/P5010 processors are based upon the e5500 core, built on Power Architecture® technology, offering speeds of 1.6 to 2.0 GHz. They feature a three-level cache hierarchy with 32 KB of instruction and data cache per core, 512 KB of unified backside L2 cache per core, and 2 MB of shared frontside CoreNet platform cache fronting the dual memory controllers. The I/O includes 18 SerDes lanes running at up to 5 GHz, multiplexed across four PCI Express® gen. 2.0 controllers, one 10 GE XAUI interface, four 1 GbE SGMII interfaces, two Serial RapidIO® (version 1.3 with features of version 2.1) interfaces, four 2.5 Gb/s SGMII interfaces, two SATA 2.0 interfaces and the high-speed Aurora debug interface. They include a 64-bit DDR3 and DDR3L (low power) DRAM interface with 8-bit ECC support running at up to 1333 MT/s data rate. It includes two USB 2.0 interfaces (including PHY), two DUARTs, an SD/MMC interface, a 32-bit local bus, four I^2C and SPI. Both processors also include the accelerator blocks collectively known as the Data Path Acceleration Architecture (DPAA) that offload packet handling, pattern matching and security algorithm calculation from the core as well as support for RAID 5/6 hardware assist.

The P5020DS has significant flexibility in allocation of its 18 SerDes lanes to various functions. Its base configuration supports two RGMII ports, two PCI Express x2 slots (two lanes to each slot), 4 x 4 slots for the optional Freescale SGMII-PEX-RISER, a 2 x 4 slot for the optional Freescale XAUI-RISER, the Aurora high-speed debug port and two SATA ports. It can also be configured to support one PCI Express slot of widths up to x8 (at 2.5 Gb/s).

The dual memory controllers of the P5020DS support 4 GB of DDR3 at 1333 MT/s. It has 128 MB of NOR flash, 1 GB NAND flash, 256 KB IC EEPROM and two SPI memories: 16 MB flash and 128 KB EEPROM. It also has two USB 2.0 receptacles and an SD card slot.

The P5020DS is pre-loaded with a software development kit with support for DPAA, including SMP Linux® kernel, Hugetlbfs for applications with a large memory footprint, user space DPAA for high-performance packet handling, u-boot and a GCC toolchain.

freescale™ QorIQ

QorIQ P5020DS Board Features

Processor

- P5020, 2.0 GHz core with 1333 MT/s DDR3 data rate
- Multiple SysClk inputs for generating various device frequencies

Memory

- Dual unbuffered DDR3 240-pin uDIMM modules with ECC (72-bit bus), 4 GB memory, 1333 MT/s data rate
- 128 MB NOR flash
- 1 GB NAND flash
- SPI-based 128 MB flash
- SPI-based 128 KB EEPROM
- SD connector to interface with an SD memory card

PCI Express

- Two x2 PCI Express slots
- Can support the Freescale XAUI-RISER and SGMII-PEX-RISER option cards

SATA

- Two vertical SATA connectors

USB 2.0

- Two Full-Speed USB controllers
- One Type A and one MicroAB receptacle

Ethernet

- Support two 10/100/1000 ports with no add-in cards
- dTSEC4 and dTSEC5 as RGMII to Vitesse VSC8244 PHY
- Optional SGMII-PEX-RISER expands 10/100/1000 port count to five
- 10 GE supported with optional XAUI-RISER card

DUART

- Two DUARTs

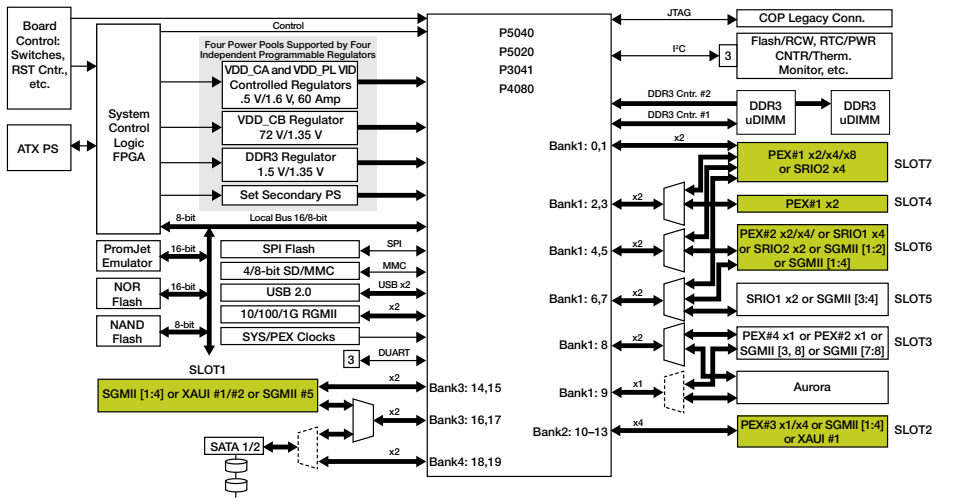
Debug

- JTAG/COP
- Aurora high-speed connector

Other

- IEEE® 1588 connector for Symmetricom option card
- Temperature sensor
- Eight general-purpose I/Os

QorIQ P5020DS Block Diagram



For more information, visit freescale.com/QorIQ

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