S32R41 RADAR MCU – HIGH PERFORMANCE FOR HIGH RESOLUTION RADAR

S32R41 is a radar microprocessor unit (MPU) dedicated to advanced 77 GHz Radar applications. The architecture features Arm® Cortex®-A53 and Cortex-M7 cores which are combined with radar processing accelerators (SPT and BBE) to create an optimal radar processing chain. It is designed to target the ADAS radar market, and is also suitable for industrial and consumer radar applications. The comprehensive feature set enables the S32R41 family to span the radar application space. The high performance processing in combination with Dual MIPI CSI2 interfaces and 8 MB of local SRAM enable 4D high resolution radar systems. The S32R41 also matches advanced corner and long range front radar applications.

KEY FEATURES

- Cortex-A53 @800 MHz,
- 2 Cortex-M7 lockstep pairs @400 MHz
- SPT 3.5 @600 MHz
- BBE32 DSP @600 MHz
- 8 MB SRAM with ECC
- HSE Security module
- 1x SAR ADC 8-channel
- 2x MIPI CSI2
- 2x Ethernet interfaces, 1x RGMII (1000 Mbps), 1x RMII (100 Mbps)
- 2x FlexCAN with FD
- ISO 26262 SEooC ASIL B(D)
- -40 °C to 150 °C (Tj) AEC-Q100 Grade-1
- 297-ball FCBGA, 11 x 11 mm

TARGET APPLICATIONS

- Automotive High Resolution Radar
- Adaptive Cruise Control
- Autonomous Emergency Braking
- Blind Spot Detection
- Front/Rear Cross-traffic-functions
- Lane Change Assistance
- Park Assist
- Reverse-AEB
- Zonal Architecture

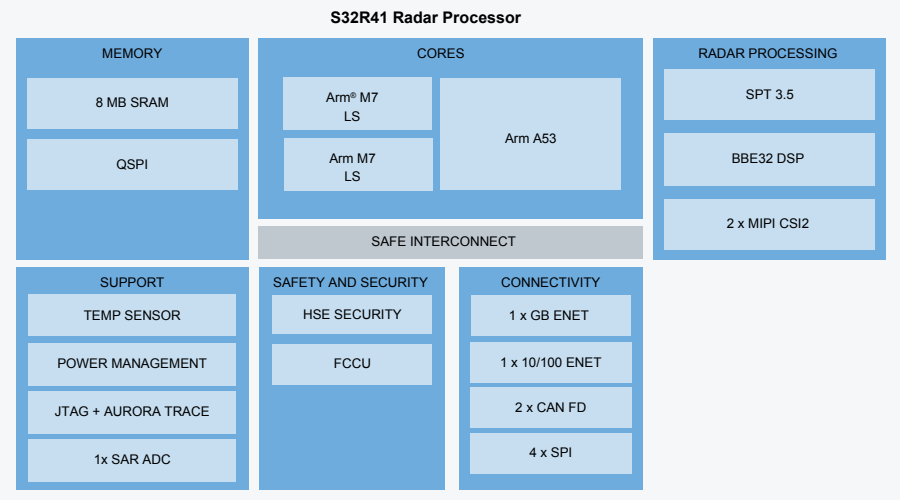
RELATED RADAR PRODUCTS

- S32R45: S32R Radar MPU – High Performance for Imaging Radar
- TEF82xx: Fully Integrated 77 GHz RFCMOS Automotive Radar Transceiver
- PF5103: Multi-Channel (5) PMIC for Automotive Applications: 3 LVBUCK and 2 LDO, Fit for ASIL-B/D Safety Level
- TJA1462: CAN Signal Improvement Capability Transceiver with Standby Mode
- TJA1103A: ASIL B Compliant 100BASE-T1 Ethernet PHY

SOFTWARE AND TOOLS

- AUTOSAR® MCAL4.4
- HSE firmware
- Safety SDK
- Inter-process communication framework
- Linux® BSP
- Platform SDK M7
- RADAR SDK
- S32 Design Studio
- S32 compilers (GCC, Windriver)
- S32 RADAR QKIT RTM
- Debuggers (Lauterbach, NXP and GHS)

S32R41 RADAR PROCESSOR BLOCK DIAGRAM



BENEFITS

- SPT 3.5 provides performance increase over SPT 2.8
- BBE32 DSP with VFPU provides new radar post processing capabilities
- Large SRAM memory support for significantly increased radar data and algorithm software
- Support up to two cascaded transceivers for advanced high resolution Radar
  - Optimized architecture to support high throughput needed for cascaded transceiver sensors
- Functional Safety
- Architecture supports up to functional safety level ASIL D
- Software enablement
- Extensive Radar SDK with enablement for advanced radar and fusion processing algorithms
- Security: HSE provides OTA update capability and ISO 21434 ready

SOFTWARE ENABLEMENT

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SECURITY

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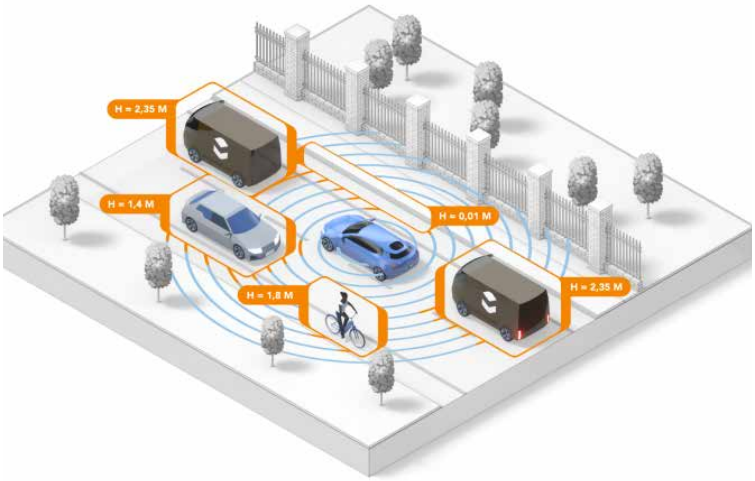

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