Document Number:KLX3PB
Rev 1, 08/2014

KLx3 Product Brief

Supports all KLx3 devices

Contents

1 KLx3 family introduction

The device is highly-integrated, market leading ultra low-power 32-bit microcontroller based on the enhanced Cortex-M0+ (CM0+) core platform. The features of the KLx3 family derivatives are as follows.

- Core platform clock up to 48 MHz, bus clock up to 24 MHz.
- Memory option is up to 256 KB Flash and 32 KB RAM
- Wide operating voltage ranges from 1.71–3.6 V with fully functional flash program/erase/read operations
- Multiple package options from 64 LQFP and 64 MAPBGA
- Ambient operating temperature ranges from –40 °C to 85 °C for WLCSP package and –40 °C to 105 °C for all the others.

The family acts as an ultra low-power, cost-effective microcontroller to provide developers an appropriate entry-level 32-bit solution. The family is the next-generation MCU solution for low-cost, low-power, high-performance devices applications. It's valuable for cost-sensitive, portable applications requiring long battery life-time.

For further information on other Kinetis family products please go to freescale.com/kinetis.

2 Key features

Core
- ARM® Cortex®-M0+ core up to 48 MHz

Memories
- Up to 256 KB program flash memory
- Up to 32 KB SRAM
- 16KB ROM with built-in bootloader
- 32 Byte Register File

System peripherals
- 4-channel DMA controller
- Watchdog
- Low-leakage wakeup unit
- SWD debug interface and Micro Trace Buffer
- Bit Manipulation Engine

Clocks
- 48 MHz high accuracy internal reference clock
- 32–40 kHz, or 3–32 MHz crystal oscillator
- 1 kHz LPO clock
- 8/2 MHz IRC

Operating Characteristics
- Voltage range: 1.71 to 3.6 V
- Temperature range: –40 to 105 °C

Human-machine interface
- Segment LCD controller supporting up to 28x8 or 32x4 24x8 or 28x4
- General-purpose input/output up to 54

Communication interfaces
- USB full-speed slave controller with on-chip transceiver and 5 V to 3.3 V regulator, supporting crystal-less recovery
- Two 16-bit SPI modules
- One UART module supporting ISO7816
- Two LPUART modules
- Two I2C modules supporting up to 1 Mbit/s
- One I2S (SAI) module
- One FlexIO module

Analog Modules
- 16-bit, 16-channel SAR ADC with internal voltage reference
- High-speed analog comparator containing a 6-bit DAC and programmable reference input
- One 12-bit DAC
- 1.2 V voltage reference (Vref)

Timers
- One 6-channel Timer/PWM module
- Two 2-channel Timer/PWM modules
- One low-power timer
- Periodic interrupt timer
- Real time clock

Security and integrity modules
- 80-bit unique identification number per chip

3 Block diagram

The following figure shows a superset block diagram of the device. Other devices within the family have a subset of the features.

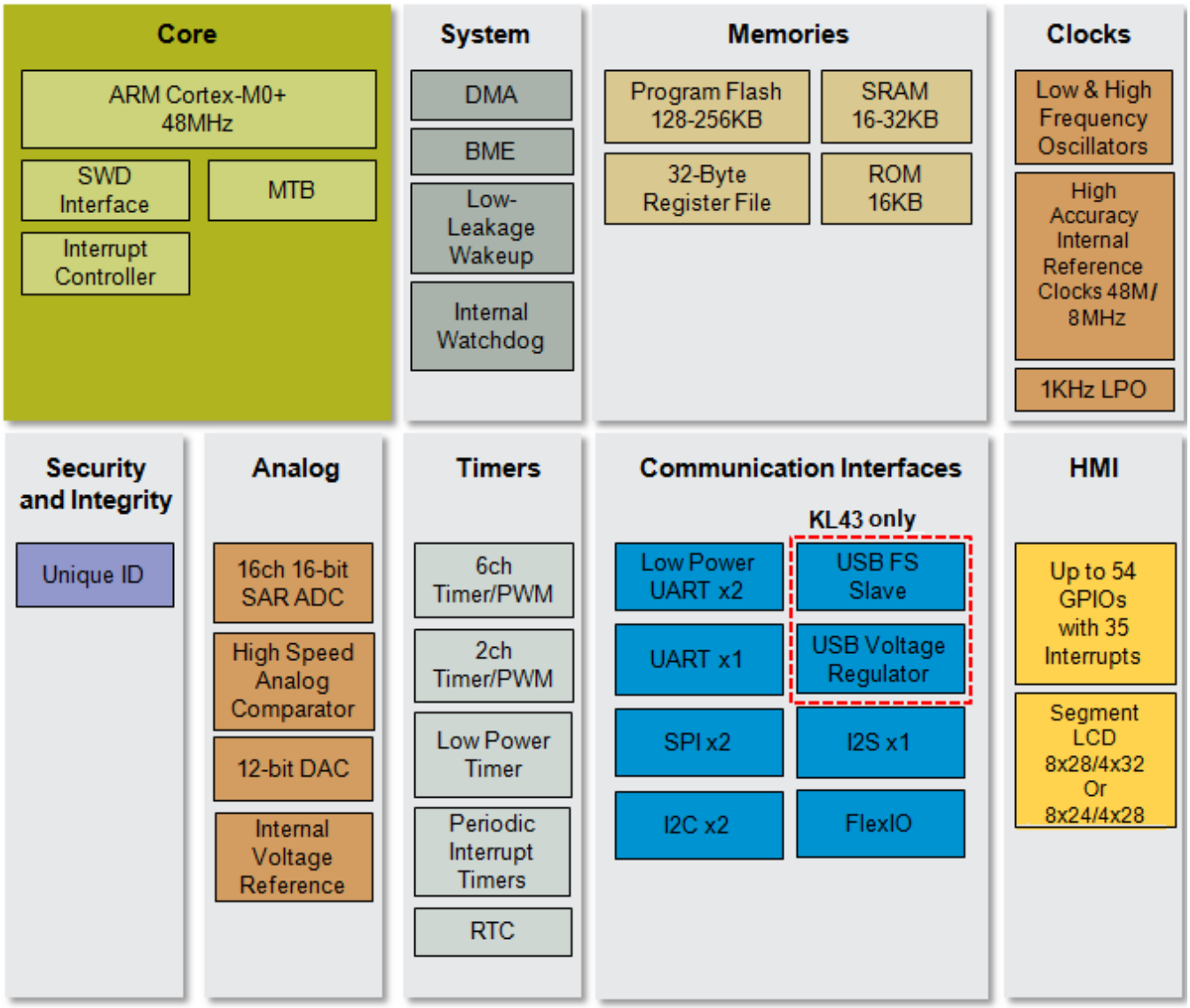

Figure 1. KLx3 Family Block Diagram

4 Features

4.1 High level feature comparison

Table 1. High level feature comparison

Features	Sub_Family	
	KL33	KL43
CPU Frequency	48 MHz	48 MHz
Flash Memory	up to 256 KB	up to 256 KB

Table continues on the next page...

Table 1. High level feature comparison (continued)

Features	Sub_Family	
	KL33	KL43
SRAM	up to 32 KB	up to 32 KB
USB Slave FS	—	Yes
USB Vreg	—	Yes
Segment LCD	Yes	Yes
64LQFP	Yes	Yes
64MAPBGA	Yes	Yes

4.2 Common features

Table 2. KL43/33 common features

Core/System Modules			Timers Modules	
Core	ARM Cortex-M0+		General Purpose Timer/PWM	1x6ch+2x2ch
CPU Frequency	48 MHz		Low Power Timer	
DMA	4 ch		PIT (32-bit)	1x2ch
Bit Manipulation Engine	Yes		RTC	Yes
Debug	SWD		Communication interface	
Trace	MTB		Low Power UART	2
Memories			UART w/ ISO7816-3	1
Flash	up to 256 KB		16-bit SPI	2
SRAM	up to 32 KB		I2C	2
ROM	16 KB		I2S	1
Register File	32 Byte		FlexIO	1
Clock Modules			USB Slave FS[1]	1
MCG-Lite	Yes		USB Vreg[1]	120 mA
Main OSC	32-40 kHz or 3-32MHz		Human Machine Interface	
48 MHz high accuracy IRC	Yes		Segment LCD	Yes
8/2MHz IRC	Yes		NMI	Yes
Security and Integrity			Total GPIOs	up to 54
Watchdog	Yes		GPIOs w/ Interrupt	up to 31
Analog Modules			High Current GPIOs	6
ADC	1x 16-bit SAR, up to 16 ch		Operating Characteristics	
Analog Comparator	1, 6-bit DAC, up to 6 channels		Voltage Range	1.71-3.6 V
12-bit DAC	1		Flash Write V	1.71-3.6 V
1.2V VREF	1		Temp Range	• -40 to 105 °C, or • -40 to 85 °C

1. It's only available on KL43.

4.3 Feature differences per package

Package	64LQFP	64MAPBGA
Flash	up to 256KB	up to 256KB
SRAM	up to 32KB	up to 32KB
Segment LCD	Yes	Yes
Total GPIOs	up to 54	up to 54
GPIOs w/ Interrupt	up to 31	up to 31
High Current GPIOs	6	6

4.4 Orderable part numbers

The following table summarizes the part numbers of the devices covered by this document. See the Part identification section for details on the part number format.

Table 4. Ordering Information

Part Number	Memory		Maximum number of I\O's
	Flash (KB)	SRAM (KB)	
MKL33Z128VLH4	128	16	54
MKL33Z256VLH4	256	32	54
MKL33Z128VMP4	128	16	54
MKL33Z256VMP4	256	32	54
MKL43Z128VLH4	128	16	50
MKL43Z256VLH4	256	32	50
MKL43Z128VMP4	128	16	50
MKL43Z256VMP4	256	32	50

4.5 Power modes

The Power Management Controller (PMC) provides multiple power options to allow the user to optimize power consumption for the level of functionality needed.

Depending on the stop requirements of the user application, a variety of stop modes are available that provide partial power-down or full power-down of certain logic and/or memory. I/O states are held in all modes of operation. The following table compares the various power modes available.

For each run mode, there is a corresponding Wait and Stop mode. Wait modes are similar to ARM Sleep modes. Stop modes (VLPS, STOP) are similar to ARM Sleep Deep mode. The Very Low Power Run (VLPR) operating mode can drastically reduce runtime power when the maximum bus frequency is not required to handle the application needs.

The three primary modes of operation are Run, Wait, and Stop. The WFI instruction invokes both Wait and Stop modes for the chip. The primary modes are augmented in a number of ways to provide lower power based on application needs.

Table 5. Chip power modes

Power mode	Description	Core mode	Recovery
RUN	RUN mode - 48MHz core/ 24MHz flash and bus, all peripheral clocks enabled, while (1) from flash	Run	—
RUN_CO	RUN mode in compute operation - 48MHz core/ 24MHz flash/bus clock disabled, while(1) from flash	Run	—
VLPR_CO	VLPR in compute operation - 4MHz core/0.8MHz flash/bus clock disabled, while (1) from flash	Run	—
WAIT	Core disabled/48MHz system/ 24MHz bus/flash disabled, all peripheral clocks disabled	Sleep	Interrupt
VLPW	Core disabled/4MHz system/ 0.8MHz bus/flash disabled, all peripheral clocks disabled	Sleep	Interrupt
STOP	Core/system/bus clock are all off, lowest power mode that retrains all registers, LVD on, peripherals clocks off, chip in static state	Deep Sleep	Interrupt
VLPS	Similar to STOP, with LVD off, lowest power mode with ADC and pin interrupts enabled	Deep Sleep	Interrupt
LLS	Most peripherals in state retention mode with clocks off (SRAM and IO retrained), OSC, LLWU, RTC, CMP, TSI can be used, NVIC off, LLWU to wake up.	Deep Sleep	Wakeup Interrupt
VLLS3	Similar to LLS, but reset flow is executed after waken up (causing long wake-up time), SRAM is retrained	Deep Sleep	Wakeup Reset
VLLS1	Similar to VLLS3, SRAM is not retrained, 32-byte system register file to maintain critical data	Deep Sleep	Wakeup Reset
VLLS0	Similar to VLLS1, LPO disabled, with POR circuit on/off	Deep Sleep	Wakeup Reset

4.6 Module-by-module feature list

The following sections describe the high-level module features for the family's superset device.

4.6.1 Core modules

4.6.1.1 ARM Cortex M0+ core

- Up to 48 MHz core frequency from 1.71 V to 3.6 V across temperature range of –40 °C to 105 °C
- Support up to 32 interrupt request sources
- 2-stage pipeline microarchitecture for reduced power consumption and improved architectural performance (cycles per instruction)
- Binary compatible instruction set architecture with the CM0 core
- Thumb instruction set combines high code density with 32-bit performance.
- Serial wire debug (SWD) reduces the number of pins required for debugging.
- Micro trace buffer (MTB) provides lightweight program trace capabilities using system RAM as the destination memory.
- Single cycle 32 bits by 32 bits multiply

4.6.1.2 Nested Vectored Interrupt Controller (NVIC)

- Up to 32 interrupt sources
- Includes a single nonmaskable interrupt

4.6.1.3 Wake-Up Interrupt Controller (WIC)

- Supports interrupt handling when system clocking is disabled in low-power modes
- Takes over and emulates the NVIC behavior when correctly primed by the NVIC on entry to Very-Deep-Sleep mode
- A rudimentary interrupt masking system with no prioritization logic signals for wake-up as soon as a nonmasked interrupt is detected.
- Contains no programmer’s model visible state and is therefore invisible to end users of the device other than through the benefits of reduced power consumption while sleeping

4.6.1.4 Debug Controller

- 2-pin serial wire debug (SWD) provides external debugger interface
- Micro trace buffer (MTB) provides simple execution trace capability and operates as a simple AHB-Lite SRAM controller.

4.6.2 System modules

4.6.2.1 Power Management Control Unit (PMC)

- Separate digital (regulated) and analog (referenced to digital) supply outputs
- Programmable power saving modes
- No output supply decoupling capacitors required

- Available wake-up from power saving modes via RTC and external inputs
- Integrated Power-on Reset (POR)
- Integrated Low Voltage Detect (LVD) with reset (brownout) capability
- Selectable LVD trip points
- Programmable Low Voltage Warning (LVW) interrupt capability
- Buffered bandgap reference voltage output
- Factory programmed trim for bandgap and LVD
- 1 kHz Low-Power Oscillator (LPO)

4.6.2.2 DMA Channel Multiplexer (DMA MUX)

- Four independently selectable DMA channel routers
- Two periodic trigger sources available
- Each channel router can be assigned to 1 of 63 possible peripheral DMA sources.

4.6.2.3 DMA Controller

Four independently programmable DMA controller channels provide the means to directly transfer data between system memory and I/O peripherals.

- DMA controller is capable of functioning in Run, Wait, Stop, and VLPS modes of operation.
- Dual-address transfers via 32-bit master connection to the system bus
- Data transfer in 8-, 16-, or 32-bit blocks
- Continuous-mode or cycle-steal transfers from software or peripheral initiation

4.6.2.4 COP Watchdog module

- Independent clock source input
- Choice between the following clock sources
  - LPO oscillator
  - Bus clock
  - IRC8M/2M
  - OSCERCLK

4.6.2.5 System clocks

- System Oscillator (OSC)—Loop-control pierce oscillator; crystal or ceramic resonator range of 32 kHz to 40 kHz (low range mode) or 3-32 MHz (high range mode)
- Multipurpose Clock Generator- Lite (MCG-Lite)
  - Internal reference clocks—Can be used as a clock source for other on-chip peripherals
    - 48 MHz high accuracy internal reference clock
    - 8/2 MHz low power internal reference clock
    - 1 kHz LPO clock

4.6.3 Memories and memory interfaces

4.6.3.1 On-chip memory

- 48 MHz performance devices
  - Up to 256 KB program flash memory
  - Up to 32 KB SRAM
  - 16 KB ROM with build-in bootloader
- Security circuitry to prevent unauthorized access to RAM and flash memory contents

4.6.4 Analog

4.6.4.1 Analog-to-Digital Converter (ADC)

- Linear successive approximation algorithm with up to 16-bit resolution
- Output modes:
- Single or continuous conversion
- Configurable sample time and conversion speed/power
- Conversion complete and hardware average complete flag and interrupt
- Input clock selectable from up to four sources
- Operation in low-power modes for lower noise operation
- Asynchronous clock source for lower noise operation with option to output the clock
- Selectable asynchronous hardware conversion trigger with hardware channel select
- Automatic compare with interrupt for various programmable values
- Temperature sensor
- Hardware average function
- Selectable voltage reference
- Self-calibration mode

4.6.4.2 High-Speed Analog Comparator (CMP)

- 6-bit DAC programmable reference generator output
- Up to six selectable comparator inputs; each input can be compared with any input by any polarity sequence
- Selectable interrupt on rising-edge, falling-edge, or either rising or falling edges of the comparator output
- Comparator output supports:
  - Sampled
  - Windowed (ideal for certain PWM zero-crossing-detection applications
  - Digitally filtered using external sample signal or scaled peripheral clock
- Two performance modes:
  - Shorter propagation delay at the expense of higher power
  - Low power, with longer propagation delay
- Operational in all MCU power modes except for VLLS0

4.6.4.3 12-bit Digital-to-Analog Converter (DAC)

- 12-bit resolution
- Guaranteed 6-sigma monotonicity over input word
- High- and low-speed conversions
  - 1 µs conversion rate for high speed, 2 µs for low speed
- Power-down mode
- Automatic mode allows the DAC to generate its own output waveforms including square, triangle, and sawtooth.
- Automatic mode allows programmable period, update rate, and range.
- DMA support

4.6.4.4 Voltage reference (VREF)

- Programmable trim register with 0.5 mV steps, automatically loaded with factory trimmed value upon reset
- Programmable buffer mode selection:
  - Off
  - Bandgap enabled/standby (output buffer disabled)
  - Low power buffer mode (output buffer enabled)
  - High power buffer mode (output buffer enabled)

- 1.2 V output at room temperature
- Output pin VREF_OUT, shared with normal VREFH

4.6.5 Timers

4.6.5.1 Low-Power Timer (LPTMR)

- 16-bit time counter or pulse counter with compare
  - Optional interrupt can generate asynchronous wakeup from any low-power mode
  - Hardware trigger output
  - Counter supports free-running mode or reset on compare
- Configurable clock source for prescaler/glitch filter
- Configurable input source for pulse counter
  - Rising-edge or falling-edge

4.6.5.2 Timer/PWM (TPM)

- Selectable source clock
- Programmable prescaler
- 16-bit counter supporting free-running or initial/final value, and counting is up or up-down
- Input capture, output compare, and edge-aligned and center-aligned PWM modes
- Generation of hardware triggers
- DMA support for TPM events

4.6.5.3 Periodic Interrupt Timers (PITs)

- Two general-purpose interrupt timers
- Two interrupt timers for triggering ADC conversions
- 32-bit counter resolution
- Clocked by bus clock frequency
- DMA support

4.6.5.4 Real-Time Clock (RTC)

- 32-bit seconds counter with 32-bit alarm
- 16-bit prescaler with compensation
- Register write protection
- Hard Lock requires MCU POR to enable write access

4.6.6 Communication interfaces

4.6.6.1 FlexIO

- The FlexIO module is capable of supporting a wide range of protocols including, but not limited to UART, I2C, SPI, I2S, PWM/Waveform generation.
- Array of 32-bit shift registers with transmit, receive and data match modes.
- Double buffered shifter operation for continuous data transfer.
- Shifter concatenation to support large transfer sizes.
- Automatic start/stop bit generation.
- Interrupt, DMA or polled transmit/receive operation.

- Programmable baud rates independent of bus clock frequency, with support for asynchronous operation during stop modes.
- Highly flexible 16-bit timers with support for a variety of internal or external trigger, reset, enable and disable conditions.

4.6.6.2 Inter-Integrated Circuit (I^2C)

- Compatible with I^2C bus standard and *SMBus Specification Version 2* features
- Up to 400 kbit/s with maximum bus loading
- Up to 1 Mbit/s operation with maximum bus loading
- Multimaster operation
- Software programmable for one of 64 different serial clock frequencies
- Programmable slave address and glitch input filter
- Interrupt or DMA driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Bus busy detection broadcast and 10-bit address extension
- Address matching causes wake-up when the processor is in low-power mode.

4.6.6.3 USB Module (FS)

- Complies with USB specification rev 2.0
- USB device mode
  - Full-speed operation via the on-chip transceiver
  - Supports one upstream facing port
  - Supports four programmable, bidirectional USB endpoints, including endpoint 0
- Suspend mode/low power
  - As host, firmware can suspend individual devices or the entire USB and disable chip clocks for low-power operation
  - Device supports low-power suspend
  - Remote wake-up supported for device
  - Integrated with the processor's low power modes
- Includes an on-chip full-speed (12 Mbps) transceiver

4.6.6.4 USB Voltage Regulator

- 5 V regulator input typically provided by USB VBUS power
- 3.3V regulated output powers on-chip USB transceiver
- Output pin from regulator can be used to power external board components and source up to 120mA
- Eliminates cost of external LDO
- 3.3V regulated output can power MCU main power supply

4.6.6.5 UART2

The UART2 includes the following features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection with /32 fractional divide, based on the module clock frequency
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Programmable transmitter output polarity

- Programmable receive input polarity
- Up to 14-bit break character transmission.
- 11-bit break character detection option
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Address match feature in the receiver to reduce address mark wakeup ISR overhead
- Ability to select MSB or LSB to be first bit on wire
- Support for ISO 7816 protocol to interface with SIM cards and smart cards
  - Support for T=0 and T=1 protocols
  - Automatic retransmission of NACK'd packets with programmable retry threshold
  - Support for 11 and 12 ETU transfers
  - Detection of initial packet and automated transfer parameter programming
  - Interrupt-driven operation with seven ISO-7816 specific interrupts:
    - Wait time violated
    - Character wait time violated
    - Block wait time violated
    - Initial frame detected
    - Transmit error threshold exceeded
    - Receive error threshold exceeded
    - Guard time violated
- Interrupt-driven operation with flags, not specific to ISO-7816 support
  - Transmitter data buffer at or below watermark
  - Transmission complete
  - Receiver data buffer at or above watermark
  - Idle receiver input
  - Receiver data buffer overrun
  - Noise error
  - Framing error
  - Parity error
  - Active edge on receive pin
  - LIN break detect
- Receiver framing error detection
- Hardware parity generation and checking
- 1/16 bit-time noise detection
- DMA interface

4.6.6.6 LPUART0 and LPUART1

- Full-duplex, standard non-return-to-zero (NRZ) format
- Programmable baud rates (13-bit modulo divider) with configurable oversampling ratio from 4x to 32x
- Transmit and receive baud rate can operate asynchronous to the bus clock:
  - Baud rate can be configured independently of the bus clock frequency
  - Supports operation in Stop modes
- Interrupt or polled operation:
  - Transmit data register empty and transmission complete
  - Receive data register full
  - Receive overrun, parity error, framing error, and noise error
  - Idle receiver detect
  - Active edge on receive pin
  - Break detect supporting LIN
  - Receive data match
- Hardware parity generation and checking
- Programmable 8-bit, 9-bit or 10-bit character length
- Programmable 1-bit or 2-bit stop bits
- Three receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
  - Receive data match
- Automatic address matching to reduce ISR overhead:
  - Address mark matching
  - Idle line address matching
  - Address match start, address match end
- Optional 13-bit break character generation / 11-bit break character detection
- Configurable idle length detection supporting 1, 2, 4, 8, 16, 32, 64 or 128 idle characters
- Selectable transmitter output and receiver input polarity

4.6.6.7 Serial Peripheral Interface (SPI)

- Master and slave mode
- Full-duplex, three-wire synchronous transfers
- Programmable transmit bit rate
- Double-buffered transmit and receive data registers
- Serial clock phase and polarity options
- Slave select output
- Mode fault error flag with CPU interrupt capability
- Control of SPI operation during wait mode
- Selectable MSB-first or LSB-first shifting
- Support for both transmit and receive by DMA

4.6.6.8 Synchronous Serial Interface (I^2S)

- Independent (asynchronous) or shared (synchronous) transmit and receive sections with separate or shared internal/ external clocks and frame syncs, operating in master or slave mode intended for audio support
- Master or slave mode operation
- Normal mode operation using frame sync
- Network mode operation allowing multiple devices to share the port with up to 32 time slots
- Programmable data interface modes, such as I^2S, LSB aligned, and MSB aligned
- Programmable word length (8, 10, 12, 16, 18, 20, 22 or 24 bits)
- AC97 support

4.6.7 Human-machine interface

4.6.7.1 General-Purpose Input/Output (GPIO)

- Hysteresis and configurable pullup/pulldown device on all input pins
- Configurable drive strength on some output pins
- Independent pin value register to read logic level on digital pin

5 Part numbers and packaging

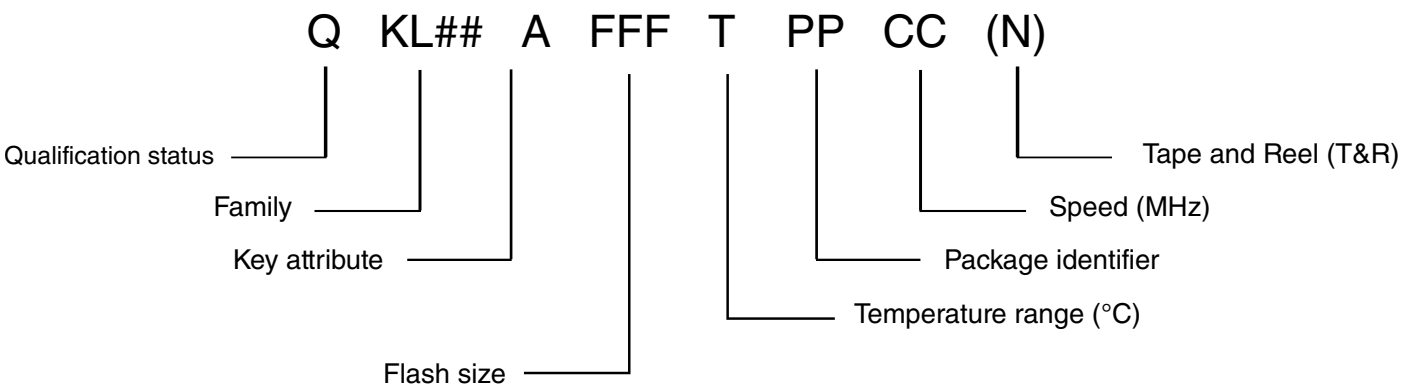

Figure 2. Part numbers diagrams

Table 6. Part number fields descriptions

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KL##	Kinetis family	• KL33 • KL43
A	Key attribute	• Z = Cortex-M0+
FFF	Program flash memory size	• 128 = 128 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	
PP	Package identifier	• LH = 64 LQFP (10 mm x 10 mm) • MP = 64 MAPBGA (5 mm x 5 mm)
CC	Maximum CPU frequency (MHz)	• 4 = 48 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

6 Revision history

The following table provides a revision history for this document.

Table 7. Revision history

Rev. No.	Date	Substantial changes
0	01/2014	• Initial release

1	08/2014	• Public release
		  • Updated feature list
		  • Updated Orderable part numbers
		  • In Section "Module-by-module feature list", added two sections: 'Low-Power Timer' and 'FlexIO'

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