Freescale Semiconductor
Product Brief

MCF5373PB
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MCF5373 ColdFire® Microprocessor Product Brief

Supports MCF5372L, MCF5372, MCF5373L, & MCF5373

by: Microcontroller Division

The MCF537*x* devices are a family of highly-integrated 32-bit microprocessors based on the Version 3 ColdFire microarchitecture. All MCF537*x* devices contain a 32-Kbyte internal SRAM, a two-bank SDR/DDR SDRAM controller, a 16-channel DMA controller, up to three UARTs, a queued SPI, as well as other peripherals that enable the MCF537*x* family for use in general purpose industrial control applications. Optional peripherals include a fast Ethernet controller, USB host and On-the-Go controllers, a CAN module, and cryptography hardware accelerators.

This document provides an overview of the MCF537*x* microprocessor family, focusing on its highly diverse feature set. It was written from the perspective of the MCF5373L device. However, it also pertains to the MCF5372L, MCF5372, MCF53721, and MCF5373. See the following section for a summary of differences between the various devices of the MCF537*x* family.

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1 MCF537*x* Device Configurations

The following table compares the various device derivatives available within the MCF537*x* family.

Table 1. MCF537*x* Family Configurations

Module	MCF5372	MCF5372L	MCF53721	MCF5373	MCF5373L
ColdFire Version 3 Core with EMAC (Enhanced Multiply-Accumulate Unit)	•	•	•	•	•
Core (System) Clock	up to 180 MHz	up to 240 MHz		up to 180 MHz	up to 240 MHz
Peripheral and External Bus Clock (Core clock ÷ 3)	up to 60 MHz	up to 80 MHz		up to 60 MHz	up to 80 MHz
Performance (Dhrystone/2.1 MIPS)	up to 158	up to 211		up to 158	up to 211
Instruction/Data Cache	16 Kbytes				
Static RAM (SRAM)	32 Kbytes				
SDR/DDR SDRAM Controller	•	•	•	•	•
USB 2.0 Host	—	•	•	—	•
USB 2.0 On-the-Go	—	•	•	—	•
Synchronous Serial Interface (SSI)	•	•	•	•	•
Fast Ethernet Controller (FEC)	•	•	•	•	•
Cryptography Hardware Accelerators	—	—	•	•	•
Embedded Voice-over-IP System Solution	—	—	•	—	—
FlexCAN 2.0B communication module	—	—	•	—	—
UARTs	3	3	3	3	3
I^2C	•	•	•	•	•
QSPI	•	•	•	•	•
PWM Module	—	•	•	—	•
Real Time Clock	•	•	•	•	•
32-bit DMA Timers	4	4	4	4	4
Watchdog Timer (WDT)	•	•	•	•	•
Periodic Interrupt Timers (PIT)	4	4	4	4	4
Edge Port Module (EPORT)	•	•	•	•	•
Interrupt Controllers (INTC)	2	2	2	2	2
16-channel Direct Memory Access (DMA)	•	•	•	•	•
FlexBus External Interface	•	•	•	•	•
General Purpose I/O (GPIO)	up to 46	up to 62	up to 62	up to 46	up to 62
JTAG - IEEE® 1149.1 Test Access Port	•	•	•	•	•
Package	160 QFP	196 MAPBGA	196 MAPBGA	160 QFP	196 MAPBGA

2 Block Diagram

The superset device in the MCF537*x* family is available in a 196 mold array process ball grid array (MAPBGA) package. Figure 1 shows a top-level block diagram of the MCF5373.

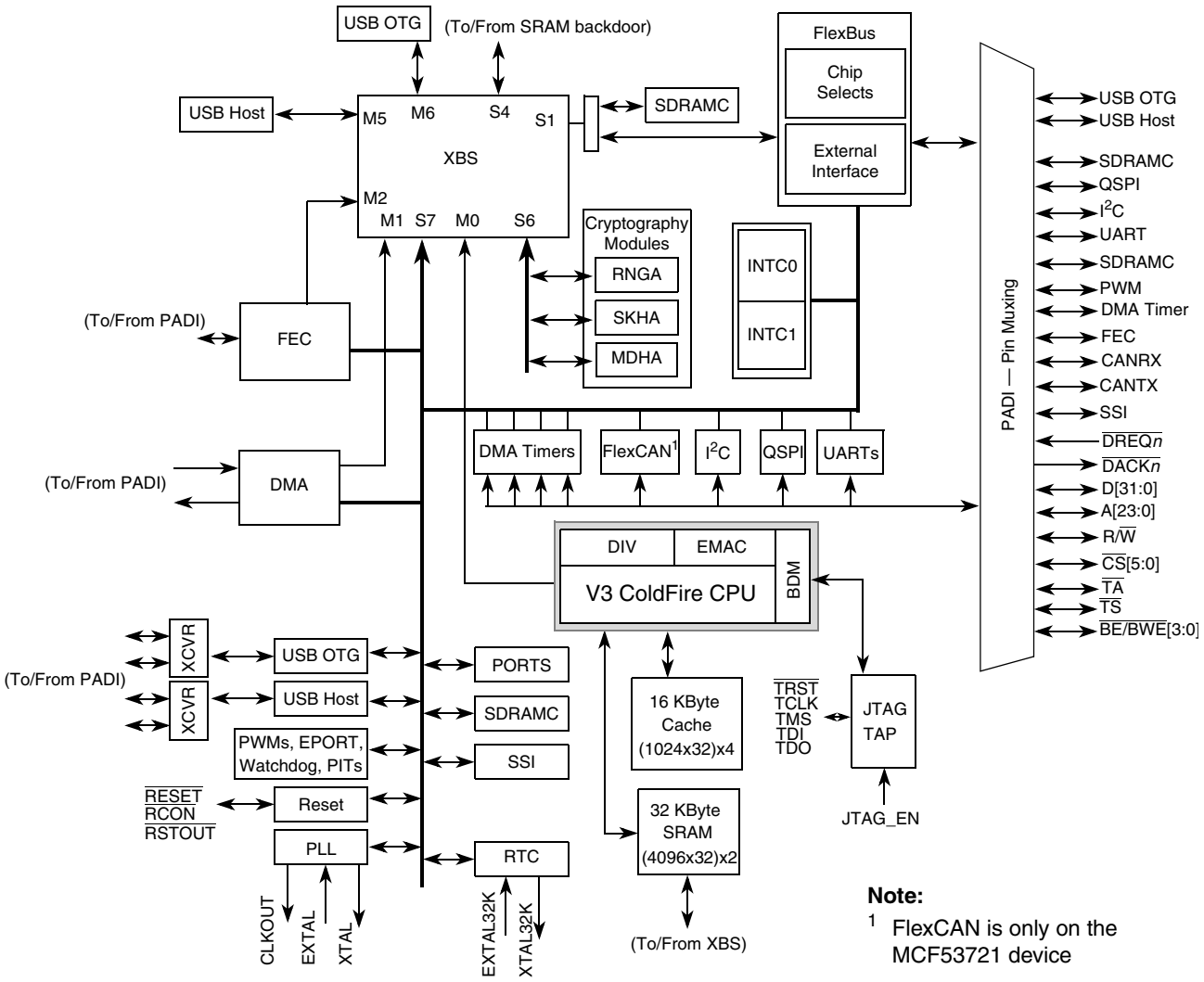

Figure 1. MCF5373 Block Diagram

3 Features

The following is a brief summary of the functional blocks in the MCF5373L superset device. For more details refer to the *MCF5373 ColdFire Microprocessor Reference Manual* (MCF5373RM).

- Version 3 ColdFire variable-length RISC processor core
  - Static operation
  - 32-bit address and data path on-chip
  - Processor core runs at three times the bus frequency

  - Sixteen general-purpose 32-bit data and address registers
  - Implements the ColdFire instruction set architecture, ISA_A+, with extensions to support the user stack pointer register, and 4 new instructions for improved bit processing
  - Enhanced multiply-accumulate (EMAC) unit with four 48-bit accumulators to support 32-bit signal processing algorithms
  - Hardware divide execution unit supporting various 32-bit operations
  - Illegal instruction decode that allows for 68K emulation support
- System debug support
  - Background debug mode (BDM) Revision B+ for in-circuit debugging
  - Real time debug support, with nine user-visible hardware breakpoint registers (PC and address with optional data) that can be configured into a 1- or 2-level trigger
- JTAG support for system level board testing
- On-Chip memories
  - 16-Kbyte unified write-back cache
  - 32-Kbyte dual-ported SRAM on CPU internal bus, accessible by core and non-core bus masters (DMA, FEC, and USB host and OTG)
- Power management
  - Fully static operation with processor wait, doze, and stop modes
  - Very rapid response to interrupts from sleep mode
  - Global clock disable register to disable clocks to most modules
  - Ability to bypass PLL circuitry for low-power and low-speed mode
- Embedded voice-over-IP (VoIP) system solution
  - Fully integrated and tested software VoIP package
- SDR/DDR SDRAM controller
  - Supports a glueless interface to SDR and DDR SDRAM devices
  - 16-bit (DDR) or 32-bit (SDR) fixed memory port width
  - 16 bytes critical word first burst transfer
  - Up to 14 lines of row address, up to 12 (in 32-bit mode) or 13 (in 16-bit bus mode) column address lines, 2 bits of bank address, and a maximum of two pinned-out chip selects. The maximum row bits plus column bits equals 24 in 32-bit bus mode or 25 in 16-bit mode
  - Supports up to 256 MBytes of memory per chip select, 512 MBytes total
  - Supports page mode to maximize the data rate
  - Supports sleep and self-refresh modes
- Universal Serial Bus (USB) host controller
  - Fully compliant with the *Universal Serial Bus Specification, Revision 2.0*
  - Support for full speed (FS = 12 Mbps) and low speed (LS = 1.5 Mbps) with on-chip FS/LS transceiver

  - Compatible with the *Enhanced Host Controller Interface (EHCI) Specification for Universal Serial Bus, Revision 1.0*
  - Connects to external 5 V power control chip for 100mA to 500mA downstream power
  - Uses 60 MHz reference clock based off of the system clock or from an external pin
- Universal Serial Bus (USB) On-the-Go (OTG) controller
  - Fully compliant with the *On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a*
  - Support for full speed and low speed with on-chip transceiver in host mode.
  - Support for full speed with on-chip transceiver in device mode.
  - Connects to external OTG charge pump and resistor chip via I^2C bus
  - Embedded host controller compatible with the *Enhanced Host Controller Interface (EHCI) Specification for Universal Serial Bus, Revision 1.0*
  - Uses 60 MHz reference clock based on the system clock or from an external pin
- Synchronous serial interface (SSI)
  - Supports shared (synchronous) transmit and receive sections
  - Normal mode operation using frame sync
  - Network mode operation allowing multiple devices to share the port with as many as 32 time slots
  - Gated clock mode operation requiring no frame sync
  - Programmable data interface modes such as I^2S, LSB, MSB aligned
  - Programmable word length up to 24 bits
  - AC97 support
- Fast Ethernet controller (FEC)
  - 10/100 BaseT/TX capability, half duplex or full duplex
  - On-chip transmit and receive FIFOs
  - Built-in dedicated DMA controller
  - Memory-based flexible descriptor rings
  - Media independent interface (MII) to external transceiver (PHY)
- Cryptography hardware accelerators
  - FIPS-140 compliant random number generator
  - MD5 and SHA-160 one-way hash algorithms
  - DES, Triple-DES, and AES ciphers
- FlexCAN module
  - Full implementation of the CAN protocol specification version 2.0B
    - Standard Data and Remote Frames (up to 109 bits long)
    - Extended Data and Remote Frames (up to 127 bits long)
    - 0–8 bytes data length

  - Programmable bit rate up to 1 Mbit/sec
- 16 flexible Message Buffers (MBs) of 0–8 bytes data length each, configurable as Rx or Tx, all supporting standard and extended messages
- Listen-only mode capability
- Content-related addressing
- Three programmable mask registers: global (for MBs 0-13), special for MB14 and special for MB15
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message

- Three universal asynchronous receiver transmitters (UARTs)
  - 16-bit divider for clock generation
  - Interrupt control logic
  - DMA support with separate transmit and receive requests
  - Data formats can be 5, 6, 7, or 8 bits with even, odd or no parity
  - Up to two stop bits in 1/16 increments
  - Error-detection capabilities
  - Flow control support includes request-to-send ($\overline{\text{URTS}}$) and clear-to-send ($\overline{\text{UCTS}}$) lines
- I^2C module
  - Interchip bus interface for EEPROMs, A/D converters, and keypads
  - Fully compatible with industry-standard I^2C bus
  - Master or slave modes support multiple masters
  - Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
  - Full-duplex, three-wire synchronous transfers
  - Up to three chip selects available
  - Master mode operation only with programmable master bit rates
  - Up to 16 pre-programmed transfers
- Pulse width modulation (PWM) module
  - Four independent PWM channels with programmable period and duty cycle
  - Dedicated counter for each PWM channel
  - Programmable PWM enable/disable for each channel
  - Software selection of PWM duty pulse polarity for each channel
- Real time clock
  - Full clock – days, hours, minutes, seconds
  - Minute countdown timer with interrupt

  - Programmable daily alarm with interrupt
  - Sampling timer with interrupt
  - Once-per-day, once-per-hour, once-per-minute, and once-per-second interrupts
  - Operation at 32.768 kHz, 32 kHz, or 38.4 kHz (determined by reference clock crystal)
- Four 32-bit DMA timers
  - 12.5 ns resolution at 80 MHz
  - Programmable prescaler and sources for clock input, including an external clock option
  - Input-capture capability with programmable trigger edge on input pin
  - Output-compare with programmable mode for the output pin
  - Free run and restart modes
  - Maskable interrupts and DMA trigger capability on input capture or output compare
- Software watchdog timer
  - 16-bit counter
  - Low-power mode support
- Four periodic interrupt timers (PITs)
  - 16-bit counter
  - Selectable as free running or count down
- Phase locked loop (PLL)
  - 16 MHz reference frequency
  - Programmable dithering
- Interrupt controllers (x2)
  - Support for up to 126 interrupt sources
  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low power modes
- DMA controller
  - 16 fully programmable channels with 32-byte transfer control
  - Data movement via dual-address transfers for 8-, 16-, 32-, and 128-bit data values
  - Programmable source and destination addresses, transfer size, and support for enhanced address modes
  - Support for major and minor nested counters with one request and one interrupt per channel
  - Support for channel-to-channel linking and scatter/gather for continuous transfers with fixed priority and round-robin channel arbitration.
  - External request pins for up to four channels
- FlexBus (external interface)

  - Glueless connections to 8-, 16-, or 32-bit external memory devices (SRAM, Flash, ROM, etc.)
  - Support for independent primary and secondary wait states per chip select
  - Programmable address setup and hold time with respect to chip select negation, per transfer direction
  - Glueless interface to SRAM devices with or without byte strobe inputs
  - Programmable wait state generator
  - 32-bit bidirectional data bus and 24-bit address bus
  - Up to six chip selects available
  - Byte/write enables (byte strobes)
  - Ability to boot from external memories that are 8, 16, or 32 bits wide
- Chip configuration module (CCM)
  - System configuration during reset
  - Unique part identification number and part revision number
- Reset controller
  - Separate reset in and reset out signals
  - Five reset sources: power-on reset (POR), external, software, watchdog, PLL loss of lock
  - Status flag indication of source of last reset
- General purpose I/O interface
  - Up to 64 bits of GPIO for the MCF5372L, MCF53721, and MCF5373L
  - Up to 46 bits of GPIO for the MCF5372 and MCF5373
  - Bit manipulation supported via set/clear functions
  - Unused peripheral pins may be used as extra GPIO
  - Programmable drive strength or slew rate control for related group of pins

3.1 V3 Core Overview

The Version 3 ColdFire processor core consists of two independent pipeline structures decoupled by an instruction buffer. The four-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V3 core implements the ColdFire Instruction Set Architecture Revision A+ with added support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the core includes the enhanced multiply-accumulate unit (EMAC) for improved signal processing capabilities. The EMAC implements a four-stage execution pipeline, optimized for 32 × 32 bit operations, with support for four 48-bit accumulators. Supported operands include 16- and 32-bit signed and unsigned integers and signed fractional operands, as well as a complete set of instructions to process these data types. The EMAC

provides superb support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

The core also includes a hardware divide unit that performs a number of integer-divide operations. The supported divide functions include: 32-bit dividend and 16-bit divisor producing a 16-bit quotient and a 16-bit remainder, 32-bit dividend and 32-bit divisor producing a 32-bit quotient, and 32-bit dividend and 32-bit divisor producing a 32-bit remainder.

3.2 Debug Module

The ColdFire processor core debug interface is provided to support system debugging with low-cost debug and emulator development tools. Through a standard debug interface, you can access debug information. This allows the processor and system to be debugged without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of nine programmable registers—a pair of upper and lower address registers, a pair of data registers (a 32-bit data register and a 32-bit data mask register), and four 32-bit PC registers plus a 32-bit PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception.

To support program trace, the V3 Coldfire core's debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at one-half the CPU's clock rate.

3.3 JTAG

The MCF5373 supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a bypass register, a boundary-scan register, and an ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The MCF5373 implementation can do the following:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample MCF5373 system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the MCF5373 for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

3.4 On-chip Memories

3.4.1 Cache

The MCF5373 architecture includes a 16-Kbyte unified cache. This four-way set-associative cache provides pipelined, single-cycle access on cached instructions and operands.

As with all ColdFire caches, the cache controller implements a non-lockup, streaming design. The use of processor-local memories decouples performance from external memory speeds and increases available bandwidth for external devices or the on-chip DMA module.

The cache implements line-fill buffers to optimize 16-byte line burst accesses. Additionally, the cache supports copyback, write-through, or cache-inhibited modes. A four-entry, 32-bit buffer is used for cache line push operations and can be configured for deferred write buffering in write-through or cache-inhibited modes.

3.4.2 SRAM

The SRAM module provides a general-purpose 32-Kbyte memory block that the ColdFire core can access in a single cycle. The memory is ideal for storing critical code or data structures or for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The dual-port SRAM module is also accessible by the DMA, USB host and OTG, and FEC non-core bus masters through the crossbar switch. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a bus-mastering device operate in alternate regions of the SRAM to maximize system performance. As an example, system performance can be increased significantly if Ethernet packets are moved from the FEC into the SRAM (rather than external memory) prior to any processing.

3.5 Voice-over-IP (VoIP) System Solution

A fully integrated and tested VoIP software development kit is provided with the MCF53721 device. The development kit also includes a royalty-free uClinux™ embedded software BSP complete with source code, GNU tools, kernel, and a broad collection of applications and drivers. This open source BSP is augmented by a complete take-to-market middleware system that includes certified SIP telephony stack, audio subsystem with APIs, and advanced device management system.

The product is suitable for applications that require real-time two-way voice communications and control interfaces, including:

- Building intercom systems
- Building fire and alarm panels
- Emergency panels and poles
- Drive-thru kiosks
- Self-serve kiosks

- Elevator control panels
- Gas bar attendant
- Point-of-sale equipment
- Terminal adapter equipment
- Handsets, spearkerphones
- WiFi phones

Figure 2 illustrates the placement of the VoIP development kit in an embedded system solution.

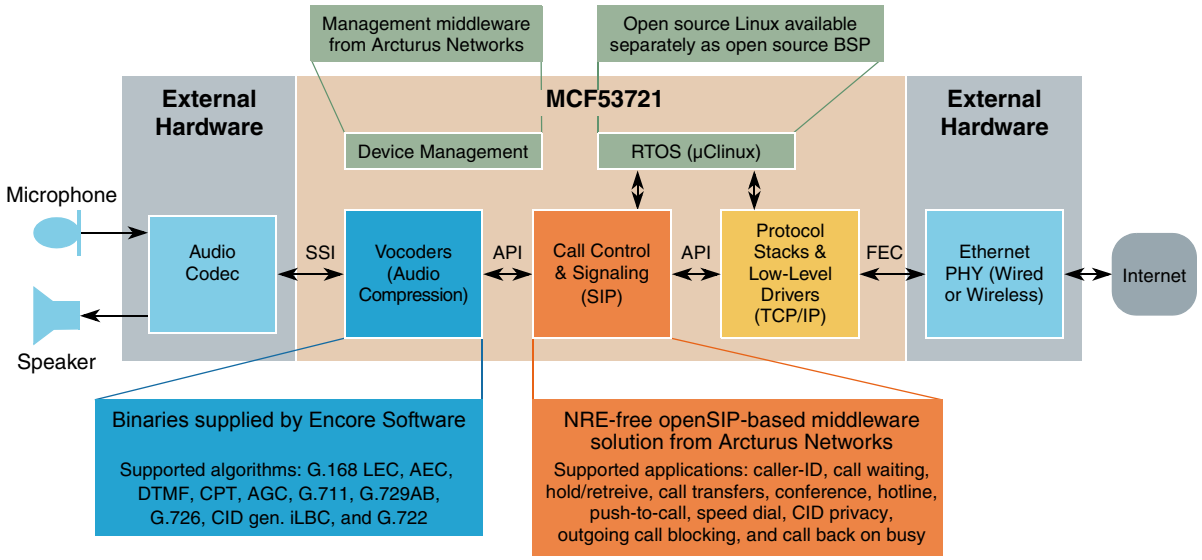

Figure 2. MCF53721 Embedded VoIP System Solution

3.6 SDR/DDR SDRAM Controller

The SDRAM controller provides a glueless interface to SDR and DDR SDRAM memory devices. The module uses a 32-bit (for SDR) or a 16-bit (for DDR) memory port and can address up to 512 MB of data (256 MB per chip select). The controller supports DDR and SDR SDRAM, but both cannot be used at the same time.

3.7 USB Host and OTG Controllers

MCF5373 supports two separate USB 2.0 compliant controllers on chip; a host-only core and an On-The-Go (or dual-role) core. Both controllers support full-speed (12 Mbps) and/or low-speed (1.5 Mbps) USB data rates via on-chip transceivers (The USB OTG module in device mode does not support low-speed). The USB host module and the USB On-The-Go module's embedded host controller are compliant with the EHCI driver model and support directly connected full-speed and low-speed devices without the need for UHCI/OHCI companion controllers and associated driver stacks. Both USB controllers contain chaining direct memory access (DMA) engines that reduce interrupt load on the CPU, thereby reducing total system bus bandwidth utilization.

The USB controllers are compliant with the following industry standards:

- *Universal Serial Bus Specification, Revision 2.0*
- *On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a*
- *Enhanced Host Controller Interface (EHCI) Specification for Universal Serial Bus, Revision 1.0*
- *USB 2.0 Transceiver Macrocell Interface (UTMI) Specification, Version 1.05*

3.7.1 USB Host Controller

The USB host controller is configured for a single port, which can connect to downstream hubs to support connection of up to 127 devices. The host controller also supports connection to external USB power control devices for downstream power delivery.

3.7.2 USB On-the-Go Controller

The second USB controller is programmable to support host, device or On-the-Go operations. The dual-role feature allows device-to-device connectivity, without the need for a host PC (e.g. digital camera to photo printer).

3.8 Synchronous Serial Interface (SSI)

The SSI is a full-duplex, serial port that allows the chip to communicate with a variety of serial devices, including audio codecs, digital signal processors (DSPs), and microprocessors that implement the inter-IC sound bus standard (I^2S) or Intel AC97 standard. SSI typically transfers samples in a periodic manner.

3.9 Fast Ethernet Controller (FEC)

The MCF5373's integrated fast Ethernet controller (FEC) performs the full set of IEEE® 802.3/Ethernet CSMA/CD media access control and channel interface functions. The FEC supports connection and functionality for the 10/100 Mbps 802.3 media independent interface (MII). It requires an external transceiver (PHY) to complete the interface to the media.

3.10 Cryptography Accelerators

The superset device, MCF5373L, incorporates small, fast, dedicated hardware accelerators for random number generation, message digest and hashing, and the DES, 3DES, and AES block cipher functions. This allows for the implementation of common Internet security protocol cryptography operations with performance well in excess of software-only algorithms. Each of the three accelerator modules contains a DMA option for transferring data.

3.11 FlexCAN

The FlexCAN module implements the 2.0B CAN protocol that is a commonly used industrial control serial bus that meets the specific requirements of real-time processing, reliable operation in a harsh EMI environment, cost-effectiveness, and required bandwidth. FlexCAN has 16 message buffers.

3.12 UARTs

The MCF5373L contains three independent, full-duplex UARTs. The three UARTs can be clocked by the system bus clock, eliminating the need for an externally supplied clock. They can use DMA requests on transmit-ready and receive-ready as well as interrupt requests for servicing.

3.13 I^2C Bus

The I^2C bus is a two-wire, bidirectional serial bus that provides an efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices.

3.14 QSPI

The queued serial peripheral interface module provides a high-speed synchronous serial peripheral interface with queued transfer capability. It allows up to 16 transfers to be queued at once, eliminating CPU intervention between transfers.

3.15 Pulse Width Modulation (PWM) Timer

The pulse width modulation (PWM) timer generates a synchronous series of pulses having programmable duty cycle. With a suitable low-pass filter, the PWM can be used as a digital-to-analog converter.

The PWM module has four channels, each having a programmable period and duty cycle as well as a dedicated counter. A flexible clock select scheme allows a total of four different clock sources to be used with the counters. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%. The PWM outputs can be programmed as left-aligned outputs or center-aligned outputs

3.16 Real Time Clock

The real time clock module has a dedicated 32/32.768/38.4 kHz crystal oscillator and provides the system with a full clock, capable of interrupting the core once per day, hour, minute, or second. It also contains a sampling timer which can periodically interrupt the core.

3.17 DMA Timers (DTIM0-DTIM3)

There are four independent, DMA-transfer-generating 32-bit timers (DTIM[3:0]) on the MCF5373L. Each timer module incorporates a 32-bit timer with a separate register set for configuration and control. The timers can be configured to operate from the system clock or from an external clock source using one of the DT*n*IN signals. If the system clock is selected, it can be divided by 16 or 1. The input clock is further divided by a user-programmable 8-bit prescaler that clocks the actual timer counter register (TCR*n*). Each of these timers can be configured for input-capture or output-compare mode. By configuring the internal registers, each timer may be configured to assert an external pin, generate an interrupt on a particular event, or cause a DMA transfer.

3.18 Software Watchdog Timer

The watchdog timer is a 16-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

3.19 Periodic Interrupt Timers (PIT0-PIT3)

The four periodic interrupt timers (PIT[3:0]) are 16-bit timers that provide precise interrupts at regular intervals with minimal processor intervention. Each timer can count down from the value written in its PIT modulus register, or it can be a free-running down-counter.

3.20 Clock Module and Phase Locked Loop (PLL)

The MCF5373L contains a 16 MHz crystal oscillator, a phase-locked loop, as well as status and control registers. The PLL's output dividers and dithering waveform are register programmable. The system operates via two main clocks generated by the PLL, typically 240 MHz (core) and 80 MHz (peripherals). However, two additional clocks are also generated by the PLL for use by the USB and SDRAM controller modules. To improve noise immunity, the PLL has its own power supply inputs, PLL_VDD and PLL_VSS. All other circuits are powered by the normal internal supply pins, IVDD (core), EVDD (I/O), SD_VDD (SDRAM), and VSS.

The PLL circuitry may be bypassed to reduce system speed and decrease power consumption. The external clock (EXTAL) is used directly, with an optional programmable divider, to produce the internal core and bus clocks.

3.21 Interrupt Controllers (INTC0/INTC1)

There are two interrupt controllers on the MCF5373, which can support up to 126 interrupt sources. Each interrupt source has a unique interrupt vector, and all sources of a given controller provide a programmable level (1-7).

3.22 DMA Controller

The implementation of the DMA on the MCF537x family is targeted towards cost-sensitive applications while providing a high level of functionality. The DMA executes in parallel with the core, enabling transfers of data between the memory and peripherals with little intervention from the core, thus increasing system performance, as well as simplifying software development. The DMA is capable of performing complex data transfers via 16 programmable DMA channels. The hardware microarchitecture includes the DMA engine (which performs source/destination address calculations and data movement operations), and a dedicated memory array containing transfer control descriptors.

3.23 FlexBus External Interface

The FlexBus provides an external interface to 8-, 16-, or 32-bit memory devices (SRAM, Flash, ROM, etc.). The FlexBus's internal data lines are shared with the SDRAM controller. When the SDRAMC is in DDR mode (DRAMSEL = 0), the D[31:16] signals are dedicated to the SDRAM controller data bus and the D[15:0] signals are dedicated to the FlexBus data bus. In SDR mode (DRAMSEL = 1), all 32 data lines are shared between the FlexBus and SDRAM controller.

Features are available to support external flash modules and secondary wait states on reads and writes and a signal to support active-low address valid ($\overline{TS}$). Six programmable chip-select outputs provide signals to enable external memory and peripheral circuits, providing all handshaking and timing signals for automatic wait-state insertion and data bus sizing.

Base memory address and block size are programmable, with some restrictions. For example, the starting address must be on a boundary that is a multiple of the block size. Each chip select can be configured to provide read and write enable signals suitable for use with most popular static RAMs and peripherals. Data bus width (8-bit, 16-bit, or 32-bit) is programmable on all chip selects, and further decoding is available for protection from user mode access or read-only access.

3.24 Reset Controller Module

The reset controller is provided to determine the cause of reset, assert the appropriate reset signals to the system, and keep track of what caused the last reset. There are five sources of reset:

- External
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock
- Software

External reset on the $\overline{RSTOUT}$ pin is software-assertable independent of chip reset state. There are also software-readable status flags indicating the cause of the last reset.

3.25 GPIO

Unused bus interface and peripheral pins on the MCF5373L can be used as discrete general-purpose inputs and outputs. These are managed by a dedicated GPIO module that logically groups all pins into ports located within a contiguous block of memory-mapped control registers. Each port has registers that configure, monitor, and control the port pins. Slew rate control or output pad drive strength control is available on all pins.

Most of the pins associated with the FlexBus interface may be used for several different functions. Their primary function is to provide an external interface to access off-chip resources. When not used for this, the pins may be used as general-purpose digital I/O pins.

4 Documentation

Documentation is available from a local Freescale distributor, a Freescale sales office, the Freescale Literature Distribution Center, or through the Freescale World Wide Web address at http://www.freescale.com/coldfire.

5 Revision History

Table 2 provides a revision history for this document.

Table 2. MCF5373PB Document Revision History

Rev. No.	Substantive Change(s)
0	Initial release.
0.1	Added bullet in USB OTG list in Section 3, “Features” to specify that in device mode the module does not support low-speed mode. Section 3.7, “USB Host and OTG Controllers” added “(The USB OTG module in device mode does not support low-speed.)” in first paragraph.
1	Changed the following in Figure 1: Corrected various signal names: EXTAL32M -> EXTAL, XTAL32M -> XTAL, DACK*n* -> $\overline{\text{DACK}}$*n*, DREQ*n* -> $\overline{\text{DREQ}}$*n*. Removed BNDREG signal as it is not an external signal. Replaced USB signal labels with ‘(To/from PADI)’ as these signals are muxed with others. Corrected UART entry in Table 1; All devices have 3 UARTs available. Instances of ULPI were removed throughout since the device does not support this feature.
2	Added MCF53721 devices to Table 1 and accompanying VoIP system solution row. Added “Embedded Voice-over-IP (VoIP) System Solution” bullet to Section 3, “Features.” Added Section 3.5, “Voice-over-IP (VoIP) System Solution.”
3	Added FlexCAN for the MCF53721 device.

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