Freescale Semiconductor
Product Brief

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MPC8315E Product Brief PowerQUICC II Pro Processor

This document provides an overview of the MPC8315E PowerQUICC II Pro processor features, including a block diagram showing the major functional components. The MPC8315E is a cost-effective, low-power, highly integrated host processor that addresses the requirements of several storage, consumer, and industrial applications, including main CPUs and I/O processors in network attached storage (NAS), voice over IP (VoIP) router/gateway, intelligent wireless LAN (WLAN), set top boxes, industrial controllers, and wireless access points. The MPC8315E extends the PowerQUICC II Pro family, adding higher CPU performance, additional functionality, and faster interfaces while addressing the requirements related to time-to-market, price, power consumption, and package size. This document also supports the MPC8314E host processors but is written from the perspective of the MPC8315E. Note that the MPC8315 and MPC8314 do not support a security engine. In addition, the MPC8314E and MPC8314 do not support dual SATA controllers.

Contents

1 Application Examples

The internal features of the MPC8315E make it suitable for a wide variety of network communication applications as described in this section.

1.1 Media Server / NAS

Figure 1 shows how the MPC8315E can be configured as a media server.

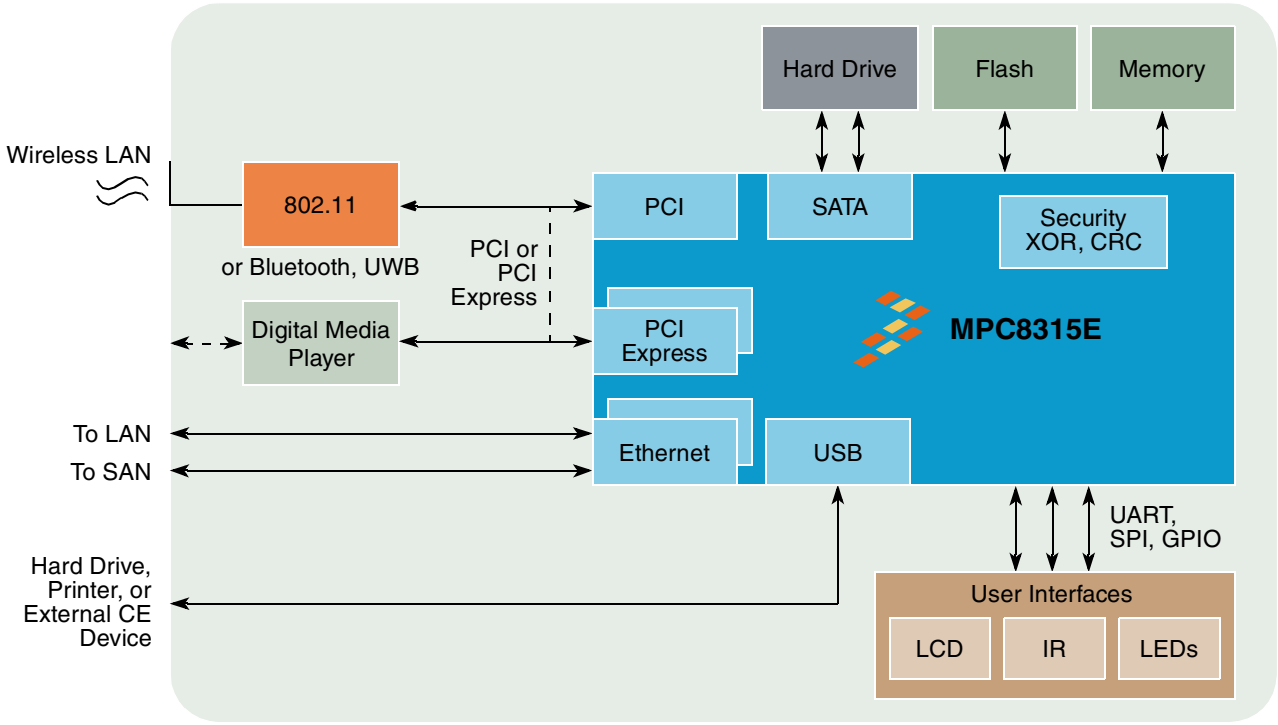

Figure 1. MPC8315E as a Media Server

Multimedia home networking emphasizes both audio and video streaming in the home. Since digital audio takes up relatively little bandwidth, almost any current home network can stream digital audio. However, video is the test of a multimedia home network. For example, the digital media player is a device that allows a user to select and play media content from a digital media server on the network and is usually integrated with the display during playback. As consumers begin to demand standard and high definition video streams and content providers require Digital Rights Management of encrypted streams, multimedia system and network demands grow significantly.

The MPC8315E offers signficant processor and memory performance coupled with high levels of System-on-Chip integration. The dual integrated serial ATA (SATA) 3 Gbps controllers offer connectivity to the amount of storage necessary in a NAS application while dual Ethernet controllers offer connectivity to both a LAN and a storage area network (SAN). Wireless LAN is provided via either PCI Express for next generation IEEE Std. 802.11n™ chipsets and PCI for legacy IEEE Std. 802.11a, 802.11b, 802.11g. The security engine provides acceleration for IPSec as well as DTCP-IP applications.

1.2 Low-End Voice Gateway

Figure 2 illustrates how the MPC8314E can perform the function of a complete low-end voice gateway system.

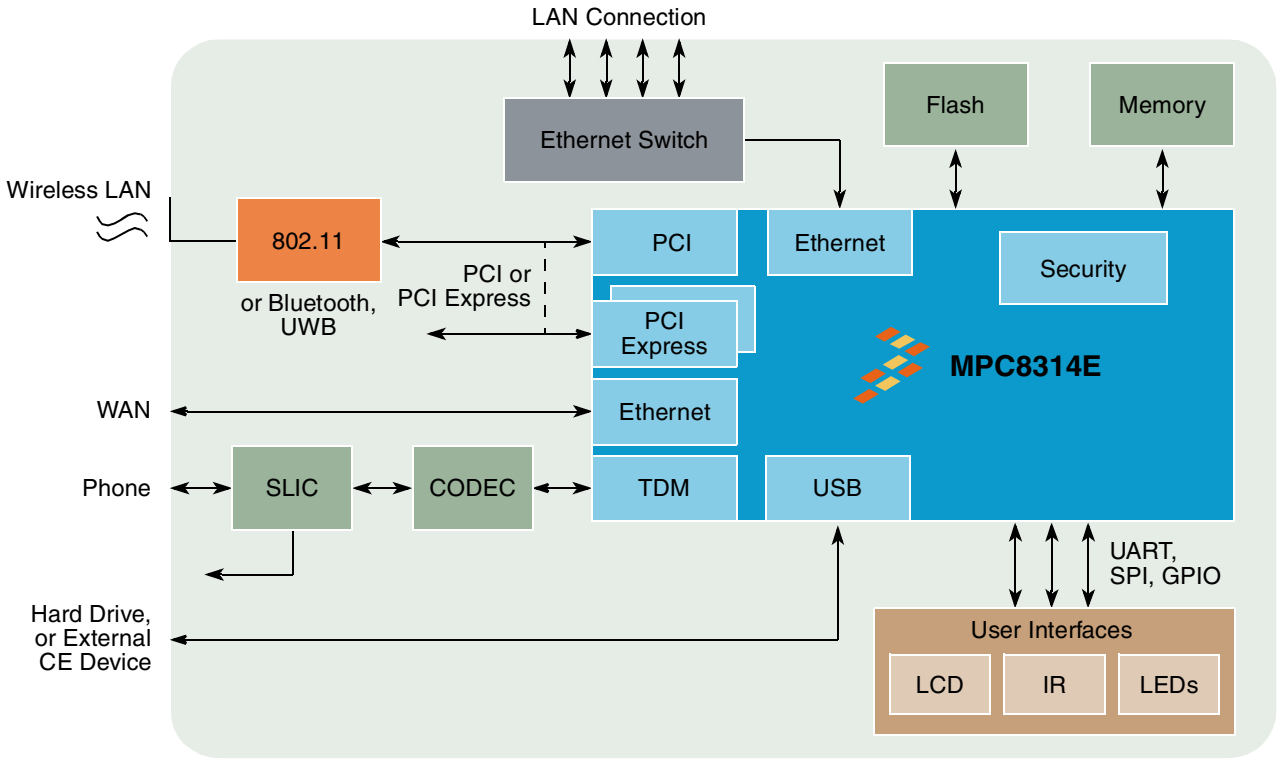

Figure 2. MPC8314E Serving as a Low-End Voice Gateway Application

In this application, the TDM interface provides connectivity to the codec and SLIC for easy integration of voice capabilities. The Ethernet interfaces provide wired access to the WAN and Ethernet switch while wireless connectivity can be provided using PCI or PCI Express. The USB 2.0 interface with integrated PHY provides connectivity to either a hard drive or external CE device. The security core is available to accelerate protocols such as IPSec or IEEE Std. 802.11i for wireless LAN.

1.3 802.11n WLAN Access Point

Figure 3 illustrates the MPC8315E acting as an 802.11n WLAN access point.

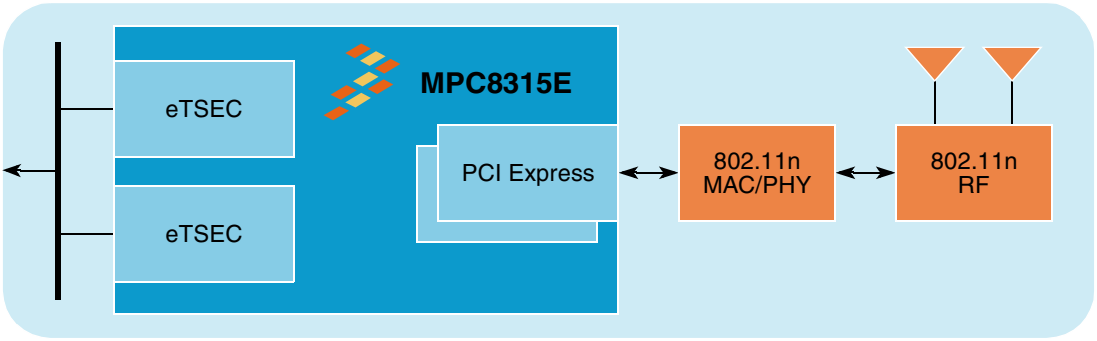

Figure 3. MPC8315E as a WLAN Access Point

Current systems are being designed for IEEE Std. 802.11b and 802.11a/g as well as combo radios. The WiFi chipsets use PCI in current systems. The demand on system performance continues to grow as the industry migrates to IEEE Std. 802.11n chipsets using PCI Express and the IT community requires additional management features.

WLAN access points (WAPs) require low power and are often powered exclusively by Power over Ethernet (POE). Each Ethernet line can supply about 12 W. After accounting for radio and other board power needs, this often leaves <2.5 W for the embedded processor.

When not using PCI Express, available SGMII interfaces make it possible to connect to low-power Gigabit Ethernet PHYs. SGMII support on the Gigabit Ethernet PHYs lowers overall power consumption. The MPC8315E also has superior PCI to memory performance.

2 Features

The MPC8315E incorporates the e300 (MPC603e-based) core, which includes 16 Kbytes of L1 instruction and data caches, on-chip memory management units (MMUs), and floating-point support.

In addition to the e300 PowerPC™ core, the SoC platform includes features such as a dual enhanced three-speed 10, 100, 1000 Mbps Ethernet controllers (eTSECs) with SGMII support, a 32- or 16-bit DDR1/DDR2 SDRAM memory controller, dual SATA 3 Gbps controllers (MPC8315E-specific), a security engine that provides acceleration for control and data plane security protocols, and a high degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration. The MPC8315E also offers peripheral interfaces such as 32-bit PCI interface with up to 66-MHz operation, 16-bit enhanced local bus interface with up to 66-MHz operation, TDM interface, and USB 2.0 with an on-chip USB 2.0 PHY.

The MPC8315E offers additional high speed interconnect support with dual integrated SATA 3 Gbps interfaces and dual single-lane PCI Express interfaces. When not used for PCI Express, the SerDes interface may be configured to support SGMII. The MPC8314E version of the device does not offer the SATA controllers.

The MPC8315E security engine allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the PKE, DES, 3DES, AES, SHA-1, and MD-5 algorithms.

Table 1 highlights the primary functional differences between the MPC8315E and MPC8314E.

Table 1. Functionality of the MPC8315E and MPC8314E

Descriptions	MPC8315E	MPC8314E
PCI Express or SGMII	2 ports	2 ports
SATA	2 ports	0 ports
PCI	1 interface	1 interface

2.1 Block Diagram

A block diagram of the MPC8315E is shown in Figure 4.

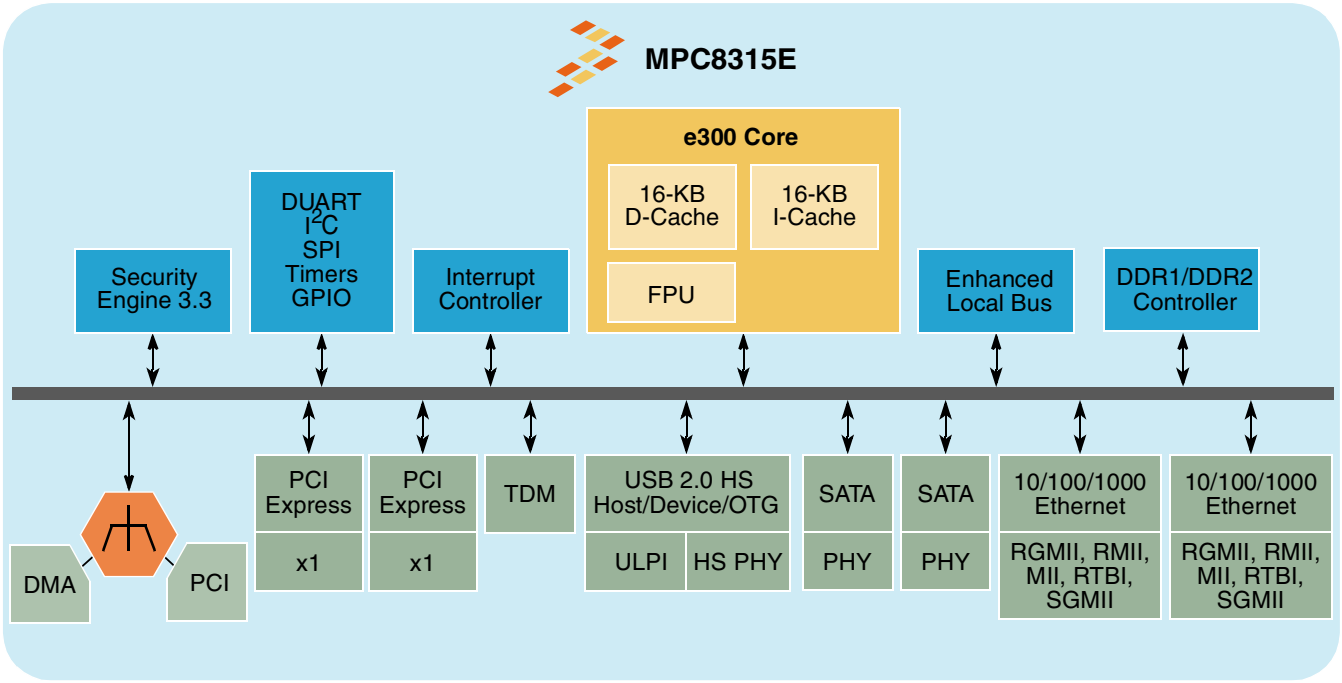

Figure 4. MPC8315E Block Diagram

2.2 Chip-Level Features

The major features of the MPC8315E are as follows:

- e300 (MPC603e-based) core, which includes 16 Kbytes of L1 instruction and data caches, a floating point unit, and performance monitor
- Dual SATA 3 Gbps controllers with integrated PHY
- Dual PCI Express x1 controllers with integrated SerDes PHY

- Dual three-speed 10, 100, 1000 Mbps Ethernet controllers (eTSEC)
- 32/16-bit DDR1/DDR2 memory controller
- Dedicated security engine
- TDM interface
- 32-bit PCI 2.3 controller (3.3V-compatible)
- USB 2.0 host and device controller with an on-chip high-speed PHY
- Flexible enhanced local bus controller (eLBC)
- Intergrated programmable interrupt controller (IPIC)
- Power Management Controller (PMC)
- Four-channel General Purpose DMA controller
- Single I^2C controller
- Serial peripheral interface (SPI) controller with master and slave support
- General-purpose I/O (GPIO) port with 32 parallel I/O pins muxed on various interfaces
- System timers including a periodic interrupt timer, real-time clock, software watchdog timer, and four general-purpose timers
- Dual UART (DUART)
- Designed to comply with IEEE Std. 1149.1™, JTAG boundary scan
- 620 TEPBGA II package

2.3 Module Features

The PowerQUICC II Pro MPC8315E is a high-performance, power-saving, highly integrated host processor solution.

2.3.1 e300 Core

The e300 core has the following features:

- Operates at up to 400 MHz
- 16-Kbyte instruction cache, 16-Kbyte data cache with ECC
- Floating point unit
- Software-compatible with the Freescale processor families implementing the PowerPC Architecture
- Performance monitor

2.3.2 Dual Serial ATA (SATA) Controllers

The SATA controllers have the following features:

- Designed to comply with *Serial ATA 2.5 Specification*
- ATAPI 6+
- Spread spectrum clocking on receive

- Asynchronous notification
- Hot plug including asynchronous signal recovery
- Link power management
- Native command queuing
- Staggered spin-up and port multiplier support
- Port multiplier support
- SATA 1.5 and 3.0 Gbps operation
- Interrupt driven
- Power management support
- Error handling and diagnostic features
  - Far end/near end loopback
  - Failed CRC error reporting
  - Increased ALIGN insertion rates
  - Scrambling and CONT override

2.3.3 Dual PCI Express Interfaces

The PCI Express interfaces have the following features:

- PCI Express 1.0a compatible
- x1 link width
- Selectable operation as root complex or endpoint
- Both 32- and 64-bit addressing
- 128-byte maximum payload size
- Support for MSI and INTx interrupt messages
- Virtual channel 0 only
- Selectable Traffic Class
- Full 64-bit decode with 32-bit wide windows
- Dedicated descriptor-based DMA engine per interface with separate read and write channels

2.3.4 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The MPC8315E eTSECs include the following features:

- Designed to comply with IEEE Std. 802.3™, 802.3u™, 820.3x™, 802.3z™, 802.3ab™, 802.3au™
- Support for different Ethernet physical interfaces:
  - 1000 Mbps IEEE Std. 802.3 RGMII, 802.3z RTBI, full-duplex
  - 10/100 Mbps IEEE Std. 802.3 MII full and half-duplex
  - 10/100 Mbps IEEE Std. 802.3 RMII full and half-duplex
  - Support for SGMII 4-wire differential signaling (Tx, Rx)

- Support for Wake-on-Magic Packet™, a method to bring hte device from standby to full operating mode
- 9.6 Kbyte jumbo frame support
- RMON statistics support
- Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per eTSEC module
- MII management interface for external PHY control and status
- Programmable CRC generation and checking
- Support for weighted round robin and strict priority queueing
- TCP/IP checksum offload for Rx and Tx
- IPv6 and Magic Packet support
- IEEE Std. 1588™ support added
- Lossless flow control support
- QoS support for 8 Rx and 8 Tx hardware queues
- Customizable per-packet rejection
- Customizable per-packet filtering/filing to 64 logical receive queues.
  - Examples: 802.1p, IP TOS, Diffserv classification, TCP/UDP ports, etc.
- Layer 2 features
  - VLAN insertion and deletion per frame
  - 2 exact-match MAC addresses
- Increased hash table address matching

2.3.5 DDR1/DDR2 Memory Controller

The MPC8315E DDR1/DDR2 memory controller includes the following features:

- Single 16- or 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 266 MHz data rate
- Support for two physical banks (chip selects), each bank independently addressable
- 64 Mbit to 1 Gbit devices with x8/x16/x32 data ports (no direct x4 support)
- Support for one 16-bit device or two 8-bit devices on a 16-bit bus OR one 32-bit device or two 16-bit devices or four 8-bit devices on a 32-bit bus
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O

2.3.6 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, 802.11i, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are:

- Public key execution unit (PKEU)
  - RSA and Diffie-Hellman (to 4096b)
  - Programmable field size up to 2048-bits
  - Elliptic curve cryptography (1023b)
  - F2m and F(p) modes
  - Programmable field size up to 511-bits
- Data encryption standard execution unit (DEU)
  - DES, 3DES
  - Two key (K1, K2) or three key (K1, K2, K3)
  - ECB and CBC modes for both DES and 3DES
- Advanced encryption standard unit (AESU)
  - Implements the Rinjdael symmetric key cipher
  - Key lengths of 128, 192, and 256 bits
  - ECB, CBC, CCM, CTR, GCM, CMAC, OFB, CFB and LRW modes
  - XOR acceleration
- Message digest execution unit (MDEU)
  - SHA with 160-bit or 256-bit message digest
  - SHA-384/512
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- Random number generator (RNG)
  - Combines a True Random Number Generator (TRNG) and a NIST-approved Pseudo-Random Number Generator (PRNG) (as described in Annex C of FIPS140-2 and ANSI X9.62)
- Cyclical Redundancy Check Hardware Accelerator (CRCA)
  - Implements CRC32C as required for iSCSI header and payload checksums, CRC32 as required for IEEE Std. 802™ packets, as well as for programmable 32-bit CRC polynomials

2.3.7 TDM Interface

The TDM interface supports the following features:

- Independent receive and transmit with dedicated data, clock and frame sync line
- Separate or shared RCK and TCK whose source can be either internal or external
- Glueless interface to E1/T1 frames and MVIP, SCAS, and H.110 buses
- Up to 128 time slots, where each slot can be programmed to be active or inactive

- 8- or 16-bit word widths
- The TDM Transmitter Sync Signal (TFS), Transmitter Clock Signal (TCK) and Receiver Clock Signal (RCK) can be configured as either input or output
- Frame sync and data signals can be programmed to be sampled either on the rising edge or on the falling edge of the clock
- Frame sync can be programmed as active low or active high
- MSB or LSB first support

2.3.8 PCI Controller

The MPC8315E PCI controller includes the following features:

- Designed to comply with *PCI Local Bus Specification Revision 2.3*
- Single 32-bit data PCI interface operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V tolerant)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

2.3.9 USB Dual-Role Controller

The MPC8315E USB controller includes the following features:

- Designed to comply with *USB Revision 2.0 Specification*
- Full-speed/high-speed PHY (with host/device support)
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports USB on-the-go (OTG) mode, which includes both device and host functionality when using an external ULPI (UTMI+ low-pin interface) PHY
- Supports ULPI or on-chip USB 2.0 full-speed/high-speed PHY

2.3.10 Enhanced Local Bus Controller (eLBC)

The MPC8315E enhanced local bus controller (eLBC) port allows connections with a wide variety of external DSPs and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The three user

programmable machines (UPMs) can be programmed to interface to synchronous devices or custom ASIC interfaces. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM or UPM controller. Both may exist in the same system.

The eLBC offers the following features:

- Multiplexed 26-bit address and 16-bit data operating at up to 66 MHz
- Four chip selects support four external slaves
- Up to eight-beat burst transfers
- 16- and 8-bit port sizes are controlled by an on-chip memory controller
- Three protocol engines available on a per chip select basis:
  - General-purpose chip select machine (GPCM)
  - NAND flash control machine (FCM)
  - Three user programmable machines (UPMs)
- Default boot ROM chip select with configurable bus width (8 or 16 bits)

2.3.11 Integrated Programmable Interrupt Controller (IPIC)

The IPIC implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The IPIC programming model is compatible with the MPC8260 interrupt controller and supports external and internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

2.3.12 Power Management Controller (PMC)

The MPC8315E supports a range of power management states that significantly lower power consumption under the control of the power management controller. The PMC includes the following features:

- Provides power management when the device is used in both PCI host and agent modes
- Supports PCI Power Management 1.2 D0, D1, D2, D3hot, and D3cold states
- Support for PME generation in PCI agent mode, PME detection in PCI host mode
- Supports wake-up from Ethernet (Magic Packet), USB, GPIOs, and PCI (PME input as host) while in the D1, D2 and D3hot states
- Supports a proprietary low-power standby power management state called D3warm
  - The PMC, one Ethernet port, and the GTM block remain powered via a split power supply controlled through an external power switch
  - Wake-up events include Ethernet (Magic Packet), GTM, 2 GPIOs (GPIO_0, GPIO_1), or 2 IRQ inputs (IRQ_B1, IRQ_B2) and cause the device to transition back to normal operation
- PCI Express-based PME events are not supported by the PMC

2.3.13 DMA Controller

The MPC8315E provides an integrated general purpose four-channel DMA controller with the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local masters)
- Misaligned transfer capability for source/destination address
- Supports external DREQ, DACK, and DONE signals

2.3.14 Single I^2C, Serial Peripheral Interface (SPI), DUART, Timers

The I^2C controller is a synchronous, multi-master bus that can be connected to additional devices for expansion and system development.

The serial peripheral interface (SPI) allows the MPC8315E to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. 16-byte FIFOs are supported for both the transmitter and the receiver.

The MPC8315E system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

The general purpose timers have the following features:

- Four 16-bit programmable timers
- Two timers cascaded internally or externally to form a 32-bit timer
- One timer cascaded internally or externally to form a 64-bit timer
- Three programmable input clock sources for the timer prescalers
- Input capture capability
- Output compare with programmable mode for the output pin
- Free run and restart modes
- Functional and programming compatibility with MPC8260 timers

3 Developer Environment

Development tools, hardware platforms, software building blocks and application-specific software solutions are available from Freescale and our Freescale Alliance Program, including third party protocol and signaling stack suppliers, real time operating systems support, and a variety of applications software support. All of this builds upon the existing industry standard PowerQUICC family support program.

To simplify and accelerate the development process, Freescale will provide a user-friendly, integrated development environment (IDE), which includes a compiler, instruction set simulator, and debugger for the e300 PowerPC core.

Freescale also provides an RDB board as a reference platform and programming development environment for the MPC8315E with a complete Linux board support package. The RDB board will support on-board DDR/DDR2 memory, a PCI interface, and a debug port.

4 Document Revision History

Table 2 shows the revision history of this product brief.

Table 2. Revision History

Revision	Section/page	Substantive Change(s)	Author	Date
Rev. 0	N/A	This is the first public version of this document.	Judith Chen	09/14/07

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