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Freescale Semiconductor
Product Brief

MPC8323E PowerQUICC™ II Pro Processor Product Brief

This document provides an overview of the MPC8323E PowerQUICC™ II Pro processor features. The MPC8323E is a cost-effective, highly integrated communications processor that addresses the requirements of several small office/home office (SoHo), access, IP services, and industrial control applications. The MPC8323E extends current PowerQUICC™ I offerings, adding better CPU performance, additional functionality, and faster interfaces while addressing the requirements related to time-to-market, price, power consumption, and board real estate. This document is written from the perspective of the MPC8323E, and unless otherwise noted, the information also applies to the MPC8323, MPC8321E, and MPC8321. Note that the MPC8323 and MPC8321 do not support a security engine.

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1 Application Examples

The internal features of the MPC8323E make it suitable for a wide variety of network communication applications as described in this section.

1.1 SoHo Router

Figure 1 illustrates how a typical small office/home office (SoHo) router application can be realized with the MPC8323E.
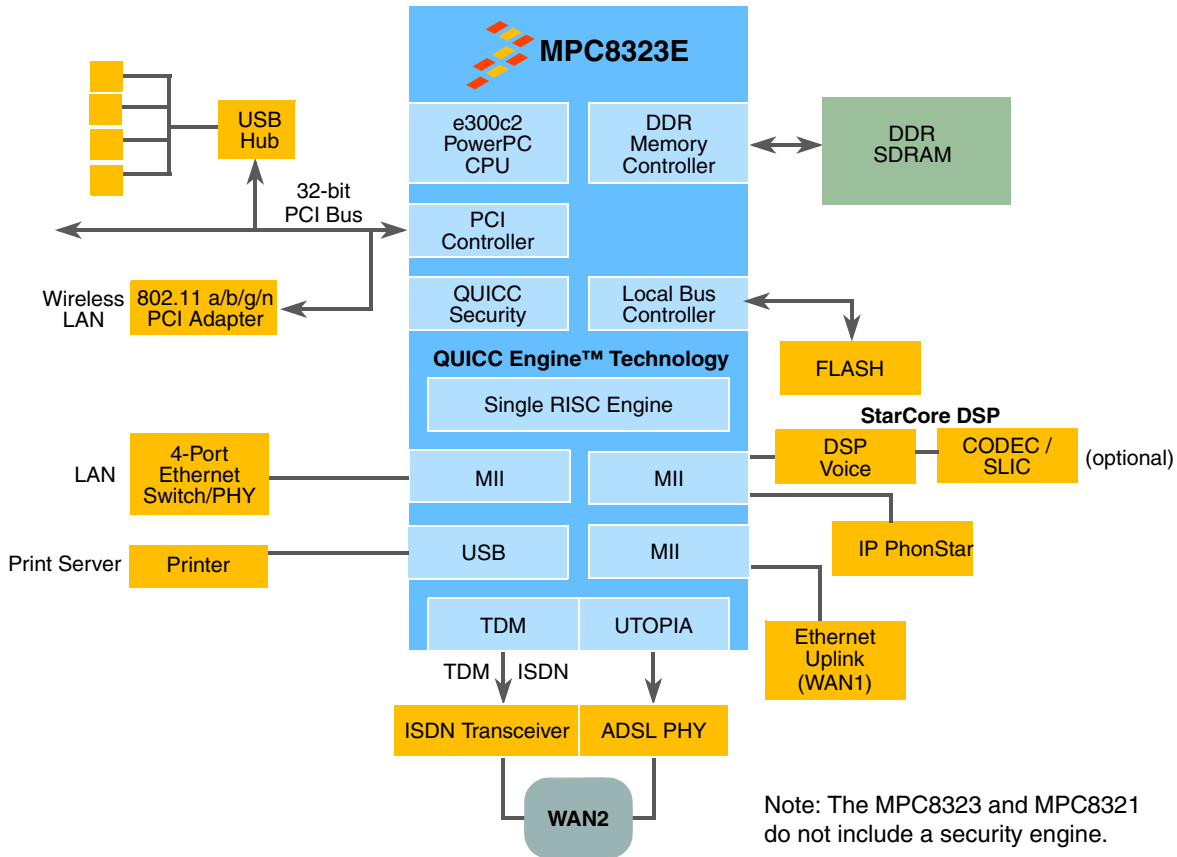

Figure 1. SoHo Router Using MPC8323E

In this application the MPC8323E provides all of the processing and protocol functions required to implement the SoHo router. Specifically, the QUICC Engine™ technology is used to carry voice, data and video using IP over the LAN and WAN interfaces. On the LAN side, one UCC is used to connect to a 4-port fast Ethernet switch. One Ethernet interface is used for uplink, and one of the TDM interfaces provides a leased line E1/T1 connection or an ISDN connection. One UCC is used as an ATM interface supporting AAL5 cell sharing for dial-up ADSL connection, while the last UCC can be configured as serial (UART) or Ethernet (MII) for debug and control.

Alternatively, the remaining UCC of the MPC8323E could be used to support an Ethernet connection to a low cost digital signal processor (DSP) such as the Freescale Starcore family of DSPs based on the StarCore technology supporting 4 to 32 voice ports, which can be used for plain old telephone system

(POTS) telephones or for IP-based telephones using a combination of premium voice algorithms such as G.729a/b, G.723.1 or G.711. For very high-density voice ports, the MSC8122 DSP can be used through an Ethernet interface.

Other interfaces connected to the PCI bus can include a four-port universal serial bus (USB) hub for connecting equipment such as printers, copiers, scanners, and system back up disks. In addition, a wireless LAN interface can be connected to the PCI bus supporting IEEE Std. 802.11-a/b/g/n connectivity within the office environment.

Finally, the security engine provides acceleration for encryption, authentication, and standards based tunnelling as required by IPSec.

1.2   DSLAM Line Card

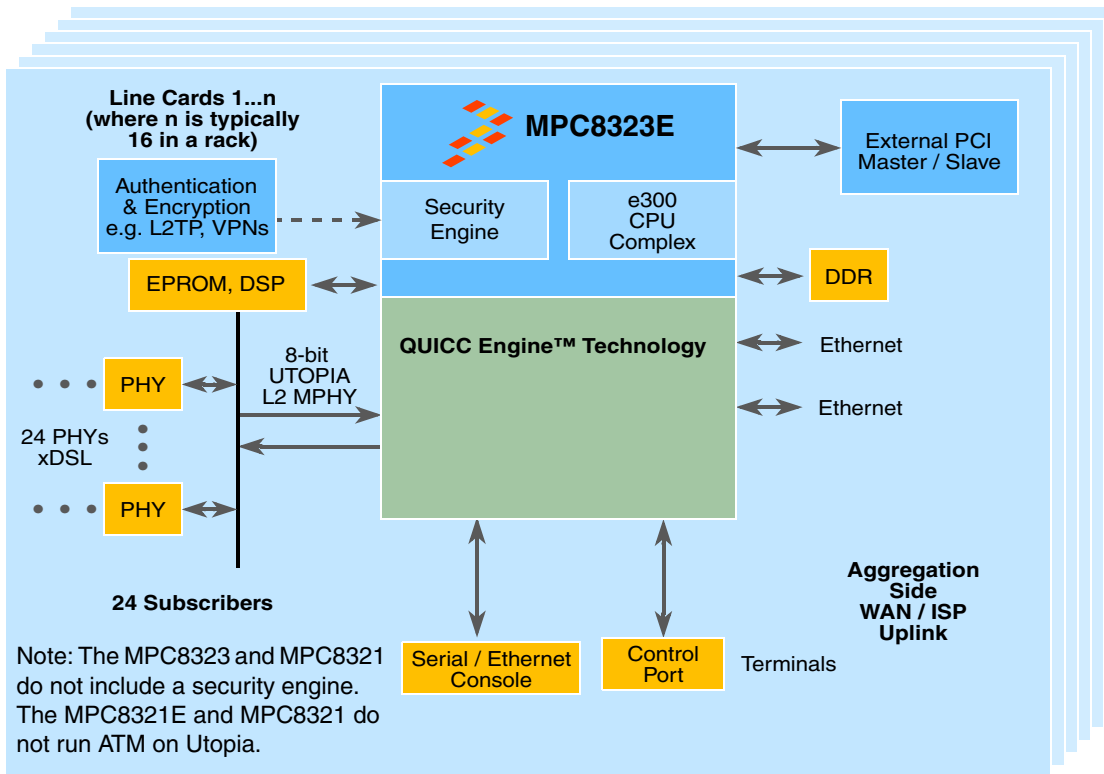The diagram in Figure 2 illustrates how an intelligent DSLAM line-card can be readily implemented.

Figure 2. MPC8323E Line Card Implementation

In this example, the versatility of the UCCs enables the convergence of both packet and circuit switched networks because both ATM and Ethernet functions can be supported. As shown on the left-hand side of Figure 2, subscribers are connected to the DSLAM line-card through the DSL PHYs and the integrated UTOPIA interface on the MPC8323E. Note that the MPC8321 and MPC8321E do not run ATM on Utopia.

2   Features

The MPC8323E incorporates a unique configuration of the e300c2 (MPC603e-based) core. While this version of e300 core does not have a Floating-Point Unit (FPU) it has been designed to include dual integer units as well as a modified multiply instruction. These architectural enhancements enable more efficient operations to be executed in parallel, resulting in significant performance improvement. The core also includes 16 Kbytes of L1 instruction and data caches and on-chip memory management units (MMUs). The MPC8323E also includes a 32-bit PCI controller, four DMA channels, a dedicated security engine, a flexible local bus, and a 32-bit DDR-1/DDR-2 SDRAM memory controller.

A new single-RISC version of the QUICC Engine™ technology forms the heart of the networking capability of the MPC8323E. The QUICC Engine technology contains several peripheral controllers and a 32-bit reduced instruction set computing (RISC) controller. Unique microcode packages provide support for network address translation (NAT), firewall, IPSec, and advanced Quality of Service (QoS). Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs). The QUICC Engine technology provides termination and switching between a wide range of protocols including ATM, Ethernet, TDM, and HDLC. Note that the MPC8321E and MPC8321 do not run ATM on the Utopia interface.

2.1 Block Diagram

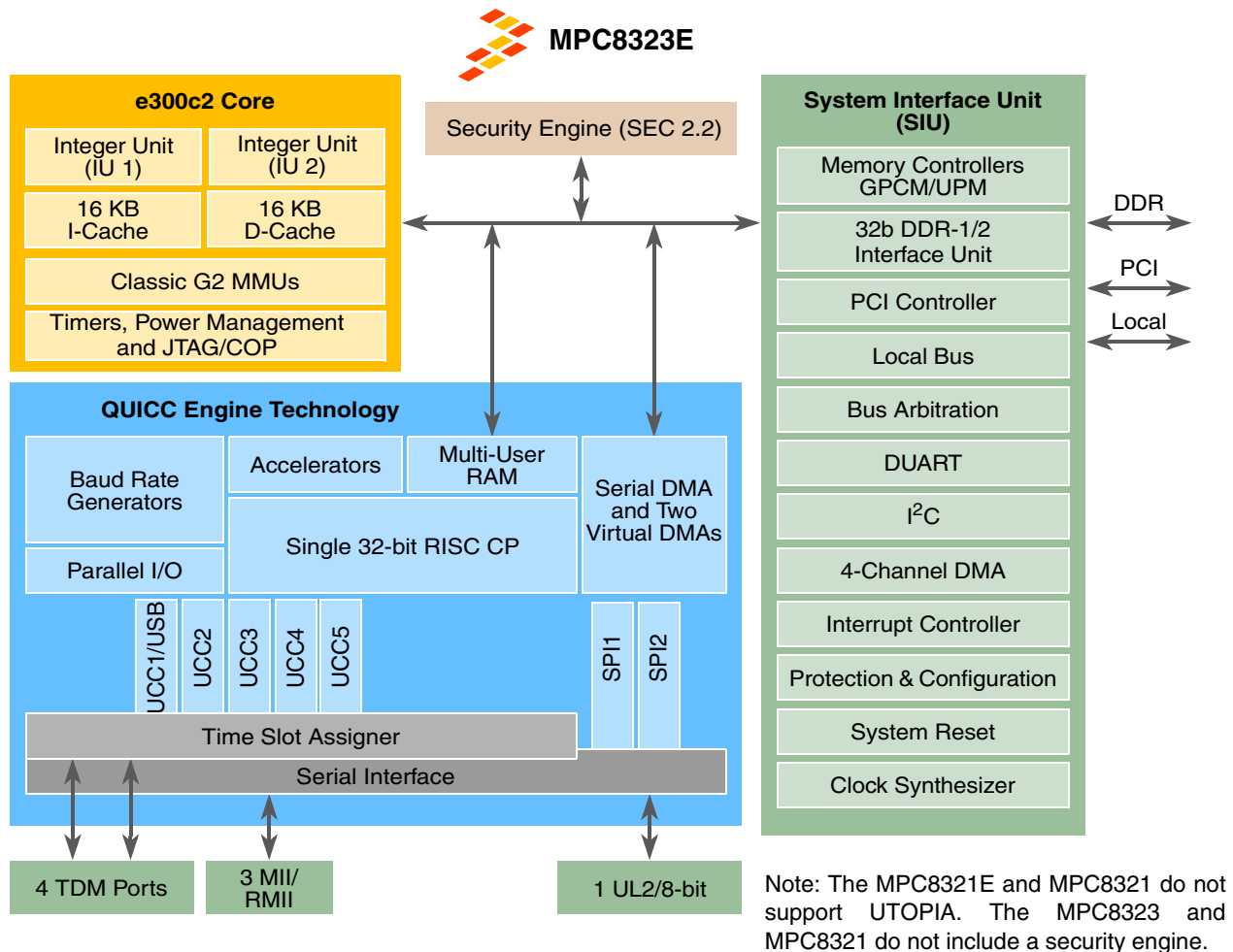A block diagram of the MPC8323E is shown in Figure 3.

Figure 3. MPC8323E Block Diagram

Each of the five UCCs can support a variety of communication protocols: 10/100 Mbps Ethernet, ATM support up to OC-3 speeds, serial ATM, multi-PHY ATM, HDLC, UART, and BISYNC.

In addition, the QUICC Engine technology can support an UTOPIA level 2 capable of supporting 31 multi-PHY. This support is specific to the MPC8323E since the MPC8321E and MPC8321 do not run ATM through the Utopia interface. UCC1 can also support USB 2.0 (full/low speed).

The MPC8323E's security engine (SEC 2.2) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, and MD-5 algorithms.

In summary, the MPC8323E provides users with a highly integrated, fully programmable communications processor. This helps ensure that a low-cost system solution can be quickly developed and will offer flexibility to accommodate new standards and evolving system requirements.

2.2 Chip-Level Features

The PowerQUICC II Pro MPC8323E is a high-performance, highly integrated communication processor solution. The following features are supported in the MPC8323E.

- High-performance, low power, and cost-effective communications processor
- The MPC8323E QUICC Engine technology offers a future-proof solution for next generation designs by supporting programmable protocol termination and network interface termination to meet evolving protocol standards
- Single platform architecture supports the convergence of IP packet networks and ATM networks
- DDR-1/DDR-2 memory controller—one 32-bit interface at up to 266 MHz supporting both DDR-1 and DDR-2
- e300c2 PowerPC core with 16-Kbyte instruction cache and 16-Kbyte data cache, and two integer units
- Peripheral interfaces such as 32-bit PCI interface with up to 66-MHz operation, 16-bit local bus interface with up to 66-MHz operation, and USB 2.0 (full/low speed)
- Security engine provides acceleration for control and data plane security protocols
- High degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration

2.2.1 Protocols

The following protocols are supported in the MPC8323E.

- ATM SAR up to 155 Mbps (OC-3) full duplex, with ATM traffic shaping (ATF TM4.1)
- ATM AAL1 structured and unstructured circuit emulation service (CES 2.0)
- IMA and ATM transmission convergence sub-layer
- ATM OAM handling features compatible with ITU-T I.610
- IP termination support for IPv4 and IPv6 packets including TOS, TTL, and header checksum processing
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics.
- 64 channels of HDLC/transparent

2.2.2 Serial Interfaces

The following serial interfaces are supported in the MPC8323E.

- One UL2 interface with 31 multi-PHY addresses (MPC8323E-specific)
- Up to three 10/100Mbps Ethernet interfaces using MII or RMII
- Up to four T1/E1/J1/E3 or DS-3 serial interfaces
- Dual UART and SPI interfaces, and an I^{2}C interface

System scalability is also made available through the number of UCCs.

2.3 Module Features

2.3.1 QUICC Engine Technology

The QUICC Engine technology is a versatile communications complex that integrates several communications peripheral controllers. It provides on-chip system design for a variety of applications, particularly in communications and networking systems. The QUICC Engine technology has the following features:

- One 32-bit RISC controller for flexible support of the communications peripherals
- Serial DMA channel for receive and transmit on all serial channels
- Five universal communication controllers (UCCs) supporting the following protocols and interfaces (not all of them simultaneously):
  - 10/100 Mbps Ethernet/IEEE Std. 802.3
  - IP support for IPv4 and IPv6 packets including TOS, TTL and header checksum processing
  - ATM protocol through UTOPIA interface (MPC8323E-specific)
  - HDLC /transparent up to 70-Mbps full-duplex
  - HDLC BUS up to 10 Mbps
  - Asynchronous HDLC
  - UART
  - BISYNC up to 2 Mbps
  - QUICC multi-channel controller (QMC) for 64 TDM channels
- One UTOPIA interface supporting 31 multi-PHYs. Note that the MPC8321E and MPC8321 do not run ATM on UTOPIA.
- Two serial peripheral interfaces (SPIs). SPI2 is dedicated to Ethernet PHY management.
- Four TDM interfaces
- 13 independent baud rate generators and 19 input clock pins for supplying clocks to UCC serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers

The UCCs are similar to the PowerQUICC II peripherals: SCC (BISYNC, UART, and HDLC bus), and FCC (fast Ethernet, HDLC, transparent, and ATM).

2.3.2 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, 802.11i, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are:

- Data encryption standard execution unit (DEU), supporting DES and 3DES
- Advanced encryption standard unit (AESU), supporting AES

- Message digest execution unit (MDEU), supporting MD5, SHA1, SHA-256, and HMAC with any algorithm
- One crypto-channel supporting multi-command descriptor chains

2.3.3 DDR Memory Controller

The MPC8323E DDR-1/DDR-2 memory controller includes the following features:

- Single 32-bit interface supporting both DDR-1 and DDR-2 SDRAM
- Support for up to 266-MHz data rate
- Support for two x16 devices
- Support for up to 8 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O
- Support for 256-Mbyte addressing using 2, 128-Mbyte x16 devices

2.3.4 PCI Controller

The MPC8323E PCI controller includes the following features:

- PCI specification Revision 2.2 compatible
- Single 32-bit data PCI interface operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

2.3.5 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model is compatible with the MPC8260 interrupt controller, and it supports 8 external and 27 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

2.3.6 DMA Controller, I^{2}C, DUART, Local Bus Controller, and Timers

The MPC8323E provides an integrated four-channel DMA controller with the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local and remote masters).
- Supports misaligned transfers

There is a single I^{2}C controller. This synchronous, multi-master bus can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. 16-byte FIFOs are supported for both the transmitter and the receiver.

The MPC8323E local bus controller (LBC) port allows connections with a wide variety of external DSPs and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The three user programmable machines (UPMs) can be programmed to interface to synchronous devices or custom ASIC interfaces. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM or UPM controller. Both may exist in the same system. The local bus can operate at up to 66 MHz.

The MPC8323E system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

3   Developer Environment

Development tools, hardware platforms, software building blocks and application-specific software solutions are available from Freescale and our Freescale Alliance Program, including third party protocol and signaling stack suppliers, real time operating systems support, and a variety of applications software support. All of this builds upon the existing industry standard PowerQUICC family support program.

To simplify and accelerate the development process, Freescale will provide a user-friendly, integrated development environment (IDE), which includes a compiler, instruction set simulator, and debugger for the e300c2 PowerPC core.

Freescale also provides an MDS board as a reference platform and programming development environment for the MPC8323E with a complete Linux board support package. The MDS board will support on-board DDR-1/DDR-2 SDRAM memory, a PCI interface, and a debug port and can be configured with optional daughter cards supporting protocols such as OC-3, 4xT1/E1 and Ethernet (10/100Base T).

4   Document Revision History

Table 1 provides a revision history for this product brief.

Table 1. Document Revision History

Rev. No.	Location(s)	Substantive Change(s)
Rev. 0		• Initial revision
Rev. 1	2/4	• Added new information to features.

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