QCVS FAQ Guide

Contents

1 Introduction

This guide lists most frequently asked questions (FAQs) about QorIQ Configuration and Validation Suite (QCVS).

The questions are divided into the following categories:

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2 Product installation

This section describes how to resolve the issues that appear during the installation of the QCVS product.

While installing QCVS, you might encounter the following problems:

- I tried to install QCVS into CodeWarrior for Power Architecture on Windows Vista/7/8. The installation process stopped with the following error messages: on page 1
- I tried to install QCVS into CodeWarrior for Power Architecture on Linux. I got this (or similar) error message during installation: on page 2
- I installed QorIQ Configuration and Validation Suite into CodeWarrior for Power Architecture on Windows Vista / Windows 7. The installation process finished without any errors. However, QorIQ Configuration and Validation Suite does not work. on page 2
- I have an RCW obtained with an older version of QCS and when I import it back into the tool I get errors. How can I continue working with that RCW? on page 3

2.1 I tried to install QCVS into CodeWarrior for Power Architecture on Windows Vista/7/8. The installation process stopped with the following error messages:

```
An error occurred while installing the items session context was:
(profile=PlatformProfile, phase=org.eclipse.equinox.internal.p2.engine.phases.Install,
operand=null --> [R]com.freescale.processorexpert.feature.QCVS_root <QCVS version>,
action=com.freescale.updater.customactions.actions.FreescaleInstall). Target: Path could not
be created
```

The reason is that you did not have administrator privileges when you installed QCVS. This particular error occurs when you have installed CodeWarrior in some administrator location (such as, the `Program Files` folder) on Windows Vista/7/8. To successfully install QCVS, follow these steps:

I tried to install QCVS into CodeWarrior for Power Architecture on Linux. I got this (or similar) error message during installation:

1. Log off from Windows.
2. Log in to Windows as an administrator.
3. Install QCVS.
4. Do not restart CodeWarrior after installation, quit it, log off from Windows, and log in to Windows using your original (non-administrator) credentials.

2.2 I tried to install QCVS into CodeWarrior for Power Architecture on Linux. I got this (or similar) error message during installation:

```
An error occurred while installing the items session context was:
(profile=PlatformProfile, phase=org.eclipse.equinox.internal.p2.engine.phases.Install,
operand=null --> [R]com.freescale.processorexpert.feature.QCVS_root <QCVS version>,
action=com.freescale.updater.customactions.actions.FreescaleInstall). Target: Path
<Path> could not be created
```

The reason is that you did not have administrator privileges when you installed QCVS. This particular error occurs when you install CodeWarrior in some root location, for example, */usr/lib*. To successfully install QCVS, follow these steps:

1. Run CodeWarrior with administrator (root) permissions (`sudo ./cwide`).
2. Install QCVS.
3. Do not restart CodeWarrior after installation, quit it, and run it again using your original (non-root) credentials.

2.3 I installed QorIQ Configuration and Validation Suite into CodeWarrior for Power Architecture on Windows Vista / Windows 7. The installation process finished without any errors. However, QorIQ Configuration and Validation Suite does not work.

If you receive the following (or similar) error message while creating a new project after you installed QorIQ Configuration and Validation Suite, it means you did not use administrator permissions during installation. This particular error occurs when you have CodeWarrior installed in the `Program Files` folder on Windows Vista / Windows 7.

```
Generator: INTERNAL ERROR: at line : Error in including "<component>.drv" (file: Drivers
\<component>.src)
```

and/or,

```
INTERNAL ERROR: at line <line number>: %launchExt failed with the following error:
LaunchExtObject.LoadLibrary: not possible to load requested library...
```

To fix the issue, perform the following steps:

1. Uninstall QorIQ Configuration and Validation Suite.
2. Run CodeWarrior with administrator permissions and install QorIQ Configuration and Validation Suite using the following steps:

a. Open Windows Explorer and navigate to the <*CodeWarrior installation folder*>*eclipse* folder.
b. Right-click `cwide.exe` and select the **Run as administrator** option.
c. Enter administrator login ID and password in the administrator login dialog. If the administrator login dialog does not appear, quit CodeWarrior, log off from Windows, and log in as administrator.
d. Install QorIQ Configuration and Validation Suite.
e. Do not restart CodeWarrior after the installation, quit it, and run it again with your original (non-administrator) credentials.

2.4 I have an RCW obtained with an older version of QCS and when I import it back into the tool I get errors. How can I continue working with that RCW?

The errors are probably due to new errata constraints this QCVS version now supports. The errors can be ignored by clicking the small triangle (View Menu) on the top right corner of the **Component Inspector** view and choosing **Ignore Constraints and non-Critical Errors**. However, we strongly recommend you to rather adjust the configuration to address the errors.

3 DDR tool

This section provides FAQs related to the DDR tool of the QCVS product.

The questions are listed below:

3.1 What is the difference between data eye and margin table?

A data eye is an eye shape pattern generated by setting an oscilloscope to infinite-persistent display mode, and DQ signal is captured while DQ value is changed from 1 to 0 and from 0 to 1 repeated for a period of time. The scope is usually triggered on the strobe signal (DQS) indicating where the sampling of DQ takes place within the data eye. A scope-captured data eye cannot identify the passing or failing regions within the data eye. The read or write margin table is the pass/fail based reconstruction of data eye with the location of strobe selected by memory controller during the initialization. The margin table identifies the passing or failing regions within the data eye of the DDR interface.

3.2 What are the limitations of data eye captured by an oscilloscope?

A scope data eye does not have any pass or fail information. The best scope captured is at the pin of the DRAM or memory controller that is still considered as middle of the data bus transmission line. With data rates exceeding GHz, the complexity of non-intrusive measurement becomes impossible. The equipment is costly and it can only measure limited number of signals. In addition, it is time consuming to set up and capture meaningful data with an oscilloscope.

3.3 What are the advantages of using the read/write margin validation scenario?

Running a margin scenario provides the pass and fail information of data bus. It reconstructs the pseudo data eye to the true end of the transmission line. It is simple to set up and it is relatively inexpensive. In addition, it provides meaningful information about the DDR interface very quickly and with minimum setup.

3.4 Why and when is margin table useful?

Deciding the functionality of the DDR interface is the first step for any DDR interface design. When you have a functional DDR interface, you would like to know how much timing margin is available, it means, after how much time the DDR interface is expected to fail. A functional DDR interface with zero timing margin would be more susceptible to failures at some point during its operation.

3.5 How much margin is good or acceptable?

The more timing margin is available, the more stable the interface would be. However, having one or two passing (light green) timing steps on both sides of the selected strobe location (bright green cell) is considered as good or acceptable.

3.6 What information do the green cells in read/write margin table provide?

These are the cells that have passed the direct memory access (DMA) test. The validation sweeps the strobe signal in the data eye for each byte lane and at each timing step during the sweep, a stress DMA test is conducted to check for pass or fail. When the DMA test is passed, the corresponding cell/timing step is marked as green.

3.7 What information do the bright green cells in the margin table provide?

The bright green cells are where the memory controller has placed the strobe signal crossing to sample the data during the initialization.

3.8 Are the margin tables same as the setup and hold timing parameter for memory controller?

No, the margin table displays the passing and failing regions within the data eye in the DDR interface. The passing region satisfies the required setup and hold time for all components of DDR interface, including the setup and hold time for memory controller, DRAM, and degradation of the board.

3.9 Why is the controller selected strobe location not in the middle of passing region?

The controller determines the best possible strobe location during the initialization. The tests conducted by software and controller may differ; therefore, the strobe location may not always fall exactly in the middle of the passing region determined by software means.

3.10 The location of strobe is not in the center of passing region, can I manually move it to center?

No, manual selection of strobe location is not available. This is because a fixed setting that seems to be ideal setting cannot change and adapt itself to each individual board conditions or variations. However, the controller auto calibration will take place on each individual board and it has an auto tracking capability to adjust itself as board conditions vary during operation. Therefore, the location of strobe selected by the memory controller does not seem to be ideal in the margin table, it is considered to be much better than manual selection.

The result I get after running the margin scenario shows that I have a very low passing margin. Is it because of a bad memory controller?

3.11 The result I get after running the margin scenario shows that I have a very low passing margin. Is it because of a bad memory controller?

No, if the margin table shows one or two timing steps on both sides of the selected strobe location in the passing region, then that would be acceptable or good margin. If that is not the case and no margin is available, then the DDR interface on the board under the test would be considered to have low margin. The size of the passing margin would depend on all the components in the DDR interface, including memory controller, DRAM, and board (interconnect). Freescale has tested the memory controller with the same margin tool and has got acceptable passing region in its reference design boards. If low passing margin is observed on several boards, then the boards can be examined for showing low margin.

3.12 On Linux, I get connection errors when I click Read SPD in the DDR component wizard, or when I try to run a DDR validation.

Before executing QCVS, run the *\eclipse\Optimization\target-connection\cdde\cdde-linux\bin\createlinks_xpcom.sh* script. Then, ensure to start Eclipse with `sudo` rights, as follows:

```
sudo ./eclipse
```

3.13 How can I run DDR validation multiple times in a row?

On the **Validation** page of **Component Inspector**, select the scenarios you want to run and click the **Start Validation** button to perform validation. After all the scenarios have been validated, click the **Revert to initial DDR configuration** button (highlighted in the figure below) to revert to the DDR configuration from where you started the previous validation, and then click the **Start Validation** button again to rerun validation starting from the same initial DDR configuration.

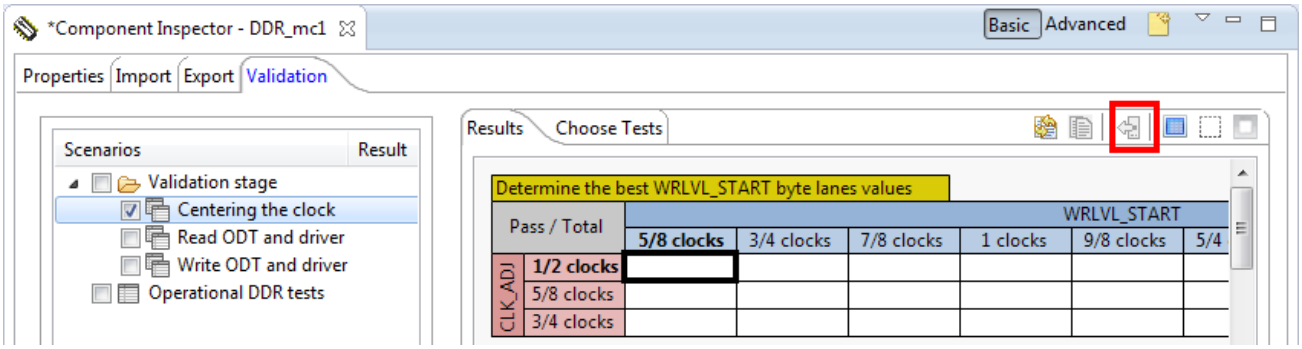

Figure 1. Reverting to initial DDR configuration

4 PBL tool

This section provides FAQ related to the PBL tool of the QCVS product.

The question is listed below:

4.1 PBI command CRC does not work with the Stop command on LS2080, LS2085, LS2088, and LS1088 (NSEC=1).

For non-secure devices (devices having NSEC fuse blown to 1), including all versions and personalities of LS2080, LS2085, LS2088, and LS1088, pre-boot initialization (PBI) command CRC (cyclic redundancy check) does not work with the Stop command due to a hardware erratum. The QCVS PBL tool issues a warning if it detects that the current device is impacted by this limitation. The workaround is to disable CRC in the final Stop command and use only Stop command to terminate the sequence of PBI commands.

If you create a QorIQ configuration project with a non-secure device and PBL component and set the **CRC in final Stop command** property of the PBL component to “yes”, then you will receive a warning. The warning disappears when you set the **CRC in final Stop command** property to “no”. The steps are as follows:

1. Import your pre-boot loader (PBL) configuration having the faulty reset configuration word (RCW) into the QCVS tool. See QCVS PBL Tool User Guide for more details.
2. If the PBI Stop command is not added automatically, then add it by editing the **PBI Data input** property on the **Properties** page of **Component Inspector**, as shown in the figure below.

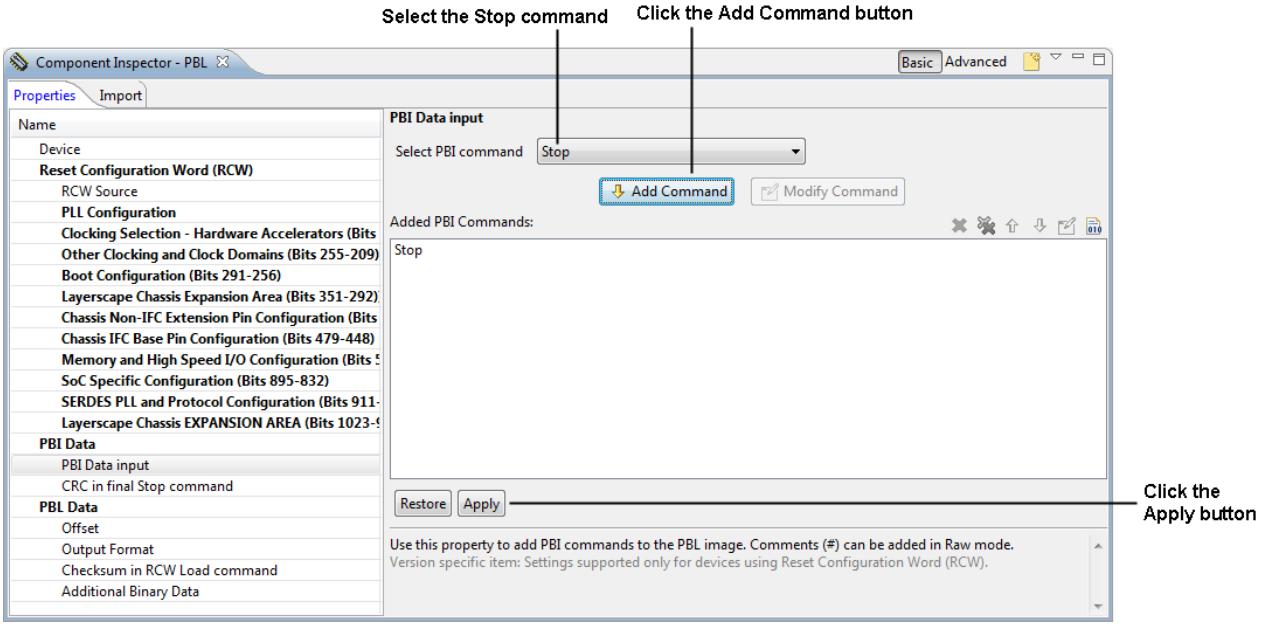

Figure 2. Adding Stop command

The **CRC in final Stop command** property is set to “yes”, by default. It means, CRC is generated after the final Stop command, by default. With the default setting of the **CRC in final Stop command** property, a warning message is displayed for the devices with NSEC = 1. The warning message is displayed in the **Details** column of the **Properties** page and in the **Problems** view, as shown in the figure below.

PBL tool

PBI command CRC does not work with the Stop command on LS2080, LS2085, LS2088, and LS1088 (NSEC=1).

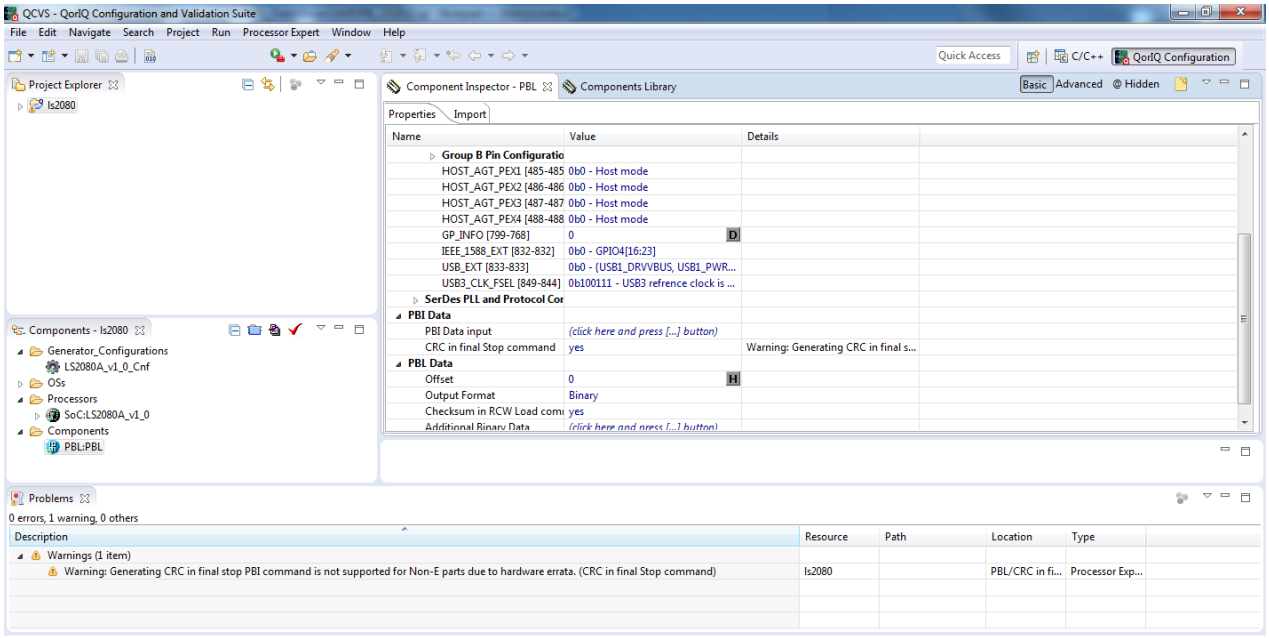

Figure 3. CRC warning

3. For devices with NSEC = 1, set the **CRC in final Stop command** property to “no”. The warning message disappears.
4. Regenerate RCW.

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