DSP56300FMAD
Rev. 6, 9/2008

DSP56300 Family Manual Addendum

This document provides updated information for revision 5 of the *DSP56300 Family Manual (DSP56300FM/AD)*. The updates include the following:

- Modified **Figure 6-5** to reflect the differences in core voltages across the product family.
- Modified assembler syntax font to improve readability for the ASL instruction.
- Modified assembler syntax font to improve readability for the ASR instruction.

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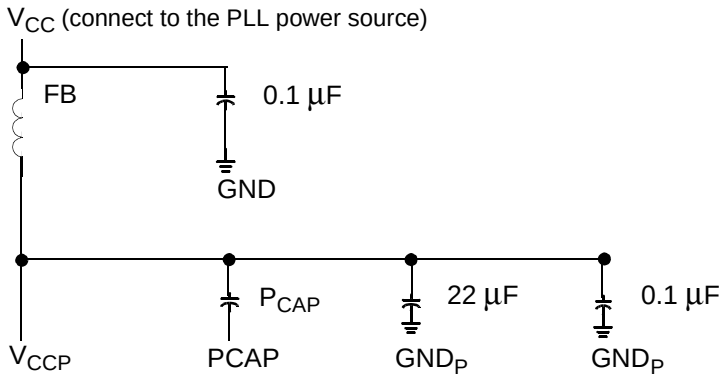
1 Recommended PLL Filter Circuit

Area to Change	Change Description
Chapter 6, PLL and Clock Generator, p. 6-11	Replace **Figure 6-5** with the following diagram.



Notes:
1. FB = Ferrite Bead with 600 Ω impedance at 100 MHz, 12 Ω at DC.
2. PCAP value calculated according to the product specific data sheet.
3. Some DSP56300 devices use power supplies for the cores and PLLs that differ from the device I/O voltage. Some contain PLLs that use different source voltages. Always connect FB to the specific power source for the PLL being protected. Refer to the individual product data sheet for details.

Figure 6-5. PLL Filter Circuit

2 ASL Instruction Assembler Syntax

Area to Change	Change Description
Chapter 13, ASL description, p. 13-14	After the heading **Assembler Syntax**, replace the indented text with the following: ASL D (parallel move) ASL #ii,S2,D ASL S1,S2,D **Note:** This is a font change only to assist in readability.

3 ASR Instruction Assembler Syntax

Area to Change	Change Description
Chapter 13, ASR description, p. 13-16	After the heading **Assembler Syntax**, replace the indented text with the following: ASR D (parallel move) ASR #ii,S2,D ASR S1,S2,D **Note:** This is a font change only to assist in readability.

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