MC13783 Information for GPL Drivers

Reference Manual

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Appendix A
MC13783 SPI Bitmap

About This Book

This document presents information on the mono processor (single SPI) application for the MC13783. The MC13783 is the audio and power management part that forms part of the Freescale Semiconductor i.2xx, i.3xx and MXC platforms. This power management and audio IC can also be used with the i.MX product family.

Audience

This document is intended for the:

- Hardware validation team
- Engineer software design team
- Phone product engineering team
- PMP product engineering team

Organization

This document is organized by the following chapters:

Chapter 1	Programmability
Chapter 2	Clock Generation and Real Time Clock
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Revision History

The following table summarizes revisions to this document since the previous release (Rev. 1.0).

Revision History

Location	Revision
Throughout document	Revised iCAP classification.
Preface	Deleted Suggested Reading document: MXC Electro-Acoustic Design Guidelines Application Note, Document Number: AN3243.
Appendix A	Added Appendix A - SPI Table.

Suggested Reading

- *MC13783 Data Sheet*, Document Number: MC13783/D, Freescale Semiconductor.
- *External Component Recommendations for the MC13783 Reference Design Application Note*, Document Number: AN3295, Freescale Semiconductor.
- *MC13783 Buck and Boost Inductor Sizing Application Note*, Document Number: AN3294, Freescale Semiconductor.
- *Interfacing the MC13783 Power Management IC with i.MX31 Applications Processors Application Note*, Document Number: AN3276, Freescale Semiconductor.
- *MC13783 Recommended Audio Output SPI Sequences Application Note*, Document Number: AN3261, Freescale Semiconductor.
- *Voltage Drop Compensation on the MC13783 Switchers Line Application Note*, Document Number: AN3249, Freescale Semiconductor.
- *Battery Management for the MC13783 Application Note*, Document Number: AN3155, Freescale Semiconductor.

Definitions, Acronyms, and Abbreviations

PMIC	Power Management Integrated Circuit
ADC	Analog to Digital Converters
DAC	Digital to Analog Converter
SSI	Serial Standard Interface
SPI	Serial Peripheral Interface
RTC	Real Time Clock
GPO	General Purpose Outputs
PWM	Pulse Width Modulation
PFM	Pulse Frequency Modulation
PLL	Phase Locked Loop
PSRR	Power Supply Rejection Ratio
ESR	Equivalent Serial Resistance

References

The following sources were referenced to produce this book:

- *MC13783 DTS*, Freescale Semiconductor.

Chapter 1
Programmability

1.1 SPI Interface

The MC13783 IC contains a SPI interface port. The SPI port is configured to utilize 32-bit serial data words, using 1 read/write bit, 6 address bits, 1 null bit, and 24 data bits. The SPI port's 64 registers correspond to the 6 address bits.

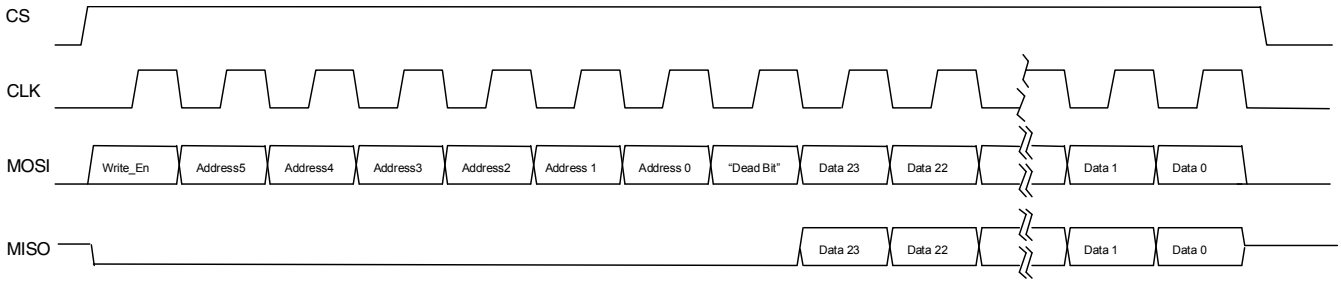

Figure 1-1. SPI Transfer Protocol Single Read/Write Access

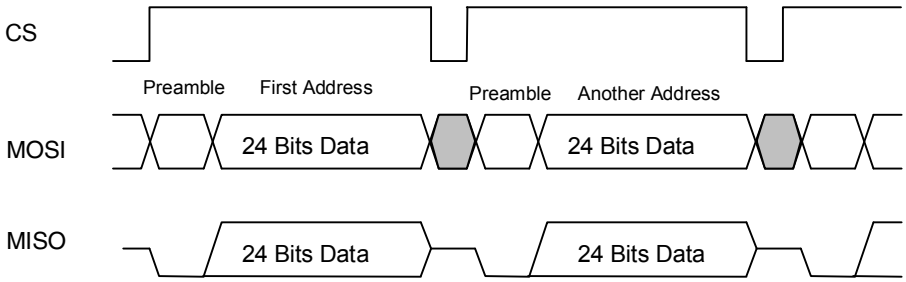

Figure 1-2. SPI Transfer Protocol Multiple Read/Write Access

Table 1-1. Register Set

Register		Register		Register		Register	
0	Interrupt Status 0	16	Regen Assignment	32	Regulator Mode 0	48	Charger
1	Interrupt Mask 0	17	Control Spare	33	Regulator Mode 1	49	USB 0
2	Interrupt Sense 0	18	Memory A	34	Power Miscellaneous	50	Charger USB 1
3	Interrupt Status 1	19	Memory B	35	Power Spare	51	LED Control 0
4	Interrupt Mask 1	20	RTC Time	36	Audio Rx 0	52	LED Control 1
5	Interrupt Sense 1	21	RTC Alarm	37	Audio Rx 1	53	LED Control 2
6	Power Up Mode Sense	22	RTC Day	38	Audio Tx	54	LED Control 3

Table 1-1. Register Set (continued)

Register		Register		Register		Register	
7	Identification	23	RTC Day Alarm	39	SSI Network	55	LED Control 4
8	Semaphore	24	Switchers 0	40	Audio CODEC	56	LED Control 5
9	Arbitration Peripheral Audio	25	Switchers 1	41	Audio Stereo DAC	57	Spare
10	Arbitration Switchers	26	Switchers 2	42	Audio Spare	58	Trim 0
11	Arbitration Regulators 0	27	Switchers 3	43	ADC 0	59	Trim 1
12	Arbitration Regulators 1	28	Switchers 4	44	ADC 1	60	Test 0
13	Power Control 0	29	Switchers 5	45	ADC 2	61	Test 1
14	Power Control 1	30	Regulator Setting 0	46	ADC 3	62	Test 2
15	Power Control 2	31	Regulator Setting 1	47	ADC 4	63	Test 3

1.2 SPI Arbitration

The complete SPI bitmap of the MC13783 is given below with one register per row for a general overview. The color coding indicates the SPI access mechanism according the following scheme:

Pale Green = Write and Read access for Primary SPI only

Pale Blue = Write and Read access for one of the SPIs

Light Blue = Write access for one of the SPIs, read access for both SPIs

Pale Orange = No write access, Read access for both SPIs

Pale Purple = Write and Read access for both SPIs

Lavender = PRI only, access with ICTEST is high

Reserved = Bits available but not assigned

White and empty = Non available bits

The SPI access mechanism can be represented graphically as shown in Figure 1-3. The color coding scheme is used with the exception of registers reading back all 0 which are colored white.

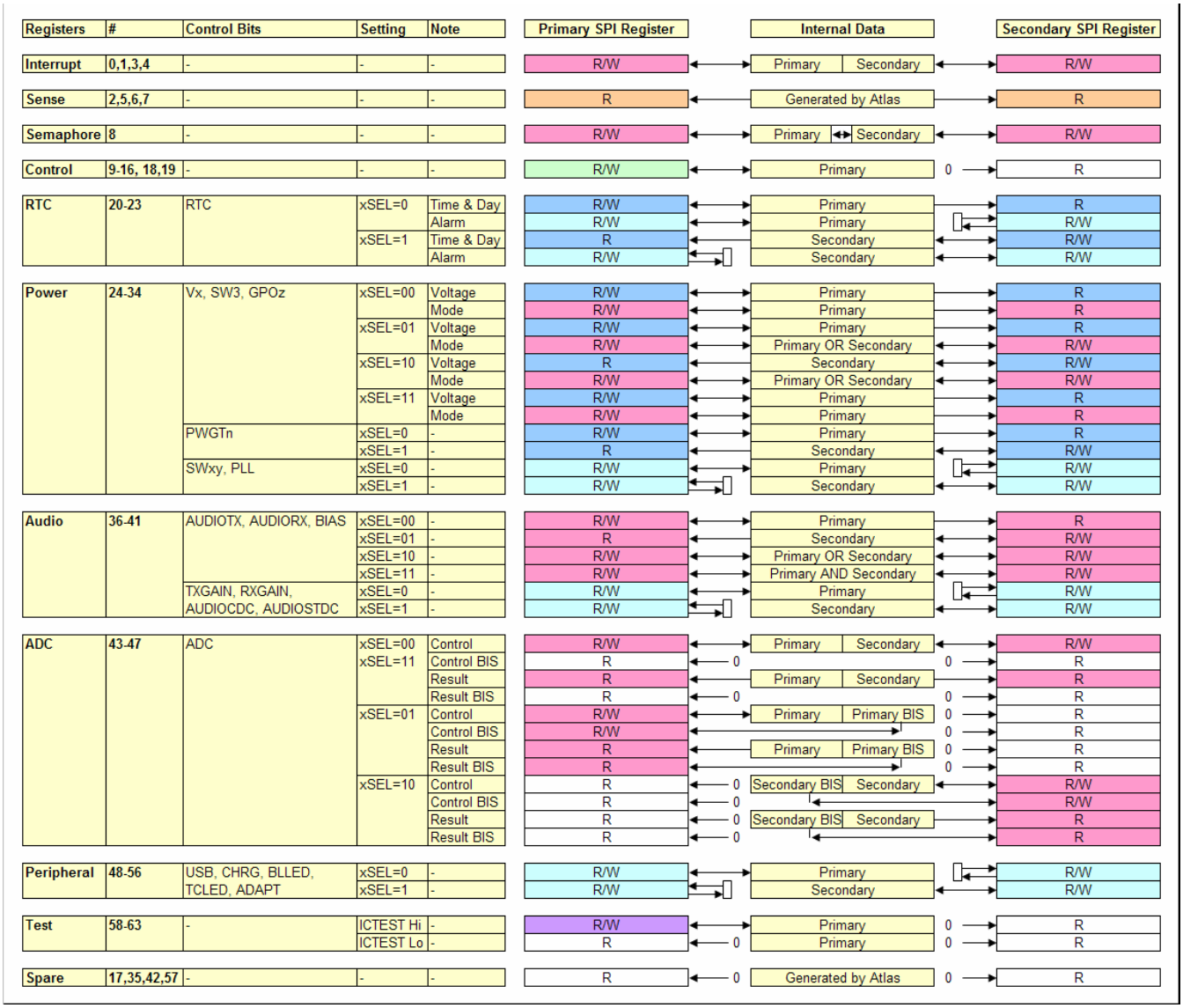

Figure 1-3. SPI Access Mechanism

In single processor configurations, the MC13783 SPI resources do not have to be shared and access control is not required. In that case, the processor has to communicate via the PRISPI bus where it has direct access to the register base. At startup, all resources, (bits or bit vectors within a SPI register) are readable and writable via the primary SPI interface while in general the secondary SPI bus has a read access only. Keep the arbitration SPI bits at reset state to guarantee correct behavior in the mono SPI operation.

1.2.1 Arbitration SPI bits

Table 1-2. Register 8, Semaphore

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
SEMCTRLA	0	R/W	RESETB	0	Semaphore control word A
Reserved	1	R/W	RESETB	0	For future use
SEMCTRLB	2	R/W	RESETB	0	Semaphore control word B
Reserved	3	R/W	RESETB	0	For future use
SEMWRTA0	4	R/W	RESETB	0	Semaphore write word A
SEMWRTA1	5	R/W	RESETB	0	
SEMWRTA2	6	R/W	RESETB	0	
SEMWRTA3	7	R/W	RESETB	0	
SEMWRTB0	8	R/W	RESETB	0	Semaphore write word B
SEMWRTB1	9	R/W	RESETB	0	
SEMWRTB2	10	R/W	RESETB	0	
SEMWRTB3	11	R/W	RESETB	0	
SEMWRTB4	12	R/W	RESETB	0	
SEMWRTB5	13	R/W	RESETB	0	
SEMRDA0	14	R/W	RESETB	0	Semaphore read word A other SPI
SEMRDA1	15	R/W	RESETB	0	
SEMRDA2	16	R/W	RESETB	0	
SEMRDA3	17	R/W	RESETB	0	
SEMRDB0	18	R/W	RESETB	0	Semaphore read word B other SPI
SEMRDB1	19	R/W	RESETB	0	
SEMRDB2	20	R/W	RESETB	0	
SEMRDB3	21	R/W	RESETB	0	
SEMRDB4	22	R/W	RESETB	0	
SEMRDB5	23	R/W	RESETB	0	

Table 1-3. Register 9, Arbitration Peripheral Audio

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
AUDIOTXSEL0	0	R/W	RESETB	0	Transmit audio amplifiers assignment Set 00 for mono SPI
AUDIOTXSEL1	1	R/W	RESETB	0	
TXGAINSEL	2	R/W	RESETB	0	Transmit gain assignment Set 00 for mono SPI

Table 1-3. Register 9, Arbitration Peripheral Audio (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
AUDIORXSEL0	3	R/W	RESETB	0	Receive audio amplifiers assignment Set 00 for mono SPI
AUDIORXSEL1	4	R/W	RESETB	0	
RXGAINSEL	5	R/W	RESETB	0	Receive gain assignment Set 00 for mono SPI
AUDIOCDCSEL	6	R/W	RESETB	0	Voice CODEC assignment Set 00 for mono SPI
AUDIOSTDCSEL	7	R/W	RESETB	0	Stereo DAC assignment Set 00 for mono SPI
BIASSEL0	8	R/W	RESETB	0	Audio bias assignment Set 00 for mono SPI
BIASSEL1	9	R/W	RESETB	0	
Reserved	10	R/W	RESETB	0	For future use
RTCSEL	11	R/W	RESETB	0	RTC write assignment Set 0 for mono SPI
ADCSEL0	12	R/W	RESETB	0	ADC assignment Set 01 for mono SPI. Prispi can queue 2 ADC requests
ADCSEL1	13	R/W	RESETB	0	
USBSEL	14	R/W	RESETB	0	USB assignment Set 0 for mono SPI
CHRGSEL	15	R/W	RESETB	0	Charger assignment Set 0 for mono SPI
BLLEDSEL	16	R/W	RESETB	0	Backlight LED assignment Set 0 for mono SPI
TCLEDSEL	17	R/W	RESETB	0	Tricolor LED assignment Set 0 for mono SPI
ADAPTSEL	18	R/W	RESETB	0	Adaptive boost assignment Set 0 for mono SPI
Reserved	19	R/W	RESETB	0	For future use
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Table 1-4. Register 10, Arbitration Switchers

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
SW1ASTBYAND	0	R/W	RESETB	0	Both standby pins control SW1A Set 0 for STANDBYPRI control Set 1 for STANDBYPRI and STANDBYSEC control
SW1BSTBYAND	1	R/W	RESETB	0	Both standby pins control SW1B Set 0 for STANDBYPRI control Set 1 for STANDBYPRI and STANDBYSEC control
SW2ASTBYAND	2	R/W	RESETB	0	Both standby pins control SW2A Set 0 for STANDBYPRI control Set 1 for STANDBYPRI and STANDBYSEC control
SW2BSTBYAND	3	R/W	RESETB	0	Both standby pins control SW2B Set 0 for STANDBYPRI control Set 1 for STANDBYPRI and STANDBYSEC control
SW3SEL0	4	R/W	RESETB	0	SW3 assignment bit 0 Set 0 for mono SPI
SW1ABDVS	5	R/W	RESETB	0	Two DVS pins control SW1 0: DVSSW1A controls SW1A 1: DVSSW1A and DVSSW1B control SW1
SW2ABDVS	6	R/W	RESETB	0	Two DVS pins control SW2 0: DVSSW2A controls SW2A 1: DVSSW2A and DVSSW2B control SW2
SW1ASEL	7	R/W	RESETB	0	SW1A assignment Set 0 for mono SPI
SW1BSEL	8	R/W	RESETB	0	SW1B assignment Set 0 for mono SPI
SW2ASEL	9	R/W	RESETB	0	SW2A assignment Set 0 for mono SPI
SW2BSEL	10	R/W	RESETB	0	SW2B assignment Set 0 for mono SPI
SW3SEL1	11	R/W	RESETB	0	SW3 assignment bit 1 Set 0 for mono SPI
PLLSEL	12	R/W	RESETB	0	Switcher PLL assignment Set 0 for mono SPI
Reserved	13	R/W	RESETB	0	For future use
PWGT1SEL	14	R/W	RESETB	0	Power gate 1 assignment Set 0 for mono SPI
PWGT2SEL	15	R/W	RESETB	0	Power gate 2 assignment Set 0 for mono SPI
Reserved	16	R/W	RESETB	0	For future use
Unused	17	R		0	Not available
Unused	18	R		0	Not available

Table 1-4. Register 10, Arbitration Switchers (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Table 1-5. Register 11, Arbitration Regulators 0

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
VAUDIOSEL0	0	R/W	RESETB	0	VAUDIO assignment Set 00 for mono SPI
VAUDIOSEL1	1	R/W	RESETB	0	
VIOHISEL0	2	R/W	RESETB	0	VIOHI assignment Set 00 for mono SPI
VIOHISEL1	3	R/W	RESETB	0	
VIOLOSEL0	4	R/W	RESETB	0	VIOLO assignment Set 00 for mono SPI
VIOLOSEL1	5	R/W	RESETB	0	
VDIGSEL0	6	R/W	RESETB	0	VDIG assignment Set 00 for mono SPI
VDIGSEL1	7	R/W	RESETB	0	
VGENSEL0	8	R/W	RESETB	0	VGEN assignment Set 00 for mono SPI
VGENSEL1	9	R/W	RESETB	0	
VRFDIGSEL0	10	R/W	RESETB	0	VRFDIG assignment Set 00 for mono SPI
VRFDIGSEL1	11	R/W	RESETB	0	
VRFREFSEL0	12	R/W	RESETB	0	VRFREF assignment Set 00 for mono SPI
VRFREFSEL1	13	R/W	RESETB	0	
VRFCPSEL0	14	R/W	RESETB	0	VRFCP assignment Set 00 for mono SPI
VRFCPSEL1	15	R/W	RESETB	0	
VSIMSEL0	16	R/W	RESETB	0	VSIM assignment Set 00 for mono SPI
VSIMSEL1	17	R/W	RESETB	0	
VESIMSEL0	18	R/W	RESETB	0	VESIM assignment Set 00 for mono SPI
VESIMSEL1	19	R/W	RESETB	0	
VCAMSEL0	20	R/W	RESETB	0	VCAM assignment Set 00 for mono SPI
VCAMSEL1	21	R/W	RESETB	0	
VRFBGSEL0	22	R/W	RESETB	0	VRFBG assignment Set 00 for mono SPI
VRFBGSEL1	23	R/W	RESETB	0	

Table 1-6. Register 12, Arbitration Regulators 1

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
VVIBSEL0	0	R/W	RESETB	0	VVIB assignment Set 00 for mono SPI
VVIBSEL1	1	R/W	RESETB	0	
VRF1SEL0	2	R/W	RESETB	0	VRF1 assignment Set 00 for mono SPI
VRF1SEL1	3	R/W	RESETB	0	
VRF2SEL0	4	R/W	RESETB	0	VRF2 assignment Set 00 for mono SPI
VRF2SEL1	5	R/W	RESETB	0	
VMMC1SEL0	6	R/W	RESETB	0	VMMC1 assignment Set 00 for mono SPI
VMMC1SEL1	7	R/W	RESETB	0	
VMMC2SEL0	8	R/W	RESETB	0	VMMC2 assignment Set 00 for mono SPI
VMMC2SEL1	9	R/W	RESETB	0	
Reserved	10	R/W	RESETB	0	For future use
Reserved	11	R/W	RESETB	0	For future use
Reserved	12	R/W	RESETB	0	For future use
Reserved	13	R/W	RESETB	0	For future use
GPO1SEL0	14	R/W	RESETB	0	GPO1 assignment Set 00 for mono SPI
GPO1SEL1	15	R/W	RESETB	0	
GPO2SEL0	16	R/W	RESETB	0	GPO2 assignment Set 00 for mono SPI
GPO2SEL1	17	R/W	RESETB	0	
GPO3SEL0	18	R/W	RESETB	0	GPO3 assignment Set 00 for mono SPI
GPO3SEL1	19	R/W	RESETB	0	
GPO4SEL0	20	R/W	RESETB	0	GPO4 assignment Set 00 for mono SPI
GPO4SEL1	21	R/W	RESETB	0	
Unused	22	R		0	Not available
Unused	23	R		0	Not available

1.3 Interrupt Handling

The MC13783 has interrupt generation capability to inform the system on important events occurring. An interrupt is signaled to the processors connected to the primary SPI by driving the PRIINT line high.

Each interrupt is latched so that even if the interrupt source becomes inactive, the interrupt will remain active until cleared. Each interrupt can be cleared by a SPI bus by writing a 1 to the appropriate bit in the Interrupt Status register, this will also cause the interrupt line to go low for that SPI bus. If a new interrupt occurs while the processor clears an existing interrupt bit, the interrupt line will remain high. Clearing an interrupt bit on one SPI bus will not clear the interrupt bit on the other SPI bus.

Each interrupt can be masked by setting the corresponding mask bit to a 1. As a result, when the interrupt bit goes high, the interrupt line will not go high. However, even when the interrupt is masked, the interrupt source can still be read from the Interrupt Status register. This gives the processor the option of polling for status from the MC13783. The MC13783 powers up with all interrupts masked, so the processor must initially poll the MC13783 to determine if any interrupts are active. Alternatively, the processor can later unmask the interrupt bits of interest. If the related interrupt bit was already high, the interrupt line will go high after the unmasking. All mask bits labeled as reserved in the SPI bitmap do default to a 1 and should not be programmed to 0.

The MC13783 sense registers contain status and input sense bits. These bits provide information to the processor about specific MC13783 IO, power on inputs and power up sources. They only represent the current status of the sources, and thus are not latched, and are not clearable. The values in this register are read only.

Table 1-7 summarizes all interrupt, mask and sense bits. Although the polarity of the sense bits is given.

Table 1-7. Interrupt, Mask and Sense Bits

Interrupt	Mask	Sense	Used for / Sense Bit Polarity	Trigger
ADCDONEI	ADCDONEM	-	ADC has finished requested conversions	L2H
ADCBISDONEI	ADCBISDONEM	-	ADCBIS has finished requested conversions	L2H
TSI	TSM	-	Touchscreen wake up	Dual
WHIGHI	WHIGHM	-	ADC reading above high limit	L2H
WLOWI	WLOWM	-	ADC reading below low limit	L2H
CHGDETI	CHGDETM	CHGDETS	Charger attach and removal Sense is 1 if above threshold	Dual
CHGOVI	CHGOVM	CHGOVS	Charger over voltage detection Sense is 1 if above threshold	Dual
CHGREVI	CHGREVM	CHGREVS	Charger path reverse current Sense is 1 if current flows into phone	L2H
CHGSHORTI	CHGSHORTM	CHGSHORTS	Charger path short circuit Sense is 1 if above threshold	L2H
CCCVI	CCCVM	CCCVS	Charger regulator operating mode Sense is 1 if voltage regulation	Dual
CHGCURRI	CHGCURRM	CHGCURRS	Charge current below threshold Sense is 1 if above threshold	H2L
BPONI	BPONM	BPONS	BP turn on threshold detection Sense is 1 if above threshold	L2H
LOBATLI	LOBATLM	LOBATLS	End of life / low battery detect Sense is 1 if end of life detected Sense is 1 if below low battery threshold	L2H
LOBATHI	LOBATHM	LOBATHS	Low battery warning Sense is 1 if above threshold	Dual
USBI	USBM	USB4V4S	USB 4V4 detect Sense is 1 if above threshold	Dual

Table 1-7. Interrupt, Mask and Sense Bits (continued)

Interrupt	Mask	Sense	Used for / Sense Bit Polarity	Trigger
-	-	USB2V0S	USB 2V0 detect Sense is 1 if above threshold	Dual
-	-	USB0V8S	USB 0V8 detect Sense is 1 if above threshold	Dual
UDPI	UDPM	UDPS	UDP detect Sense is 1 if pin is high	L2H
UDMI	UDMM	UDMS	UDM detect Sense is 1 if pin is high	L2H
IDI	IDM	IDFLOATS	USB ID Line detect Sense bits are coded, see related chapter	Dual
-	-	IDGNDS		
SE1I	SE1M	SE1S	Single ended 1 detect Sense is 1 if detected	Dual
CKDETI	CKDETM	CKDETS	Carkit detect Sense is 1 if detected	L2H
MC2BI	MC2BM	MC2BS	Microphone bias 2 detect Sense is 1 if detected	Dual
HSDETI	HSDETM	HSDETS	Headset attach Sense is 1 if attached	Dual
HSLI	HSLM	HSLS	Stereo headset detect Sense is 1 if detected	L2H
ALSPTHI	ALSPTHM	ALSPTHS	Thermal shutdown Alsp Sense is 1 if above threshold	L2H
AHSSHORTI	AHSSHORTM	AHSSHORTS	Short circuit on Ahs outputs Sense is 1 if detected	L2H
1HZI	1HZM	-	1 Hz timetick	L2H
TODAI	TODAM	-	Time of day alarm	L2H
ONOFD1I	ONOFD1M	ONOFD1S	ON1B event Sense is 1 if pin is high	Dual
ONOFD2I	ONOFD2M	ONOFD2S	ON2B event Sense is 1 if pin is high	Dual
ONOFD3I	ONOFD3M	ONOFD3S	ON3B event Sense is 1 if pin is high	Dual
SYSRSTI	SYSRSTM	-	System reset	L2H
PWRRDYI	PWRRDYM	PWRRDYS	Power ready Sense is 1 if detected	L2H
THWARNHI	THWARNHM	THWARNHS	Thermal warning higher threshold Sense is 1 if above threshold	Dual
THWARNLI	THWARNLM	THWARNLS	Thermal warning lower threshold Sense is 1 if above threshold	Dual

Table 1-7. Interrupt, Mask and Sense Bits (continued)

Interrupt	Mask	Sense	Used for / Sense Bit Polarity	Trigger
PCI	PCM	-	Power cut event	L2H
WARMI	WARMM	-	Warm start event	L2H
MEMHLDI	MEMHLDM	-	Memory hold event	L2H
CLKI	CLKM	CLKS	Clock source change Sense is 1 if source is XTAL	Dual
SEMAFI	SEMAFM	-	Semaphore	Dual
RTCRSTI	RTCRSTM	-	RTC reset occurred	L2H

Table 1-8. Register 0, Interrupt Status 0

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
ADCDONEI	0	R/W	RESETB	0	ADC has finished requested conversions
ADCBISDONEI	1	R/W	RESETB	0	ADCBIS has finished requested conversions
TSI	2	R/W	RESETB	0	Touchscreen wake up
WHIGHI	3	R/W	RESETB	0	ADC reading above high limit
WLOWI	4	R/W	RESETB	0	ADC reading below low limit
Reserved	5	R/W	RESETB	0	For future use
CHGDETI	6	R/W	RESETB	0	Charger attach/removal
CHGOVI	7	R/W	RESETB	0	Charger over voltage detection
CHGREVI	8	R/W	RESETB	0	Charger path reverse current
CHGSHORTI	9	R/W	RESETB	0	Charger path short circuit
CCCVI	10	R/W	RESETB	0	Charger path V or I regulation
CHGCURRI	11	R/W	RESETB	0	Charge current below threshold warning
BPONI	12	R/W	RTCPORB	0	BP turn on threshold
LOBATLI	13	R/W	RESETB	0	Low battery low threshold warning
LOBATHI	14	R/W	RESETB	0	Low battery high threshold warning
UDPI	15	R/W	RESETB	0	UDP detect
USBI	16	R/W	RESETB	0	USB VBUS detect
Unused	17	R		0	Not available
Unused	18	R		0	Not available
IDI	19	R/W	RESETB	0	USB ID detect
Unused	20	R		0	Not available
SE1I	21	R/W	RESETB	0	Single ended 1 detect

Table 1-8. Register 0, Interrupt Status 0 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
CKDETI	22	R/W	RESETB	0	Carkit detect
UDMI	23	R/W	RESETB	0	UDM detect

Table 1-9. Register 1, Interrupt Mask 0

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
ADCDONEM	0	R/W	RESETB	1	ADCDONEI mask bit
ADCBISDONEM	1	R/W	RESETB	1	ADCBISDONEI mask bit
TSM	2	R/W	RESETB	1	TSI mask bit
WHIGHM	3	R/W	RESETB	1	WHIGHI mask bit
WLOWM	4	R/W	RESETB	1	WLOWI mask bit
Reserved	5	R/W	RESETB	1	For future use
CHGDETM	6	R/W	RESETB	1	CHGDETI mask bit
CHGOVM	7	R/W	RESETB	1	CHGOVI mask bit
CHGREVM	8	R/W	RESETB	1	CHGREVI mask bit
CHGSHORTM	9	R/W	RESETB	1	CHGSHORTI mask bit
CCCVM	10	R/W	RESETB	1	CCCVI mask bit
CHGCURRM	11	R/W	RESETB	1	CHGCURRI mask bit
BPONM	12	R/W	RTCPORB	1	BPONI mask bit
LOBATLM	13	R/W	RESETB	1	LOBATLI mask bit
LOBATHM	14	R/W	RESETB	1	LOBATHI mask bit
UDPM	15	R/W	RESETB	1	UDPI mask bit
USBM	16	R/W	RESETB	1	USBI mask bit
Unused	17	R		1	Not available
Unused	18	R		1	Not available
IDM	19	R/W	RESETB	1	IDI mask bit
Unused	20	R		1	Unused
SE1M	21	R/W	RESETB	1	SE1I mask bit
CKDETM	22	R/W	RESETB	1	CKDETI mask bit
UDMM	23	R/W	RESETB	1	UDMI mask bit

Table 1-10. Register 2, Interrupt Sense 0

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
Unused	0	R		0	Not available
Unused	1	R		0	Not available
Unused	2	R		0	Not available
Unused	3	R		0	Not available
Unused	4	R		0	Not available
Reserved	5	R	RESETB	0	For future use
CHGDETS	6	R	RESETB	0	CHGDETI sense bit Sense is 1 if above threshold
CHGOVS	7	R	RESETB	0	CHGOVI sense bit Sense is 1 if above threshold
CHGREVS	8	R	RESETB	0	CHGREVI sense bit Sense is 1 if current flows into phone
CHGSHORTS	9	R	RESETB	0	CHGSHORTI sense bit Sense is 1 if above threshold
CCCVS	10	R	RESETB	0	CCCVI sense bit Sense is 1 if voltage regulation
CHGCURRS	11	R	RESETB	0	CHGCURRI sense bit Sense is 1 if above threshold
BPONS	12	R	RESETB	0	BPONI sense bit Sense is 1 if above threshold
LOBATLS	13	R	RESETB	0	LOBATLI sense bit Sense is 1 if end of life detected Sense is 1 if below low battery threshold
LOBATHS	14	R	RESETB	0	LOBATHI sense bit Sense is 1 if above threshold
UDPS	15	R	RESETB	0	UDPI sense bit Sense is 1 if UDP pin is high
USB4V4S	16	R	RESETB	0	USB4V4 sense bit Sense is 1 if above threshold
USB2V0S	17	R	RESETB	0	USB2V0 sense bit Sense is 1 if above threshold
USB0V8S	18	R	RESETB	0	USB0V8 sense bit Sense is 1 if above threshold

Table 1-10. Register 2, Interrupt Sense 0 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
IDFLOATS	19	R	RESETB	0	ID float sense bit/ID ground sense bit 00 = no usb accessory is attached 01 = A type plug is attached indicating a USBOTG default slave. 10 = B type plug is attached indicating a USB Host, a USB OTG default master, or no device. 11 = factory mode
IDGNDS	20	R	RESETB	0	
SE1S	21	R	RESETB	0	SE1I sense bit Sense is 1 if detected
CKDETS	22	R	RESETB	0	CKDETI sense bit Sense is 1 if detected
UDMS	23	R	RESETB	0	UDMI sense bit Sense is 1 if UDP pin is high

Table 1-11. Register 3, Interrupt Status 1

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
1HZI	0	R/W	RTCPORB	0	1 Hz timetick
TODAI	1	R/W	RTCPORB	0	Time of day alarm
Reserved	2	R/W	RESETB	0	For future use
ONOFD1I	3	R/W	RESETB	0	ON1B event
ONOFD2I	4	R/W	RESETB	0	ON2B event
ONOFD3I	5	R/W	RESETB	0	ON3B event
SYSRSTI	6	R/W	RTCPORB	0	System reset
RTCRSTI	7	R/W	RTCPORB	0	RTC reset event Inform the processor that the contents of the RTC are no longer valid
PCI	8	R/W	RTCPORB	0	Power cut event
WARMI	9	R/W	RTCPORB	0	Warm start event
MEMHLDI	10	R/W	RTCPORB	0	Memory hold event
PWRRDYI	11	R/W	RESETB	0	Power Gate and DVS Power ready
THWARNLI	12	R/W	RESETB	0	Thermal warning low threshold
THWARNHI	13	R/W	RESETB	0	Thermal warning high threshold
CLKI	14	R/W	RESETB	0	Clock source change
SEMAFI	15	R/W	RESETB	0	Semaphore
Reserved	16	R/W	RESETB	0	For future use

Table 1-11. Register 3, Interrupt Status 1 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
MC2BI	17	R/W	RESETB	0	Microphone bias 2 detect
HSDETI	18	R/W	RESETB	0	Headset attach
HSLI	19	R/W	RESETB	0	Stereo headset detect
ALSPTHI	20	R/W	RESETB	0	Thermal shutdown Alsp
AHSSHORTI	21	R/W	RESETB	0	Short circuit on Ahs outputs
Reserved	22	R/W	RESETB	0	For future use
Reserved	23	R/W	RESETB	0	For future use

Table 1-12. Register 4, Interrupt Mask 1

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
1HZM	0	R/W	RTCPORB	1	1HZI mask bit
TODAM	1	R/W	RTCPORB	1	TODAI mask bit
Reserved	2	R/W	RESETB	1	For future use
ONOFD1M	3	R/W	RESETB	1	ONOFD1I mask bit
ONOFD2M	4	R/W	RESETB	1	ONOFD2I mask bit
ONOFD3M	5	R/W	RESETB	1	ONOFD3I mask bit
SYSRSTM	6	R/W	RTCPORB	1	SYSRSTI mask bit
RTCRSTM	7	R/W	RTCPORB	1	RTCRSTI mask bit
PCM	8	R/W	RTCPORB	1	PCI mask bit
WARMM	9	R/W	RTCPORB	1	WARMI mask bit
MEMHLDM	10	R/W	RTCPORB	1	MEMHLDI mask bit
PWRRDYM	11	R/W	RESETB	1	PWRRDYI mask bit
THWARNLM	12	R/W	RESETB	1	THWARNLI mask bit
THWARNHM	13	R/W	RESETB	1	THWARNHI mask bit
CLKM	14	R/W	RESETB	1	CLKI mask bit
SEMAFM	15	R/W	RESETB	1	SEMAFI mask bit
Reserved	16	R/W	RESETB	1	For future use
MC2BM	17	R/W	RESETB	1	MC2BI mask bit
HSDETM	18	R/W	RESETB	1	HSDETI mask bit
HSLM	19	R/W	RESETB	1	HSLI mask bit
ALSPTHM	20	R/W	RESETB	1	ALSPTHI mask bit
AHSSHORTM	21	R/W	RESETB	1	AHSSHORTI mask bit

Table 1-12. Register 4, Interrupt Mask 1 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
Reserved	22	R/W	RESETB	1	For future use
Reserved	23	R/W	RESETB	1	For future use

Table 1-13. Register 5, Interrupt Sense 1

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
Unused	0	R		0	Not available
Unused	1	R		0	Not available
Reserved	2	R	RESETB	0	For future use
ONOFD1S	3	R	RESETB	0	ONOFD1I sense bit Sense is 1 if pin is high
ONOFD2S	4	R	RESETB	0	ONOFD2I sense bit Sense is 1 if pin is high
ONOFD3S	5	R	RESETB	0	ONOFD3I sense bit Sense is 1 if pin is high
Unused	6	R		0	Not available
Unused	7	R		0	Not available
Unused	8	R		0	Not available
Unused	9	R		0	Not available
Unused	10	R		0	Not available
PWRRDYS	11	R	RESETB	0	PWRRDYI sense bit Sense is 1 if detected
THWARNLS	12	R	RESETB	0	THWARNLI sense bit Sense is 1 if above threshold
THWARNHS	13	R	RESETB	0	THWARNHI sense bit Sense is 1 if above threshold
CLKS	14	R	RESETB	0	CLKI sense bit 0 =: Internal RC oscillator 1 = XTAL oscillator
Unused	15	R		0	Not available
Reserved	16	R	RESETB	0	For future use
MC2BS	17	R	RESETB	0	MC2BI sense bit Sense is 1 if detected
HSDETS	18	R	RESETB	0	HSDETI sense bit Sense is 1 if headset connected
HSLS	19	R	RESETB	0	HSLI sense bit Sense is 1 if left headset connected

Table 1-13. Register 5, Interrupt Sense 1 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
ALSPTHS	20	R	RESETB	0	ALSPTHI mask bit Note: amplifiers will be automatically turned off
AHSSHORTS	21	R	RESETB	0	AHSSHORTI mask bit Sense is 1 if short detected Note: amplifiers will be automatically turned off
Reserved	22	R	RESETB	0	For future use
Reserved	23	R	RESETB	0	For future use

Additional sense bits are available in the power up mode sense register. Via these bits the state of the power up mode selection pins for the regulators, charger and USB can be read out. Table 1-14 summarizes these bits.

Table 1-14. Register 6, Power Up Mode Sense

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
ICTESTS	0	R	NONE	*	ICTEST state 0 = ICTEST low 1 = ICTEST high
CLKSELS	1	R	NONE	*	CLKSEL state 0 = CLKSEL low 1 = CLKSEL high
PUMS1S0	2	R	NONE	*	PUMS1 state 00 = PUMS1 low 01 = PUMS1 open 10 = Not available 11 = PUMS1 high
PUMS1S1	3	R	NONE	*	
PUMS2S0	4	R	NONE	*	PUMS2 state 00 = PUMS2 low 01 = PUMS2 open 10 = Not available 11 = PUMS2 high
PUMS2S1	5	R	NONE	*	
PUMS3S0	6	R	NONE	*	PUMS3 state 00 = PUMS3 low 01 = PUMS3 open 10 = Not available 11 = PUMS3 high
PUMS3S1	7	R	NONE	*	
CHRGMOD0S0	8	R	NONE	*	CHRGMOD0 state 00 = CHRGMOD0 low 01 = CHRGMOD0 open 10 = Not available 11 = CHRGMOD0 high
CHRGMOD0S1	9	R	NONE	*	

Table 1-14. Register 6, Power Up Mode Sense (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
CHRGMOD1S0	10	R	NONE	*	CHRGMOD1 state CHRGMOD1 state 00 = CHRGMOD1 low 01 = CHRGMOD1 open 10 = Not available 11 = CHRGMOD1 high
CHRGMOD1S1	11	R	NONE	*	
UMODS0	12	R	NONE	*	UMOD state UMOD0 UMOD1 states 00 = UMOD0 low, UMOD1 = low 01 = UMOD0 open, UMOD1= low 10 = UMOD0 don't care, UMOD1 = high 11 = UMOD0 high, UMOD1 = low
UMODS1	13	R	NONE	*	
USBENS	14	R	NONE	*	USBEN state0 = USBEN low 0 = USBEN low 1 = USBEN high
SW1ABS	15	R	NONE	*	Switcher1 mode 0 = SW1A and SW1B independent operation 1 = SW1A and SW1B joined operation
SW2ABS	16	R	NONE	*	Switcher2 mode 0 = SW2A and SW2B independent operation 1 = SW2A and SW2B joined operation
Reserved	17	R	NONE	0	For future use
Reserved	18	R	NONE	0	For future use
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

1.4 IC Identification

The MC13783 parts can be identified by version and revision number. The revision of the MC13783 is binary coded and tracked with the revision identification bits REV[4:0]. The bits REV[4:3] track the full mask set revision, where bits REV[2:0] track the metal revisions. These bits are hardwired.

Table 1-15. IC Revision Bit Assignment

Full Mask		Metal Mask	
Version	Bit Assignment REV[4:3]	Version	Bit Assignment REV[2:0]
1	01	0	000
2	10	1	001

Table 1-15. IC Revision Bit Assignment

Full Mask		Metal Mask	
Version	**Bit Assignment REV[4:3]**	**Version**	**Bit Assignment REV[2:0]**
3	11	2	010
		…	…
Note: Example: Version 3.3 is identified by REV[4:0] = 11 011. Exception to this table: Version 3.2A is identified by REV[4:0] = 00 010.			

Table 1-16. Register 7, Identification

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
REV0	0	R	NONE	Version dependent	MC13783 revision
REV1	1	R	NONE	Version dependent	
REV2	2	R	NONE	Version dependent	
REV3	3	R	NONE	Version dependent	
REV4	4	R	NONE	Version dependent	
Reserved	5	R	NONE	0	For future use
ICID0	6	R	NONE	0	MC13783 derivative
ICID1	7	R	NONE	1	
ICID2	8	R	NONE	0	
FIN0	9	R	NONE	Version dependent	MC13783 fin version
FIN1	10	R	NONE	Version dependent	
FAB0	11	R	NONE	Fab dependent	MC13783 fab identifier
FAB1	12	R	NONE	Fab dependent	
Unused	13	R		0	Not available
Unused	14	R		0	Not available
Unused	15	R		0	Not available
Unused	16	R		0	Not available
Unused	17	R		0	Not available
Unused	18	R		0	Not available
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Table 1-17. Register 46, ADC 3

Name	Bit #	R/W	Reset	Default	Description
ICID0	6	R/W	NONE	0	MC13783 derivative
ICID1	7	R/W	NONE	1	
ICID2	8	R/W	NONE	0	

1.5 Test Mode Registers - Trim Registers and Spare Register

During evaluation and testing, several modules are configured in specific modes via the test mode bits. The test mode bits are available in registers 60, 61, 62 and 63.

During IC final test, several parameters are trimmed such as the main bandgap for instance. The trimming is performed via the SPI interface. The trim bits are residing in the trim registers 58 and 59.

Table 1-18. Register 58, Trim 0

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
TRIM[23:0]	23:0	R/W	NONE	TRIM	Reserved for trimming

Table 1-19. Register 59, Trim 1

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
TRIM[47:24]	23:0	R/W	NONE	TRIM	Reserved for trimming

Table 1-20. Register 60, Test 0

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
TEST[23:0]	23:0	R/W	RESETB	0	Reserved for test purposes

Table 1-21. Register 61, Test 1

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
TEST[47:24]	23:0	R/W	RESETB	0	Reserved for test purposes

Table 1-22. Register 62, Test 2

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
TEST[71:48]	23:0	R/W	RESETB	0	Reserved for test purposes

Table 1-23. Register 63, Test 3

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
TEST[95:72]	23:0	R/W	RESETB	0	Reserved for test purposes

Table 1-24. Register 57, Spare

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
Unused	0	R		0	Not available
Unused	1	R		0	Not available
Unused	2	R		0	Not available
Unused	3	R		0	Not available
Unused	4	R		0	Not available
Unused	5	R		0	Not available
Unused	6	R		0	Not available
Unused	7	R		0	Not available
Unused	8	R		0	Not available
Unused	9	R		0	Not available
Unused	10	R		0	Not available
Unused	11	R		0	Not available
Unused	12	R		0	Not available
Unused	13	R		0	Not available
Unused	14	R		0	Not available
Unused	15	R		0	Not available
Unused	16	R		0	Not available
Unused	17	R		0	Not available
Unused	18	R		0	Not available
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Chapter 2
Clock Generation and Real Time Clock

2.1 Time and Day Counters

The real time clock runs from the 32 kHz clock, either the RC oscillator or the crystal oscillator if a crystal is present. This clock is divided down to a 1Hz time tick which drives a 17 bit time of day (TOD) counter. The TOD counter counts the seconds during a 24 hour period from 0 to 86,399 and will then roll over to 0. When the roll over occurs, it increments the 15 bit DAY counter. The DAY counter can count up to 32767 days. The 1 Hz timetick can be used to generate an 1HZI interrupt. The 1HZI can be masked with corresponding 1HZM mask bit.

If the TOD and DAY registers are read at a point in time in which DAY is incremented, then care must be taken that, if DAY is read first, DAY has not changed before reading TOD. The following sequence of events can occur.

1. Software reads a value of DAY
2. The DAY counter increments (by definition, the TOD register also increments)
3. Software then reads the value of TOD

In this case, the value that is read from the TOD register is not valid for the value of DAY just read. In order to guarantee stable TOD and DAY data, all SPI reads and writes to TOD and DAY data should happen immediately after the 1HZI interrupt occurs. Alternatively, TOD or DAY readbacks could be double-read and then compared to verify that they haven't changed. This requirement results from the fact that the 32.768 kHz clock is completely independent of the SPI clock and the two cannot be synchronized, hence the possibility of glitches is introduced if these values are accessed incorrectly.

Table 2-1. Register 20, RTC Time

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
TOD0	0	R/W	RTCPORB	0	Time of day counter
TOD1	1	R/W	RTCPORB	0	
TOD2	2	R/W	RTCPORB	0	
TOD3	3	R/W	RTCPORB	0	
TOD4	4	R/W	RTCPORB	0	
TOD5	5	R/W	RTCPORB	0	
TOD6	6	R/W	RTCPORB	0	
TOD7	7	R/W	RTCPORB	0	
TOD8	8	R/W	RTCPORB	0	
TOD9	9	R/W	RTCPORB	0	
TOD10	10	R/W	RTCPORB	0	
TOD11	11	R/W	RTCPORB	0	
TOD12	12	R/W	RTCPORB	0	
TOD13	13	R/W	RTCPORB	0	
TOD14	14	R/W	RTCPORB	0	
TOD15	15	R/W	RTCPORB	0	
TOD16	16	R/W	RTCPORB	0	
Unused	17	R		0	Not available
Unused	18	R		0	Not available
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Table 2-2. Register 22, RTC Day

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
DAY0	0	R/W	RTCPORB	0	Day counter
DAY1	1	R/W	RTCPORB	0	
DAY2	2	R/W	RTCPORB	0	
DAY3	3	R/W	RTCPORB	0	
DAY4	4	R/W	RTCPORB	0	
DAY5	5	R/W	RTCPORB	0	
DAY6	6	R/W	RTCPORB	0	
DAY7	7	R/W	RTCPORB	0	
DAY8	8	R/W	RTCPORB	0	
DAY9	9	R/W	RTCPORB	0	
DAY10	10	R/W	RTCPORB	0	
DAY11	11	R/W	RTCPORB	0	
DAY12	12	R/W	RTCPORB	0	
DAY13	13	R/W	RTCPORB	0	
DAY14	14	R/W	RTCPORB	0	
Unused	15	R		0	Not available
Unused	16	R		0	Not available
Unused	17	R		0	Not available
Unused	18	R		0	Not available
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

2.2 Time Of Day Alarm

When the TOD counter is equal to the value in TODA, and the DAY counter is equal to the value in DAYA, the TODAI interrupt will be generated.

Table 2-3. Register 21, RTC Alarm

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
TODA0	0	R/W	RTCPORB	1	Time of day alarm
TODA1	1	R/W	RTCPORB	1	
TODA2	2	R/W	RTCPORB	1	
TODA3	3	R/W	RTCPORB	1	
TODA4	4	R/W	RTCPORB	1	
TODA5	5	R/W	RTCPORB	1	
TODA6	6	R/W	RTCPORB	1	
TODA7	7	R/W	RTCPORB	1	
TODA8	8	R/W	RTCPORB	1	
TODA9	9	R/W	RTCPORB	1	
TODA10	10	R/W	RTCPORB	1	
TODA11	11	R/W	RTCPORB	1	
TODA12	12	R/W	RTCPORB	1	
TODA13	13	R/W	RTCPORB	1	
TODA14	14	R/W	RTCPORB	1	
TODA15	15	R/W	RTCPORB	1	
TODA16	16	R/W	RTCPORB	1	
Unused	17	R		0	Not available
Unused	18	R		0	Not available
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Table 2-4. Register 23, RTC Day Alarm

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
DAYA0	0	R/W	RTCPORB	1	Day alarm
DAYA1	1	R/W	RTCPORB	1	
DAYA2	2	R/W	RTCPORB	1	
DAYA3	3	R/W	RTCPORB	1	
DAYA4	4	R/W	RTCPORB	1	
DAYA5	5	R/W	RTCPORB	1	
DAYA6	6	R/W	RTCPORB	1	
DAYA7	7	R/W	RTCPORB	1	
DAYA8	8	R/W	RTCPORB	1	
DAYA9	9	R/W	RTCPORB	1	
DAYA10	10	R/W	RTCPORB	1	
DAYA11	11	R/W	RTCPORB	1	
DAYA12	12	R/W	RTCPORB	1	
DAYA13	13	R/W	RTCPORB	1	
DAYA14	14	R/W	RTCPORB	1	
Unused	15	R		0	Not available
Unused	16	R		0	Not available
Unused	17	R		0	Not available
Unused	18	R		0	Not available
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Chapter 3
Power Control System

Table 3-1. Register 13, Power Control 0

Name	Bit #	R/W	Reset [1]	Default	Description Vector Bits are MSB First
PCEN	0	R/W	RTCPORB	0	Power cut enable 1 = Power Cut enabled 0 = Power Cut disabled
PCCOUNTEN	1	R/W	RTCPORB	0	Power cut counter enable 0 = infinits power cut supported 1 = PCCOUNT power cuts supported
WARMEN	2	R/W	RTCPORB	0	Warm start enable 0 = Transition to memory hold 1 = Transition to user off mode
USEROFFSPI	3	R/W	RESETB	0	SPI command for entering user off modes
USEROFFPC	4	R/W	RTCPORB	0	Automatic transition to user off during power cut 0 = Transition to user off during power cut mode if USEROFF = 1 Transition to memory hold power cut mode if USEROFF = 0 1 = Transition to user off during power cut mode independently of the USEROFF signal
USEROFFCLK	5	R/W	RTCPORB	0	0 = disable the CLK32KMCU active during user off power cut modes 1 = Keeps the CLK32KMCU active during user off power cut modes
CLK32KMCUEN	6	R/W	RTCPORB	1	0 = Disable the CLK32KMCU 1 = Enables the CLK32KMCU
VBKUP2AUTOMH	7	R/W	OFFB	0	0 = Disable VBKUP2 regulator in the memory hold modes 1 = Automatically enables VBKUP2 regulator in the memory hold modes
VBKUP1EN	8	R/W	RESETB	0	0 = Disable VBKUP1 regulator in non power cut mode 1 = Enable VBKUP1 regulator in non power cut mode
VBKUP1AUTO	9	R/W	OFFB	0	0 = Disable VBKUP1 regulator in the memory hold and user off modes 1 = Automatically enables VBKUP1 regulator in the memory hold and user off modes
VBKUP10	10	R/W	NONE	*	Sets VBKUP1 voltage 00 = 1.000 V 01 = 1.200 V 10 = 1.575 V 11 = 1.800 V
VBKUP11	11	R/W	NONE	*	

Table 3-1. Register 13, Power Control 0 (continued)

Name	Bit #	R/W	Reset [1]	Default	Description Vector Bits are MSB First
VBKUP2EN	12	R/W	RESETB	0	0 = Disable VBKUP2 regulator in non power cut mode 1 = Enable VBKUP2 regulator in non power cut mode
VBKUP2AUTOUO	13	R/W	OFFB	0	0 = Disable VBKUP2 regulator in the user off modes 1 = Automatically enables VBKUP2 regulator in the user off modes
VBKUP20	14	R/W	NONE	*	Sets VBKUP2 voltage 00 = 1.000 V 01 = 1.200 V 10 = 1.500 V 11 = 1.800 V
VBKUP21	15	R/W	NONE	*	
BPDET0	16	R/W	RTCPORB	0	BP detection threshold setting See Table 3-2 for details
BPDET1	17	R/W	RTCPORB	0	
EOLSEL	18	R/W	RTCPORB	0	Selects EOL function instead of LOBAT 0 = LOBATL monitors on the state of VRF1 VRF2 and VRFREF regulators 1 = LOBATL monitors BP level
BATTDETEN	19	R/W	RTCPORB	0	Enables battery detect function 0 = Disable battery detect function 1 = Enable Battery detect function
VCOIN0	20	R/W	RTCPORB	0	Coincell charger voltage setting 000 = 2.50 V 001 = 2.70 V 010 = 2.80 V 011 = 2.90 V 100 = 3.00 V 101 = 3.10 V 110 = 3.20 V 111 = 3.30 V
VCOIN1	21	R/W	RTCPORB	0	
VCOIN2	22	R/W	RTCPORB	0	
COINCHEN	23	R/W	RTCPORB	0	Coincell charger enable 0 = Disable coincell charger 1 = Enable coincell charger

[1] OFFB represents a reset when in Off or Invalid Power modes.

Table 3-2. BP Detection Threshold Setting

BPDET1	BPDET0	UVDET	LOBATL	LOBATH	BPON
0	0	2.6	UVDET + 0.2	UVDET + 0.4	3.2
0	1	2.6	UVDET + 0.3	UVDET + 0.5	3.2
1	0	2.6	UVDET + 0.4	UVDET + 0.7	3.2
1	1	2.6	UVDET + 0.5	UVDET + 0.8	3.2

Table 3-3. Register 14, Power Control 1

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
PCT0	0	R/W	RTCPORB	0	Power cut timer Programmable timer from 0 to 8 seconds (~32ms steps)
PCT1	1	R/W	RTCPORB	0	
PCT2	2	R/W	RTCPORB	0	
PCT3	3	R/W	RTCPORB	0	
PCT4	4	R/W	RTCPORB	0	
PCT5	5	R/W	RTCPORB	0	
PCT6	6	R/W	RTCPORB	0	
PCT7	7	R/W	RTCPORB	0	
PCCOUNT0	8	R/W	RTCPORB	0	Power cut counter Power cut counter from 0 to 15
PCCOUNT1	9	R/W	RTCPORB	0	
PCCOUNT2	10	R/W	RTCPORB	0	
PCCOUNT3	11	R/W	RTCPORB	0	
PCMAXCNT0	12	R/W	RTCPORB	0	Maximum allowed number of power cuts Programmable counter from 0 to 7
PCMAXCNT1	13	R/W	RTCPORB	0	
PCMAXCNT2	14	R/W	RTCPORB	0	
PCMAXCNT3	15	R/W	RTCPORB	0	
MEMTMR0	16	R/W	RTCPORB	0	Extended power cut timer Programmable timer from 0 to 8 seconds (~32ms steps)
MEMTMR1	17	R/W	RTCPORB	0	
MEMTMR2	18	R/W	RTCPORB	0	
MEMTMR3	19	R/W	RTCPORB	0	
MEMALLON	20	R/W	RTCPORB	0	Extended power cut timer set to infinite 0 = extended power cute timer defined by MEMTMR[3:0] 1 = infinite extended power cut time (only if MEMTMR[3:0]<>0
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Table 3-4. Register 15, Power Control 2

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
RESTARTEN	0	R/W	RTCPORB	0	Enables automatic restart after a system reset 0 = Disable Automatic restart after a system reset 1 = Enable Automatic restart one second after a system reset
ON1BRSTEN	1	R/W	RTCPORB	0	Enables system reset on ON1B pin 0 = Disable system reset on ON1B button 1 = Enable system reset on ON1B button
ON2BRSTEN	2	R/W	RTCPORB	0	Enables system reset on ON2B pin 0 = Disable system reset on ON2B button 1 = Enable system reset on ON2B button
ON3BRSTEN	3	R/W	RTCPORB	0	Enables system reset on ON3B pin 0 = Disable system reset on ON3B button 1 = Enable system reset on ON3B button
ON1BDBNC0	4	R/W	RTCPORB	0	Sets debounce time on ON1B pin 00 = 0 ms 01 = 30 ms 10 = 150 ms 11 = 750 ms
ON1BDBNC1	5	R/W	RTCPORB	0	
ON2BDBNC0	6	R/W	RTCPORB	0	Sets debounce time on ON2B pin 00 = 0 ms 01 = 30 ms 10 = 150 ms 11 = 750 ms
ON2BDBNC1	7	R/W	RTCPORB	0	
ON3BDBNC0	8	R/W	RTCPORB	0	Sets debounce time on ON3B pin 00 = 0 ms 01 = 30 ms 10 = 150 ms 11 = 750 ms
ON3BDBNC1	9	R/W	RTCPORB	0	
STANDBYPRIINV	10	R/W	RTCPORB	0	If set then STANDBYPRI is interpreted as active low
STANDBYSECINV	11	R/W	RTCPORB	0	If set then STANDBYSEC is interpreted as active low
Unused	12	R		0	Not available
Unused	13	R		0	Not available
Unused	14	R		0	Not available
Unused	15	R		0	Not available
Unused	16	R		0	Not available
Unused	17	R		0	Not available
Unused	18	R		0	Not available
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available

Table 3-4. Register 15, Power Control 2 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Table 3-5. Register 17, Control Spare

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
Unused	0	R		0	Not available
Unused	1	R		0	Not available
Unused	2	R		0	Not available
Unused	3	R		0	Not available
Unused	4	R		0	Not available
Unused	5	R		0	Not available
Unused	6	R		0	Not available
Unused	7	R		0	Not available
Unused	8	R		0	Not available
Unused	9	R		0	Not available
Unused	10	R		0	Not available
Unused	11	R		0	Not available
Unused	12	R		0	Not available
Unused	13	R		0	Not available
Unused	14	R		0	Not available
Unused	15	R		0	Not available
Unused	16	R		0	Not available
Unused	17	R		0	Not available
Unused	18	R		0	Not available
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Table 3-6. Register 18, Memory A

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
MEMA0	0	R/W	RTCPORB	0	Backup memory A
MEMA1	1	R/W	RTCPORB	0	
MEMA2	2	R/W	RTCPORB	0	
MEMA3	3	R/W	RTCPORB	0	
MEMA4	4	R/W	RTCPORB	0	
MEMA5	5	R/W	RTCPORB	0	
MEMA6	6	R/W	RTCPORB	0	
MEMA7	7	R/W	RTCPORB	0	
MEMA8	8	R/W	RTCPORB	0	
MEMA9	9	R/W	RTCPORB	0	
MEMA10	10	R/W	RTCPORB	0	
MEMA11	11	R/W	RTCPORB	0	
MEMA12	12	R/W	RTCPORB	0	
MEMA13	13	R/W	RTCPORB	0	
MEMA14	14	R/W	RTCPORB	0	
MEMA15	15	R/W	RTCPORB	0	
MEMA16	16	R/W	RTCPORB	0	
MEMA17	17	R/W	RTCPORB	0	
MEMA18	18	R/W	RTCPORB	0	
MEMA19	19	R/W	RTCPORB	0	
MEMA20	20	R/W	RTCPORB	0	
MEMA21	21	R/W	RTCPORB	0	
MEMA22	22	R/W	RTCPORB	0	
MEMA23	23	R/W	RTCPORB	0	

Table 3-7. Register 19, Memory B

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
MEMB0	0	R/W	RTCPORB	0	Backup memory B
MEMB1	1	R/W	RTCPORB	0	
MEMB2	2	R/W	RTCPORB	0	
MEMB3	3	R/W	RTCPORB	0	
MEMB4	4	R/W	RTCPORB	0	
MEMB5	5	R/W	RTCPORB	0	
MEMB6	6	R/W	RTCPORB	0	
MEMB7	7	R/W	RTCPORB	0	
MEMB8	8	R/W	RTCPORB	0	
MEMB9	9	R/W	RTCPORB	0	
MEMB10	10	R/W	RTCPORB	0	
MEMB11	11	R/W	RTCPORB	0	
MEMB12	12	R/W	RTCPORB	0	
MEMB13	13	R/W	RTCPORB	0	
MEMB14	14	R/W	RTCPORB	0	
MEMB15	15	R/W	RTCPORB	0	
MEMB16	16	R/W	RTCPORB	0	
MEMB17	17	R/W	RTCPORB	0	
MEMB18	18	R/W	RTCPORB	0	
MEMB19	19	R/W	RTCPORB	0	
MEMB20	20	R/W	RTCPORB	0	
MEMB21	21	R/W	RTCPORB	0	
MEMB22	22	R/W	RTCPORB	0	
MEMB23	23	R/W	RTCPORB	0	

Chapter 4
Supplies

4.1 Switcher

4.1.1 General Description

The switchers can be put in one of their power saving modes by SPI programming and by controlling the STANDBY pins. Each switcher has associated power saving mode bits. The SWxMODE bit setting is valid for STANDBY being low, while the SWxSTBYMODE bits are validated for STANDBY is high. Table 4-1 summarizes the buck switcher power saving modes under the assumption that a single SPI controls a switcher.

Table 4-1. Switcher Mode Control

SWxMODE for STANDBY = Low	SWxSTBYMODE for STANDBY = High	Switcher SWx	Control Loop	Pulse Skipping	Current Range
00	00	Off	-	-	-
01	01	On	PWM	No	500 mA
10	10	On	PWM	Yes	500 mA
11	11	On	PFM	-	50 mA

The buck switchers have dynamic voltage scaling capability (DVS). With DVS, the output voltage setting can be controlled via the DVS pins DVSSWxy (xy being 1A, 1B, 2A and 2B) and the STANDBY pins. Each of the switchers have 6 bits of control SWxy for their output voltage setting. There is a separate setting for the different operating modes and there is a separate setting for each of the SPI interfaces.

Table 4-2. Switcher Output Voltage Control, Single DVS

State of Pin STANDBY	State of Pin DVSSWxy	SWxABDVS=0 SWxy Output Voltage Determined By
0	0	SWxy[5:0]
0	1	SWxyDVS[5:0]
1	0	SWxySTBY[5:0]
1	1	SWxySTBY[5:0]

The DVS pins of the switchers can be combined by setting the SW1ABDVS and the SW2ABDVS bit to a "1" for combining respectively the DVSSW1A with the DVSSW1B pin and the DVSSW2A pin with DVSSW2B pin. The combined DVS pins are associated to the switcher A section. Combining the DVS

pins does not necessarily make the outputs and control of the A and B sections are combined, that is determined at startup by single/ ^parallel mode. Two DVS pins can be used for switcher A while still using the A and B switcher independently. In this case, switcher B has no longer DVS control. The SWxABDVS bits are only accessible via the primary SPI. Table 4-3 indicates the output setting of the switcher in case of combined DVS pin use.

Table 4-3. Switcher Output Voltage Control, Dual DVS

State of Pin STANDBY	State of Pin DVSSWxA	State of Pin DVSSWxB	SWxABDVS=1 SWxA Output Voltage Determined By
0	0	0	SWxA[5:0]
0	1	0	SWxADVS[5:0]
0	0	1	SWxBDVS[5:0]
0	1	1	SWxBSTBY[5:0]
1	X	X	SWxASTBY[5:0]

4.1.2 SPI Registers

Table 4-4. Output Voltage Select Range for SW1A

CODE	VOLTAGE SW1A	CODE (*)	VOLTAGE SW1A
000000	0.900	100000	1.700
000001	0.925	100001	1.700
000010	0.950	100010	1.700
000011	0.975	100011	1.700
000100	1.000	100100	1.800
000101	1.025	100101	1.800
000110	1.050	100110	1.800
000111	1.075	100111	1.800
001000	1.100	101000	1.850
001001	1.125	101001	1.850
001010	1.150	101010	1.850
001011	1.175	101011	1.850
001100	1.200	101100	2.000
001101	1.225	101101	2.000
001110	1.250	101110	2.000
001111	1.275	101111	2.000
010000	1.300	110000	2.100

Table 4-4. Output Voltage Select Range for SW1A (continued)

CODE	VOLTAGE SW1A	CODE (*)	VOLTAGE SW1A
010001	1.325	110001	2.100
010010	1.350	110010	2.100
010011	1.375	110011	2.100
010100	1.400	110100	2.200
010101	1.425	110101	2.200
010110	1.450	110110	2.200
010111	1.475	110111	2.200
011000	1.500	111000	2.200
011001	1.525	111001	2.200
011010	1.550	111010	2.200
011011	1.575	111011	2.200
011100	1.600	111100	2.200
011101	1.625	111101	2.200
011110	1.650	111110	2.200
011111	1.675	111111	2.200
Note: (*) Codes 110101 to 111111 are used as test codes for ICTEST is high.			

Table 4-5. Register 24, Switchers 0

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
SW1A0	0	R/W	NONE	*	SW1A setting See Table 4-4
SW1A1	1	R/W	NONE	*	
SW1A2	2	R/W	NONE	*	
SW1A3	3	R/W	NONE	*	
SW1A4	4	R/W	NONE	*	
SW1A5	5	R/W	NONE	*	
SW1ADVS0	6	R/W	NONE	*	SW1A setting in DVS See Table 4-4
SW1ADVS1	7	R/W	NONE	*	
SW1ADVS2	8	R/W	NONE	*	
SW1ADVS3	9	R/W	NONE	*	
SW1ADVS4	10	R/W	NONE	*	
SW1ADVS5	11	R/W	NONE	*	

Table 4-5. Register 24, Switchers 0 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
SW1ASTBY0	12	R/W	NONE	*	SW1A setting in standby See Table 4-4
SW1ASTBY1	13	R/W	NONE	*	
SW1ASTBY2	14	R/W	NONE	*	
SW1ASTBY3	15	R/W	NONE	*	
SW1ASTBY4	16	R/W	NONE	*	
SW1ASTBY5	17	R/W	NONE	*	
Reserved	18	R/W	RESETB	0	For future use
Reserved	19	R/W	RESETB	0	For future use
Reserved	20	R/W	RESETB	0	For future use
Reserved	21	R/W	RESETB	0	For future use
Reserved	22	R/W	RESETB	0	For future use
Reserved	23	R/W	RESETB	0	For future use

Table 4-6. Output Voltage Select Range for SW1B

CODE	VOLTAGE SW1B	CODE (*)	VOLTAGE SW1B
000000	0.900	100000	1.700
000001	0.925	100001	1.700
000010	0.950	100010	1.700
000011	0.975	100011	1.700
000100	1.000	100100	1.800
000101	1.025	100101	1.800
000110	1.050	100110	1.800
000111	1.075	100111	1.800
001000	1.100	101000	1.850
001001	1.125	101001	1.850
001010	1.150	101010	1.850
001011	1.175	101011	1.850
001100	1.200	101100	2.000
001101	1.225	101101	2.000
001110	1.250	101110	2.000
001111	1.275	101111	2.000
010000	1.300	110000	2.100

Table 4-6. Output Voltage Select Range for SW1B (continued)

CODE	VOLTAGE SW1B	CODE (*)	VOLTAGE SW1B
010001	1.325	110001	2.100
010010	1.350	110010	2.100
010011	1.375	110011	2.100
010100	1.400	110100	2.200
010101	1.425	110101	2.200
010110	1.450	110110	2.200
010111	1.475	110111	2.200
011000	1.500	111000	2.200
011001	1.525	111001	2.200
011010	1.550	111010	2.200
011011	1.575	111011	2.200
011100	1.600	111100	2.200
011101	1.625	111101	2.200
011110	1.650	111110	2.200
011111	1.675	111111	2.200
Note: (*) Codes 110101 to 111111 are used as test codes for ICTEST is high.			

Table 4-7. Register 25, Switchers 1

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
SW1B0	0	R/W	NONE	*	SW1B setting See Table 4-6
SW1B1	1	R/W	NONE	*	
SW1B2	2	R/W	NONE	*	
SW1B3	3	R/W	NONE	*	
SW1B4	4	R/W	NONE	*	
SW1B5	5	R/W	NONE	*	
SW1BDVS0	6	R/W	NONE	*	SW1B setting in DVS See Table 4-6
SW1BDVS1	7	R/W	NONE	*	
SW1BDVS2	8	R/W	NONE	*	
SW1BDVS3	9	R/W	NONE	*	
SW1BDVS4	10	R/W	NONE	*	
SW1BDVS5	11	R/W	NONE	*	

Table 4-7. Register 25, Switchers 1 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
SW1BSTBY0	12	R/W	NONE	*	SW1B setting in standby See Table 4-6
SW1BSTBY1	13	R/W	NONE	*	
SW1BSTBY2	14	R/W	NONE	*	
SW1BSTBY3	15	R/W	NONE	*	
SW1BSTBY4	16	R/W	NONE	*	
SW1BSTBY5	17	R/W	NONE	*	
Unused	18	R		0	Not available
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Table 4-8. Output Voltage Select Range SW2A

CODE	VOLTAGE SW2A	CODE (*)	VOLTAGE SW2A
000000	0.900	100000	1.700
000001	0.925	100001	1.700
000010	0.950	100010	1.700
000011	0.975	100011	1.700
000100	1.000	100100	1.800
000101	1.025	100101	1.800
000110	1.050	100110	1.800
000111	1.075	100111	1.800
001000	1.100	101000	1.900
001001	1.125	101001	1.900
001010	1.150	101010	1.900
001011	1.175	101011	1.900
001100	1.200	101100	2.000
001101	1.225	101101	2.000
001110	1.250	101110	2.000
001111	1.275	101111	2.000
010000	1.300	110000	2.100

Table 4-8. Output Voltage Select Range SW2A (continued)

CODE	VOLTAGE SW2A	CODE (*)	VOLTAGE SW2A
010001	1.325	110001	2.100
010010	1.350	110010	2.100
010011	1.375	110011	2.100
010100	1.400	110100	2.200
010101	1.425	110101	2.200
010110	1.450	110110	2.200
010111	1.475	110111	2.200
011000	1.500	111000	2.200
011001	1.525	111001	2.200
011010	1.550	111010	2.200
011011	1.575	111011	2.200
011100	1.600	111100	2.200
011101	1.625	111101	2.200
011110	1.650	111110	2.200
011111	1.675	111111	2.200
Note: (*) Codes 110101 to 111111 are used as test codes for ICTEST is high.			

Table 4-9. Register 26, Switchers 2

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
SW2A0	0	R/W	NONE	*	SW2A setting See Table 4-8
SW2A1	1	R/W	NONE	*	
SW2A2	2	R/W	NONE	*	
SW2A3	3	R/W	NONE	*	
SW2A4	4	R/W	NONE	*	
SW2A5	5	R/W	NONE	*	
SW2ADVS0	6	R/W	NONE	*	SW2A setting in DVS See Table 4-8
SW2ADVS1	7	R/W	NONE	*	
SW2ADVS2	8	R/W	NONE	*	
SW2ADVS3	9	R/W	NONE	*	
SW2ADVS4	10	R/W	NONE	*	
SW2ADVS5	11	R/W	NONE	*	

Table 4-9. Register 26, Switchers 2 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
SW2ASTBY0	12	R/W	NONE	*	SW2A setting in standby See Table 4-8
SW2ASTBY1	13	R/W	NONE	*	
SW2ASTBY2	14	R/W	NONE	*	
SW2ASTBY3	15	R/W	NONE	*	
SW2ASTBY4	16	R/W	NONE	*	
SW2ASTBY5	17	R/W	NONE	*	
Reserved	18	R/W	RESETB	0	For future use
Reserved	19	R/W	RESETB	0	For future use
Reserved	20	R/W	RESETB	0	For future use
Reserved	21	R/W	RESETB	0	For future use
Reserved	22	R/W	RESETB	0	For future use
Reserved	23	R/W	RESETB	0	For future use

Table 4-10. Output Voltage Select Range SW2B

CODE	VOLTAGE SW2B	CODE (*)	VOLTAGE SW2B
000000	0.900	100000	1.700
000001	0.925	100001	1.700
000010	0.950	100010	1.700
000011	0.975	100011	1.700
000100	1.000	100100	1.800
000101	1.025	100101	1.800
000110	1.050	100110	1.800
000111	1.075	100111	1.800
001000	1.100	101000	1.900
001001	1.125	101001	1.900
001010	1.150	101010	1.900
001011	1.175	101011	1.900
001100	1.200	101100	2.000
001101	1.225	101101	2.000
001110	1.250	101110	2.000
001111	1.275	101111	2.000
010000	1.300	110000	2.100

Table 4-10. Output Voltage Select Range SW2B (continued)

CODE	VOLTAGE SW2B	CODE (*)	VOLTAGE SW2B
010001	1.325	110001	2.100
010010	1.350	110010	2.100
010011	1.375	110011	2.100
010100	1.400	110100	2.200
010101	1.425	110101	2.200
010110	1.450	110110	2.200
010111	1.475	110111	2.200
011000	1.500	111000	2.200
011001	1.525	111001	2.200
011010	1.550	111010	2.200
011011	1.575	111011	2.200
011100	1.600	111100	2.200
011101	1.625	111101	2.200
011110	1.650	111110	2.200
011111	1.675	111111	2.200
Note: (*) Codes 110101 to 111111 are used as test codes for ICTEST is high.			

Table 4-11. Register 27, Switchers 3

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
SW2B0	0	R/W	NONE	*	SW2B setting See Table 4-10
SW2B1	1	R/W	NONE	*	
SW2B2	2	R/W	NONE	*	
SW2B3	3	R/W	NONE	*	
SW2B4	4	R/W	NONE	*	
SW2B5	5	R/W	NONE	*	
SW2BDVS0	6	R/W	NONE	*	SW2B setting in DVS See Table 4-10
SW2BDVS1	7	R/W	NONE	*	
SW2BDVS2	8	R/W	NONE	*	
SW2BDVS3	9	R/W	NONE	*	
SW2BDVS4	10	R/W	NONE	*	
SW2BDVS5	11	R/W	NONE	*	

Table 4-11. Register 27, Switchers 3 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
SW2BSTBY0	12	R/W	NONE	*	SW2B setting in standby See Table 4-10
SW2BSTBY1	13	R/W	NONE	*	
SW2BSTBY2	14	R/W	NONE	*	
SW2BSTBY3	15	R/W	NONE	*	
SW2BSTBY4	16	R/W	NONE	*	
SW2BSTBY5	17	R/W	NONE	*	
Unused	18	R		0	Not available
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Table 4-12. Register 28, Switchers 4

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
SW1AMODE0	0	R/W	NONE	*	SW1A operating mode 00 = OFF 01 = PWM mode No Pulse Skipping 10 = PWM mode Pulse Skipping Allowed 11 = Low Power PFM mode
SW1AMODE1	1	R/W	RESETB	0	
SW1ASTBYMODE0	2	R/W	NONE	*	SW1A operating mode in standby 00 = OFF 01 = PWM mode No Pulse Skipping 10 = PWM mode Pulse Skipping Allowed 11 = Low Power PFM mode
SW1ASTBYMODE1	3	R/W	RESETB	0	
Reserved	4	R/W	RESETB	0	For future use
Reserved	5	R/W	RESETB	0	For future use
SW1ADVSSPEED0	6	R/W	RESETB	0	SW1A DVS speed setting 00 = 25mV step each 4us. Power Ready signal not influenced 01 = 25 mV step each 4 us 10 = 25 mV step each 8 us 11 = 25 mV step each 16 us
SW1ADVSSPEED1	7	R/W	RESETB	0	
SW1APANIC	8	R/W	RESETB	0	SW1A panic mode enable 1= panic mode enabled 0= panic mode disabled

Table 4-12. Register 28, Switchers 4 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
SW1ASFST	9	R/W	RESETB	1	SW1A softstart 1= soft start enabled 0= soft start disabled
SW1BMODE0	10	R/W	NONE	*	SW1B operating mode 00 = OFF 01 = PWM mode No Pulse Skipping 10 = PWM mode Pulse Skipping Allowed 11 = Low Power PFM mode
SW1BMODE1	11	R/W	RESETB	0	
SW1BSTBYMODE0	12	R/W	NONE	*	SW1B operating mode in standby 00 = OFF 01 = PWM mode No Pulse Skipping 10 = PWM mode Pulse Skipping Allowed 11 = Low Power PFM mode
SW1BSTBYMODE1	13	R/W	RESETB	0	
SW1BDVSSPEED0	14	R/W	RESETB	0	SW1B DVS speed setting 00 = 25mV step each 4us. Power Ready signal not influenced 01 = 25 mV step each 4 us 10 = 25 mV step each 8 us 11 = 25 mV step each 16 us
SW1BDVSSPEED1	15	R/W	RESETB	0	
SW1BPANIC	16	R/W	RESETB	0	SW1B panic mode enable 0= panic mode disabled 1= panic mode enabled
SW1BSFST	17	R/W	RESETB	1	SW1B softstart 1= soft start enabled 0= soft start disabled
PLLEN	18	R/W	RESETB	0	Switcher PLL enable 0 = PLL automatically enabled 1 = Forces PLL on
PLLX0	19	R/W	RESETB	0	Switcher PLL multiplication factor See Table 4-13
PLLX1	20	R/W	RESETB	0	
PLLX2	21	R/W	RESETB	1	
Reserved	22	R/W	RESETB	0	For future use
Reserved	23	R/W	RESETB	0	For future use

Table 4-13. PLL Multiplication Factor

PLLX[2:0]	Multiplication Factor	Switching Frequency (Hz)	ADC Core Frequency (MHz)
000	28	917 504	1.835
001	29	950 272	1.901
010	30	983 040	1.966
011	31	1 015 808	2.032

Table 4-13. PLL Multiplication Factor (continued)

PLLX[2:0]	Multiplication Factor	Switching Frequency (Hz)	ADC Core Frequency (MHz)
100	32	1 048 576	2.097
101	33	1 081 344	2.163
110	34	1 114 112	2.228
111	35	1 146 880	2.294

Table 4-14. Register 29, Switchers 5

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
SW2AMODE0	0	R/W	NONE	*	SW2A operating mode 00 = OFF 01 = PWM mode No Pulse Skipping 10 = PWM mode Pulse Skipping Allowed 11 = Low Power PFM mode
SW2AMODE1	1	R/W	RESETB	0	
SW2ASTBYMODE0	2	R/W	NONE	*	SW2A operating mode in standby 00 = OFF 01 = PWM mode No Pulse Skipping 10 = PWM mode Pulse Skipping Allowed 11 = Low Power PFM mode
SW2ASTBYMODE1	3	R/W	RESETB	0	
Reserved	4	R/W	RESETB	0	For future use
Reserved	5	R/W	RESETB	0	For future use
SW2ADVSSPEED0	6	R/W	RESETB	0	SW2A DVS speed setting 00 = 25mV step each 4us. Power Ready signal not influenced 01 = 25 mV step each 4 us 10 = 25 mV step each 8 us 11 = 25 mV step each 16 us
SW2ADVSSPEED1	7	R/W	RESETB	0	
SW2APANIC	8	R/W	RESETB	0	SW2A panic mode enable 1= panic mode enabled 0= panic mode disabled
SW2ASFST	9	R/W	RESETB	1	SW2A softstart 1= soft start enabled 0= soft start disabled
SW2BMODE0	10	R/W	NONE	*	SW2B operating mode 00 = OFF 01 = PWM mode No Pulse Skipping 10 = PWM mode Pulse Skipping Allowed 11 = Low Power PFM mode
SW2BMODE1	11	R/W	RESETB	0	
SW2BSTBYMODE0	12	R/W	NONE	*	SW2B operating mode in standby 00 = OFF 01 = PWM mode No Pulse Skipping 10 = PWM mode Pulse Skipping Allowed 11 = Low Power PFM mode
SW2BSTBYMODE1	13	R/W	RESETB	0	

Table 4-14. Register 29, Switchers 5 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
SW2BDVSSPEED0	14	R/W	RESETB	0	SW2B DVS speed setting 00 = 25mV step each 4us. Power Ready signal not influenced 01 = 25 mV step each 4 us 10 = 25 mV step each 8 us 11 = 25 mV step each 16 us
SW2BDVSSPEED1	15	R/W	RESETB	0	
SW2BPANIC	16	R/W	RESETB	0	SW2B panic mode enable 1= panic mode enabled 0= panic mode disabled
SW2BSFST	17	R/W	RESETB	1	SW2B softstart 1= soft start enabled 0= soft start disabled
SW30	18	R/W	NONE	*	SW3 setting
SW31	19	R/W	NONE	*	00 = 5.0 V 01 = 5.0 V 10 = 5.0 V 11 = 5.5 V
SW3EN	20	R/W	NONE	*	SW3 enable 0 = OFF 1 = ON
SW3STBY	21	R/W	RESETB	0	SW3 controlled by standby 0 = SW3 mode not controlled by Standby 1 = SW3 mode controlled by Standby
SW3MODE	22	R/W	RESETB	0	SW3 operating mode 0 = SW3 low power mode disabled 1 = SW3 low power mode enabled
Reserved	23	R/W	RESETB	0	For future use

4.2 Linear Regulator Switchers

4.2.1 General Description

Table 4-15 summarizes the above described behavior with VxEN = regulator enable bit and VxMODE = regulator power mode bit, under the assumption that a single SPI controls a regulator.

Table 4-15. Regulator Standby Control

VxEN	VxMODE	VxSTBY	STANDBY Pin	Regulator Vx
0	X	X	X	Off
1	0	0	X	On
1	1	0	X	Low Power
1	X	1	0	On

Table 4-15. Regulator Standby Control (continued)

VxEN	VxMODE	VxSTBY	STANDBY Pin	Regulator Vx
1	0	1	1	Off
1	1	1	1	Low Power
This table is valid for all regulators, except for: • VRFBG which has no low power mode • VVIB which has no low power mode and no standby control • ADREF which has no standby control For those cases consider the VxMODE or VxSTBY bits to be 0.				

Table 4-16. Regulator Highest Power Mode Arbitration

Regulator Vx Mode Primary SPI Control	Regulator Vx Mode Secondary SPI Control	Regulator Vx Resulting Mode[1]	Read Back VxEN[2]	Read Back VxMODE[2]
Off	Off	Off	0	X
Off	Low Power	Low Power	1	1
Low Power	Off			
Low Power	Low Power			
X	On	On	1	0
On	X			

1 The resulting mode is also dependent on the VxSEL[1:0] setting, seeChapter 1, “Programmability”.

2 Valid for all regulators except VSIM when SIMEN is low, Chapter 4, “Supplies”.

The read back of the regulator control bits is based on the actual operating mode of the regulator. The three modes off, low power and on are coded on the VxEN and VxMODE bits according to Table 4-16. As a result, the value read back may be different than the value written to these bits. Both the primary and secondary SPI will read back the same data independent of the fact if they have control or not over the regulator mode. The VxSTBY bit is not affected by this and is read back as programmed.

4.2.2 SPI Registers

Table 4-17. Register 16, Regen Assignment

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
VAUDIOREGEN	0	R/W	RESETB	0	VAUDIO enabled by REGEN 0 = Enable of Vaudio regulator is not gated by REGEN 1 = Enable of Vaudio regulator is gated by REGEN
VIOHIREGEN	1	R/W	RESETB	0	VIOHI enabled by REGEN 0 = Enable of Viohi regulator is not gated by REGEN 1 = Enable of Viohi regulator is gated by REGEN
VIOLOREGEN	2	R/W	RESETB	0	VIOLO enabled by REGEN 0 = Enable of Violo regulator is not gated by REGEN 1 = Enable of Violo regulator is gated by REGEN

Table 4-17. Register 16, Regen Assignment (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
VDIGREGEN	3	R/W	RESETB	0	VDIG enabled by REGEN 0 = Enable of Vdig regulator is not gated by REGEN 1 = Enable of Vdig regulator is gated by REGEN
VGENREGEN	4	R/W	RESETB	0	VGEN enabled by REGEN 0 = Enable of Vgen regulator is not gated by REGEN 1 = Enable of Vgen regulator is gated by REGEN
VRFDIGREGEN	5	R/W	RESETB	0	VRFDIG enabled by REGEN 0 = Enable of Vrfdig regulator is not gated by REGEN 1 = Enable of Vrfdig regulator is gated by REGEN
VRFREFREGEN	6	R/W	RESETB	0	VRFREF enabled by REGEN 0 = Enable of Vrfref regulator is not gated by REGEN 1 = Enable of Vrfref regulator is gated by REGEN
VRFCPREGEN	7	R/W	RESETB	0	VRFCP enabled by REGEN 0 = Enable of Vrfcp regulator is not gated by REGEN 1 = Enable of Vrfcp regulator is gated by REGEN
VCAMREGEN	8	R/W	RESETB	0	VCAM enabled by REGEN 0 = Enable of Vcam regulator is not gated by REGEN 1 = Enable of Vcam regulator is gated by REGEN
VRFBGREGEN	9	R/W	RESETB	0	VRFBG enabled by REGEN 0 = Enable of Vrfbg regulator is not gated by REGEN 1 = Enable of Vrfbg regulator is gated by REGEN
VRF1REGEN	10	R/W	RESETB	0	VRF1 enabled by REGEN 0 = Enable of Vrf1 regulator is not gated by REGEN 1 = Enable of Vrf1 regulator is gated by REGEN
VRF2REGEN	11	R/W	RESETB	0	VRF2 enabled by REGEN 0 = Enable of Vrf2 regulator is not gated by REGEN 1 = Enable of Vrf2 regulator is gated by REGEN
VMMC1REGEN	12	R/W	RESETB	0	VMMC1 enabled by REGEN 0 = Enable of Vmmc1 regulator is not gated by REGEN 1 = Enable of Vmmc1 regulator is gated by REGEN
VMMC2REGEN	13	R/W	RESETB	0	VMMC2 enabled by REGEN 0 = Enable of Vmmc2 regulator is not gated by REGEN 1 = Enable of Vmmc2 regulator is gated by REGEN
Reserved	14	R/W	RESETB	0	For future use
Reserved	15	R/W	RESETB	0	For future use
GPO1REGEN	16	R/W	RESETB	0	GPO1 enabled by REGEN 0 = Enable of GPO1 generic output is not gated by REGEN 1 = Enable of GPO1 generic output is gated by REGEN
GPO2REGEN	17	R/W	RESETB	0	GPO2 enabled by REGEN 0 = Enable of GPO2 generic output is not gated by REGEN 1 = Enable of GPO2 generic output is gated by REGEN

Table 4-17. Register 16, Regen Assignment (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
GPO3REGEN	18	R/W	RESETB	0	GPO3 enabled by REGEN 0 = Enable of GPO3 generic output is not gated by REGEN 1 = Enable of GPO3 generic output is gated by REGEN
GPO4REGEN	19	R/W	RESETB	0	GPO4 enabled by REGEN 0 = Enable of GPO4 generic output is not gated by REGEN 1 = Enable of GPO4 generic output is gated by REGEN
REGENINV	20	R/W	RESETB	0	REGEN polarity inversion 0 = REGEN pin is active high 1 = REGEN pin is active low
VESIMESIMEN	21	R/W	RESETB	1	VESIM enabled by ESIMEN 0 = Enable of Vesim regulator is not gated by REGEN 1 = Enable of Vesim regulator is gated by REGEN
VMMC1ESIMEN	22	R/W	RESETB	0	VMMC1 enabled by ESIMEN 0 = Enable of Vmmc1 regulator is not gated by REGEN 1 = Enable of Vmmc1 regulator is gated by REGEN
VMMC2ESIMEN	23	R/W	RESETB	0	VMMC2 enabled by ESIMEN 0 = Enable of Vmmc2 regulator is not gated by REGEN 1 = Enable of Vmmc2 regulator is gated by REGEN

Table 4-18. Register 30, Regulator Setting 0

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
Reserved	0	R/W	RESETB	0	For future use
Reserved	1	R/W	RESETB	0	For future use
VIOLO0	2	R/W	NONE	*	VIOLO setting 00 = 1.20 V - 150 mA 01 = 1.30 V - 150 mA 10 = 1.50 V - 200 mA 11 = 1.80 V - 200 mA
VIOLO1	3	R/W	NONE	*	
VDIG0	4	R/W	NONE	*	VDIG setting 00 = 1.20 V - 150 mA 01 = 1.30 V - 150 mA 10 = 1.50 V - 200 mA 11 = 1.80 V - 200 mA
VDIG1	5	R/W	NONE	*	

Table 4-18. Register 30, Regulator Setting 0 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
VGEN0	6	R/W	NONE	*	VGEN setting 000 = 1.20 V - 150 mA 001 = 1.30 V - 150 mA 010 = 1.50 V - 200 mA 011 = 1.80 V - 200 mA 100 = 1.10 V - 150 mA 101 = 2.00 V - 200 mA 110 = 2.775 V - 200 mA 111 = 2.40 V - 200 mA
VGEN1	7	R/W	NONE	*	
VGEN2	8	R/W	NONE	*	
VRFDIG0	9	R/W	NONE	*	VRFDIG setting 00 = 1.20 V - 150 mA 01 = 1.50 V - 150 mA 10 = 1.80 V - 200 mA 11 = 1.875 V - 200 mA
VRFDIG1	10	R/W	NONE	*	
VRFREF0	11	R/W	NONE	*	VRFREF setting 00 = 2.475 V - 50 mA 01 = 2.60 V - 50 mA 10 = 2.70 V - 50 mA 11 = 2.775 V - 50 mA
VRFREF1	12	R/W	NONE	*	
VRFCP	13	R/W	NONE	*	VRFCP setting 0 = 2.700 V - 50 mA 1 = 2.775 V - 50 mA
VSIM	14	R/W	NONE	*	VSIM setting 0 = 1.8 V - 60 mA 1 = 2.9 V - 60 mA
VESIM	15	R/W	NONE	*	VESIM setting 0 = 1.8 V - 60 mA 1 = 2.9 V - 60 mA
VCAM0	16	R/W	NONE	*	VCAM setting 000 = 1.50 V - 150 mA 001 = 1.80 V - 150 mA 010 = 2.50 V - 150 mA 011 = 2.55 V - 150 mA 100 = 2.60 V - 150 mA 101 = 2.75 V - 150 mA 110 = 2.80 V - 150 mA 111 = 3.00 V - 150 mA
VCAM1	17	R/W	NONE	*	
VCAM2	18	R/W	NONE	*	
Reserved	19	R/W	RESETB	0	For future use
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Table 4-19. Register 31, Regulator Setting 1

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
VVIB0	0	R/W	RESETB	0	VVIB setting 00 = 1.30 V - 200 mA 01 = 1.80 V - 200 mA 10 = 2.00 V - 200 mA 11 = 3.00 V - 200 mA
VVIB1	1	R/W	RESETB	0	
VRF10	2	R/W	NONE	*	VRF1 setting 00 = 1.500 V - 350 mA 01 = 1.875 V - 350 mA 10 = 2.700 V - 350 mA 11 = 2.775 V - 350 mA
VRF11	3	R/W	NONE	*	
VRF20	4	R/W	NONE	*	VRF2 setting 00 = 1.500 V - 350 mA 01 = 1.875 V - 350 mA 10 = 2.700 V - 350 mA 11 = 2.775 V - 350 mA
VRF21	5	R/W	NONE	*	
VMMC10	6	R/W	NONE	*	VMMC1 setting 000 = 1.60 V - 350 mA 001 = 1.80 V - 350 mA 010 = 2.00 V - 350 mA 011 = 2.60 V - 350 mA 100 = 2.70 V - 350 mA 101 = 2.80 V - 350 mA 110 = 2.90 V - 350 mA 110 = 3.00 V - 350 mA
VMMC11	7	R/W	NONE	*	
VMMC12	8	R/W	NONE	*	
VMMC20	9	R/W	NONE	*	VMMC2 setting 000 = 1.60 V - 350 mA 001 = 1.80 V - 350 mA 010 = 2.00 V - 350 mA 011 = 2.60 V - 350 mA 100 = 2.70 V - 350 mA 101 = 2.80 V - 350 mA 110 = 2.90 V - 350 mA 110 = 3.00 V - 350 mA
VMMC21	10	R/W	NONE	*	
VMMC22	11	R/W	NONE	*	
Reserved	12	R/W	RESETB	0	For future use
Reserved	13	R/W	RESETB	0	For future use
Reserved	14	R/W	RESETB	0	For future use
Reserved	15	R/W	RESETB	0	For future use
Unused	16	R		0	Not available
Unused	17	R		0	Not available
Unused	18	R		0	Not available
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available

Table 4-19. Register 31, Regulator Setting 1 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Table 4-20. Register 32, Regulator Mode 0

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
VAUDIOEN	0	R/W	NONE	*	VAUDIO enable (see Section 4.2.1, “General Description”) 0 = OFF 1 = ON
VAUDIOSTBY	1	R/W	RESETB	0	VAUDIO controlled by standby (see Section 4.2.1, “General Description”) 0 = Vaudio mode not controlled by Standby 1 = Vaudio mode controlled by Standby
VAUDIOMODE	2	R/W	RESETB	0	VAUDIO operating mode (see Section 4.2.1, “General Description”) 0 = Vaudio low power mode disabled 1 = Vaudio low power mode enabled
VIOHIEN	3	R/W	NONE	*	VIOHI enable (see Section 4.2.1, “General Description”) 0 = OFF 1 = ON
VIOHISTBY	4	R/W	RESETB	0	VIOHI controlled by standby (see Section 4.2.1, “General Description”) 0 = Viohi mode not controlled by Standby 1 = Viohi mode controlled by Standby
VIOHIMODE	5	R/W	RESETB	0	VIOHI operating mode (see Section 4.2.1, “General Description”) 0 = Viohi low power mode disabled 1 = Viohi low power mode enabled
VIOLOEN	6	R/W	NONE	*	VIOLO enable (see Section 4.2.1, “General Description”) 0 = OFF 1 = ON
VIOLOSTBY	7	R/W	RESETB	0	VIOLO controlled by standby (see Section 4.2.1, “General Description”) 0 = Violo mode not controlled by Standby 1 = Violo mode controlled by Standby
VIOLOMODE	8	R/W	RESETB	0	VIOLO operating mode (see Section 4.2.1, “General Description”) 0 = Violo low power mode disabled 1 = Violo low power mode enabled

Table 4-20. Register 32, Regulator Mode 0 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
VDIGEN	9	R/W	NONE	*	VDIG enable (see Section 4.2.1, “General Description”) 0 = OFF 1 = ON
VDIGSTBY	10	R/W	RESETB	0	VDIG controlled by standby (see Section 4.2.1, “General Description”) 0 = Vdig mode not controlled by Standby 1 = Vdig mode controlled by Standby
VDIGMODE	11	R/W	RESETB	0	VDIG operating mode (see Section 4.2.1, “General Description”) 0 = Vdig low power mode disabled 1 = Vdig low power mode enabled
VGENEN	12	R/W	NONE	*	VGEN enable (see Section 4.2.1, “General Description”) 0 = OFF 1 = ON
VGENSTBY	13	R/W	RESETB	0	VGEN controlled by standby (see Section 4.2.1, “General Description”) 0 = Vgen mode not controlled by Standby 1 = Vgen mode controlled by Standby
VGENMODE	14	R/W	RESETB	0	VGEN operating mode (see Section 4.2.1, “General Description”) 0 = Vgen low power mode disabled 1 = Vgen low power mode enabled
VRFDIGEN	15	R/W	NONE	*	VRFDIG enable (see Section 4.2.1, “General Description”) 0 = OFF 1 = ON
VRFDIGSTBY	16	R/W	RESETB	0	VRFDIG controlled by standby (see Section 4.2.1, “General Description”) 0 = Vrfdig mode not controlled by Standby 1 = Vrfdig mode controlled by Standby
VRFDIGMODE	17	R/W	RESETB	0	VRFDIG operating mode (see Section 4.2.1, “General Description”) 0 = Vrfdig low power mode disabled 1 = Vrfdig low power mode enabled
VRFREFEN	18	R/W	NONE	*	VRFREF enable (see Section 4.2.1, “General Description”) 0 = OFF 1 = ON
VRFREFSTBY	19	R/W	RESETB	0	VRFREF controlled by standby (see Section 4.2.1, “General Description”) 0 = Vrfref mode not controlled by Standby 1 = Vrfref mode controlled by Standby

Table 4-20. Register 32, Regulator Mode 0 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
VRFREFMODE	20	R/W	RESETB	0	VRFREF operating mode (see Section 4.2.1, “General Description”) 0 = Vrfref low power mode disabled 1 = Vrfdref low power mode enabled
VRFCPEN	21	R/W	NONE	*	VRFCP enable (see Section 4.2.1, “General Description”) 0 = OFF 1 = ON
VRFCPSTBY	22	R/W	RESETB	0	VRFCP controlled by standby (see Section 4.2.1, “General Description”) 0 = Vrfcp mode not controlled by Standby 1 = Vrfcp mode controlled by Standby
VRFCPMODE	23	R/W	RESETB	0	VRFCP operating mode (see Section 4.2.1, “General Description”) 0 = Vrfcp low power mode disabled 1 = Vrfcp low power mode enabled

Table 4-21. Register 33, Regulator Mode 1

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
VSIMEN	0	R/W	NONE	*	VSIM enable (see Section 4.2.1, “General Description”) 0 = OFF 1 = ON
VSIMSTBY	1	R/W	RESETB	0	VSIM controlled by standby (see Section 4.2.1, “General Description”) 0 = Vsim mode not controlled by Standby 1 = Vsim mode controlled by Standby
VSIMMODE	2	R/W	RESETB	0	VSIM operating mode (see Section 4.2.1, “General Description”) 0 = Vsim low power mode disabled 1 = Vsim low power mode enabled
VESIMEN	3	R/W	NONE	*	VESIM enable (see Section 4.2.1, “General Description”) 0 = OFF 1 = ON
VESIMSTBY	4	R/W	RESETB	0	VESIM controlled by standby (see Section 4.2.1, “General Description”) 0 = Vesim mode not controlled by Standby 1 = Vesim mode controlled by Standby
VESIMMODE	5	R/W	RESETB	0	VESIM operating mode (see Section 4.2.1, “General Description”) 0 = Vesim low power mode disabled 1 = Vesim low power mode enabled

Table 4-21. Register 33, Regulator Mode 1 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
VCAMEN	6	R/W	NONE	*	VCAM enable (see Section 4.2.1, “General Description”) 0 = OFF 1 = ON
VCAMSTBY	7	R/W	RESETB	0	VCAM controlled by standby (see Section 4.2.1, “General Description”) 0 = Vcam low power mode disabled 1 = Vcam low power mode enabled
VCAMMODE	8	R/W	RESETB	0	VCAM operating mode (see Section 4.2.1, “General Description”) 0 = Vcam mode not controlled by Standby 1 = Vcam mode controlled by Standby
VRFBGEN	9	R/W	NONE	*	VRFBG enable (see Section 4.2.1, “General Description”) 0 = OFF 1 = ON
VRFBGSTBY	10	R/W	RESETB	0	VRFBG controlled by standby (see Section 4.2.1, “General Description”) 0 = Vrfbg low power mode disabled 1 = Vrfbg low power mode enabled
VVIBEN	11	R/W	RESETB	0	VVIB enable (see Section 4.2.1, “General Description”) 0 = OFF 1 = ON
VRF1EN	12	R/W	NONE	*	VRF1 enable (see Section 4.2.1, “General Description”) 0 = OFF 1 = ON
VRF1STBY	13	R/W	RESETB	0	VRF1 controlled by standby (see Section 4.2.1, “General Description”) 0 = Vrf1 mode not controlled by Standby 1 = Vrf1 mode controlled by Standby
VRF1MODE	14	R/W	RESETB	0	VRF1 operating mode (see Section 4.2.1, “General Description”) 0 = Vrf1 low power mode disabled 1 = Vrf1 low power mode enabled
VRF2EN	15	R/W	NONE	*	VRF2 enable (see Section 4.2.1, “General Description”) 0 = OFF 1 = ON
VRF2STBY	16	R/W	RESETB	0	VRF2 controlled by standby (see Section 4.2.1, “General Description”) 0 = Vrf2 mode not controlled by Standby 1 = Vrf2 mode controlled by Standby

Table 4-21. Register 33, Regulator Mode 1 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
VRF2MODE	17	R/W	RESETB	0	VRF2 operating mode (see Section 4.2.1, “General Description”) 0 = Vrf2 low power mode disabled 1 = Vrf2 low power mode enabled
VMMC1EN	18	R/W	NONE	*	VMMC1 enable (see Section 4.2.1, “General Description”) 0 = OFF 1 = ON
VMMC1STBY	19	R/W	RESETB	0	VMMC1 controlled by standby (see Section 4.2.1, “General Description”) 0 = Vmmc1 mode not controlled by Standby 1 = Vmmc1 mode controlled by Standby
VMMC1MODE	20	R/W	RESETB	0	VMMC1 operating mode (see Section 4.2.1, “General Description”) 0 = Vmmc1 low power mode disabled 1 = Vmmc1 low power mode enabled
VMMC2EN	21	R/W	NONE	*	VMMC2 enable (see Section 4.2.1, “General Description”) 0 = OFF 1 = ON
VMMC2STBY	22	R/W	RESETB	0	VMMC2 controlled by standby (see Section 4.2.1, “General Description”) 0 = Vmmc2 low power mode disabled 1 = Vmmc2 low power mode enabled
VMMC2MODE	23	R/W	RESETB	0	VMMC2 operating mode (see Section 4.2.1, “General Description”) 0 = Vmmc2 mode not controlled by Standby 1 = Vmmc2 mode controlled by Standby

Table 4-22. Register 34, Power Miscellaneous

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
Reserved	0	R/W	RESETB	0	For future use
Reserved	1	R/W	RESETB	0	For future use
Reserved	2	R/W	RESETB	0	For future use
Reserved	3	R/W	RESETB	0	For future use
Reserved	4	R/W	RESETB	0	For future use
Reserved	5	R/W	RESETB	0	For future use
GPO1EN	6	R/W	RESETB	0	GPO1 enable 0 = OFF 1 = ON

Table 4-22. Register 34, Power Miscellaneous (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
GPO1STBY	7	R/W	RESETB	0	GPO1 controlled by standby 0 = GPO1 mode not controlled by Standby 1 = GPO1 mode controlled by Standby
GPO2EN	8	R/W	RESETB	0	GPO2 enable 0 = OFF 1 = ON
GPO2STBY	9	R/W	RESETB	0	GPO2 controlled by standby 0 = GPO2 mode not controlled by Standby 1 = GPO2 mode controlled by Standby
GPO3EN	10	R/W	RESETB	0	GPO3 enable 0 = OFF 1 = ON
GPO3STBY	11	R/W	RESETB	0	GPO3 controlled by standby 0 = GPO3 mode not controlled by Standby 1 = GPO3 mode controlled by Standby
GPO4EN	12	R/W	RESETB	0	GPO4 enable 0 = OFF 1 = ON
GPO4STBY	13	R/W	RESETB	0	GPO4 controlled by standby 0 = GPO4 mode not controlled by Standby 1 = GPO4 mode controlled by Standby
VIBPINCTRL	14	R/W	RESETB	0	Enables control of VVIB by VIBEN pin See Table 4-23
PWGT1SPIEN	15	R/W	RESETB	0	Power gate 1 enable See Table 4-24
PWGT2SPIEN	16	R/W	RESETB	0	Power gate 2 enable See Table 4-24
Reserved	17	R/W	RESETB	0	For future use
Unused	18	R		0	Not available
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Table 4-23. VVIB Enabling Logic Table

Bit VVIBEN (Write)	Bit VIBPINCTRL	Pin VIBEN	Regulator VVIB[1]	Bit VVIBEN (Read)
0	0	X	Off	0
0	1	0	Off	0

Table 4-23. VVIB Enabling Logic Table (continued)

Bit VVIBEN (Write)	Bit VIBPINCTRL	Pin VIBEN	Regulator VVIB[1]	Bit VVIBEN (Read)
0	1	1	On	1
1	X	X	On	1

1 In case of dual SPI control over VVIB, the highest power mode is selected.

Table 4-24. Power Gating Logic Table[1]

Bit PWGTxSPIEN 0 = Default	Pin PWGTxEN	PWGTxDRV	Read Back PWGTxSPIEN
1	X	Low	0
0	0	High	1
0	1	Low	0

1 Applicable for watchdog, on and user off wait modes only.
If PWGT1SPIEN = PWGT2SPIEN = 1, then the charge pump is disabled.

Table 4-25. Register 35, Power Spare

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
Unused	0	R		0	Not available
Unused	1	R		0	Not available
Unused	2	R		0	Not available
Unused	3	R		0	Not available
Unused	4	R		0	Not available
Unused	5	R		0	Not available
Unused	6	R		0	Not available
Unused	7	R		0	Not available
Unused	8	R		0	Not available
Unused	9	R		0	Not available
Unused	10	R		0	Not available
Unused	11	R		0	Not available
Unused	12	R		0	Not available
Unused	13	R		0	Not available
Unused	14	R		0	Not available
Unused	15	R		0	Not available
Unused	16	R		0	Not available
Unused	17	R		0	Not available

Table 4-25. Register 35, Power Spare (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
Unused	18	R		0	Not available
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Chapter 5
Audio

Table 5-1. Register 36, Audio Rx 0

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
VAUDIOON	0	R/W	RESETB	0	Forces VAUDIO in active on mode See Table 5-2
BIASEN	1	R/W	RESETB	0	Audio bias enable 0 = Audio bias disabled 1 = Audio bias enabled
BIASSPEED	2	R/W	RESETB	0	Turn on ramp speed of the audio bias 0 = Slow ramp activated (250 ms) 1 = Fast ramp activated (25 ms)
ASPEN	3	R/W	RESETB	0	Amplifier ASP enable 0 = ASP amplifier (earpiece) disabled 1 = ASP amplifier (earpiece) enabled
ASPSEL	4	R/W	RESETB	0	Asp input selector 0 = CODEC 1 = Right
ALSPEN	5	R/W	RESETB	0	Amplifier Alsp enable 0 = ALSP amplifier (loudspeaker) disabled 1 = ALSP amplifier (loudspeaker) enabled
ALSPREF	6	R/W	RESETB	0	Bias Alsp at common audio reference 0 = ALSP Bias Center Voltage is BP/2 1 = ALSP Bias Center Voltage is REFA (Vaudio /2)
ALSPSEL	7	R/W	RESETB	0	Alsp input selector 0 = CODEC 1 = Right
LSPLEN	8	R/W	RESETB	0	Output LSPL enable 0 = LSPL amplifier disabled 1 = LSPL amplifier enabled
AHSREN	9	R/W	RESETB	0	Amplifier AhsR enable 0 = Right channel headset amplifier disabled 1 = Right channel headset amplifier enabled
AHSLEN	10	R/W	RESETB	0	Amplifier AhsL enable 0 = Left channel headset amplifier disabled 1 = Left channel headset amplifier enabled
AHSSEL	11	R/W	RESETB	0	Ahsr and Ahsl input selector 0 = CODEC for Ahsr and Ahsl 1 = Right for Ahsr and left for Ahsl

Table 5-1. Register 36, Audio Rx 0 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
HSPGDIS	12	R/W	RESETB	1	Phantom ground disable 0 = Enable Phantom ground output 1 = Disable Phantom ground output
HSDETEN	13	R/W	RESETB	0	Headset detect enable 0 = Disable headset detector 1 = Enable headset detector See Table 5-2
HSDETAUTOB	14	R/W	RESETB	0	Amplifier state determined by headset detect 0 = Ahsr, Ahsl, Amc2 amplifiers state determined by headset detection 1 = Ahsr, Ahsl, Amc2 amplifiers state not determined by headset detection
ARXOUTREN	15	R/W	RESETB	0	Output RXOUTR enable 0 = RXOUTR amplifier disabled 1 = RXOUTR amplifier enabled
ARXOUTLEN	16	R/W	RESETB	0	Output RXOUTL enable 0 = RXOUTL amplifier disabled 1 = RXOUTL amplifier enabled
ARXOUTSEL	17	R/W	RESETB	0	Arxout input selector 0 = CODEC for Rxoutr and Rxoutl 1 = Right for Rxoutr and left for Rxoutl
CDCOUTEN	18	R/W	RESETB	0	Output CDCOUT enable 0 = CDCOUT amplifier disabled 1 = CDCOUT amplifier enabled
HSLDETEN	19	R/W	RESETB	0	Headset left channel detect enable 0 = Disable headset left channel detector 1 = Enable headset left channel detector See Table 5-2
Reserved	20	R/W	RESETB	0	For future use
ADDCDC	21	R/W	RESETB	0	Adder channel CODEC selection 0 = PGArx CODEC output not added to the mixer 1 = Add PGArx CODEC output to the mixer
ADDSTDC	22	R/W	RESETB	0	Adder channel stereo DAC selection 0 = PGAst stereo DAC outputs not added to the mixer 1 = Add PGAst stereo DAC outputs to the mixer
ADDRXIN	23	R/W	RESETB	0	Adder channel line in selection 0 = PGArxin line in outputs not added to the mixer 1 = Add PGArxin line in outputs to the mixer

Table 5-2. VAUDIO Forced Enable Function

VAUDIOEN	VAUDIOMODE	VAUDIOSTBY	STANDBY pin	AUDIOON	VAUDIO
0	X	X	X	0	Off
1	0	0	X	0	On
1	1	0	X	0	Low Power

Table 5-2. VAUDIO Forced Enable Function (continued)

VAUDIOEN	VAUDIOMODE	VAUDIOSTBY	STANDBY pin	AUDIOON	VAUDIO
1	X	1	0	0	On
1	0	1	1	0	Off
1	1	1	1	0	Low Power
X	X	X	X	1	On

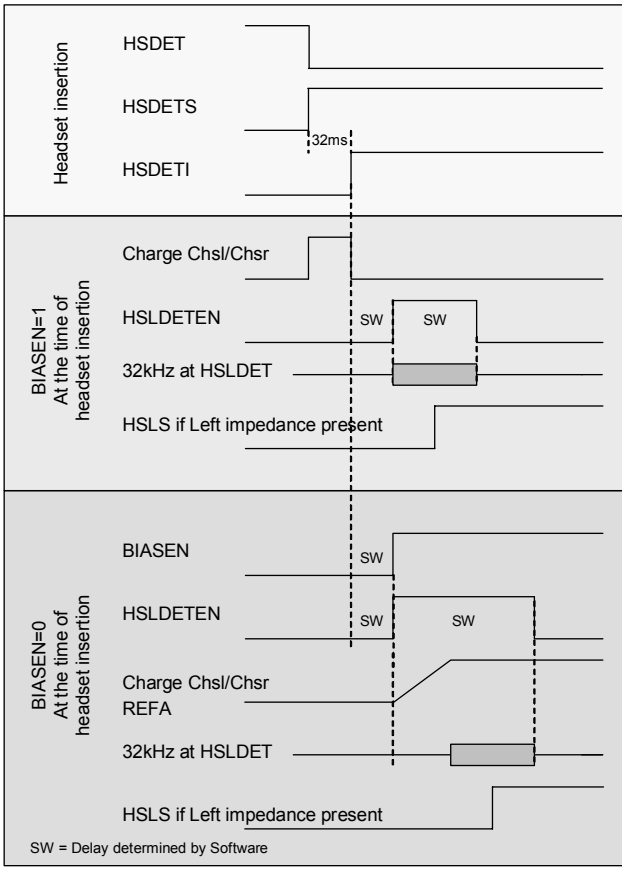

Figure 5-1. Stereo Headset Detection Timing Diagrams

Table 5-3. Register 37, Audio Rx 1

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
PGARXEN	0	R/W	RESETB	0	CODEC receive PGA enable 0 = Disable CODEC receive PGA 1 = Enable CODEC receive PGA

Table 5-3. Register 37, Audio Rx 1 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
PGARX0	1	R/W	RESETB	1	CODEC receive gain setting 0000 = -33 0001 = -33 0010 = -33 0011 = -30 0100 = -27 0101 = -24 0110 = -21 0111 = -18 1000 = -15 1001 = -12 1010 = -9 1011 = -6 1100 = -3 1101 = 0 1110 = +3 1111 = +6
PGARX1	2	R/W	RESETB	0	
PGARX2	3	R/W	RESETB	1	
PGARX3	4	R/W	RESETB	1	
PGASTEN	5	R/W	RESETB	0	Stereo DAC PGA enable 0 = Disable Stereo DAC PGA 1 = Enable Stereo DAC PGA
PGAST0	6	R/W	RESETB	1	Stereo DAC gain setting 0000 = -33 0001 = -33 0010 = -33 0011 = -30 0100 = -27 0101 = -24 0110 = -21 0111 = -18 1000 = -15 1001 = -12 1010 = -9 1011 = -6 1100 = -3 1101 = 0 1110 = +3 1111 = +6
PGAST1	7	R/W	RESETB	0	
PGAST2	8	R/W	RESETB	1	
PGAST3	9	R/W	RESETB	1	
ARXINEN	10	R/W	RESETB	0	Amplifier Arx enable 0 = Disable ARX amplifiers 1 = Enable ARX amplifiers
ARXIN	11	R/W	RESETB	0	Amplifier Arx additional gain setting 0 = No additional gain 1 = 18 dB additional gain

Table 5-3. Register 37, Audio Rx 1 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
PGARXIN0	12	R/W	RESETB	1	PGArxin gain setting 0000 = -33 0001 = -33 0010 = -33 0011 = -30 0100 = -27 0101 = -24 0110 = -21 0111 = -18 1000 = -15 1001 = -12 1010 = -9 1011 = -6 1100 = -3 1101 = 0 1110 = +3 1111 = +6
PGARXIN1	13	R/W	RESETB	0	
PGARXIN2	14	R/W	RESETB	1	
PGARXIN3	15	R/W	RESETB	1	
MONO0	16	R/W	RESETB	0	Mono adder setting 00: Left and Right Channels independent 01: Stereo Opposite (Left Channel in opposite phase) 10: Stereo to Mono Conversion (Left and Right Channels added and routed to both outputs) 11: Mono Opposite (Left and Right channels added and routed to right output, the opposite routed to left output)
MONO1	17	R/W	RESETB	0	
BAL0	18	R/W	RESETB	0	Balance attenuation setting: -21 dB to 0 dB in 3 dB steps 000 = 0 dB 001 = -3 dB 010 = -6 dB 011 = -9 dB 100 = -12 dB 101 = -15 dB 110 = -18 dB 111 = -21 dB
BAL1	19	R/W	RESETB	0	
BAL2	20	R/W	RESETB	0	
BALLR	21	R/W	RESETB	0	Channel selection for attenuation 0: Right Channel 1: Left Channel
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Table 5-4. Register 38, Audio Tx

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
MC1BEN	0	R/W	RESETB	0	Microphone bias 1 enable 0 = Microphone bias 1 disabled 1 = Microphone bias 1 enabled
MC2BEN	1	R/W	RESETB	0	Microphone bias 2 enable 0 = Microphone bias 2 disabled 1 = Microphone bias 2 enabled
MC2BDETDBNC	2	R/W	RESETB	0	Microphone bias detect debounce setting 0 = 30 ms debounce 1 = 100 ms debounce
MC2BDETEN	3	R/W	RESETB	0	Microphone bias 2 detect enable 0 = Microphone bias 2 detect disabled 1 = Microphone bias 2 detect enabled
Reserved	4	R/W	RESETB	0	For future use
AMC1REN	5	R/W	RESETB	0	Amplifier Amc1R enable See Table 5-5 0 = Amplifier Amc1R disabled 1 = Amplifier Amc1R enabled
AMC1RITOV	6	R/W	RESETB	0	Amplifier Amc1R current to voltage mode enable 0 = Amplifier Amc1R voltage to voltage mode enable 1 = Amplifier Amc1R current to voltage mode enable
AMC1LEN	7	R/W	RESETB	0	Amplifier Amc1L enable See Table 5-5 0 = Amplifier Amc1L disabled 1 = Amplifier Amc1L enabled
AMC1LITOV	8	R/W	RESETB	0	Amplifier Amc1L current to voltage mode enable 0 = Amplifier Amc1L voltage to voltage mode enable 1 = Amplifier Amc1L current to voltage mode enable
AMC2EN	9	R/W	RESETB	0	Amplifier Amc2 enable See Table 5-5 0 = Amplifier Amc2 disabled 1 = Amplifier Amc2 enabled
AMC2ITOV	10	R/W	RESETB	0	Amplifier Amc2 current to voltage mode enable 0 = Amplifier Amc2 voltage to voltage mode enable 1 = Amplifier Amc2 current to voltage mode enable
ATXINEN	11	R/W	RESETB	0	Amplifier Atxin enable 0 = Amplifier Atxin disabled 1 = Amplifier Atxin enabled
ATXOUTEN	12	R/W	RESETB	0	Reserved for output TXOUT enable, currently not used
RXINREC	13	R/W	RESETB	0	RXINR/RXINL to voice CODEC ADC routing enable See Table 5-5 0 = RXINR/RXINL not rooted to the CODECADC 1 = Root RXINR/RXINL to voice CODEC ADC, automatically enables the left channel ADC section of the voice CODEC if the voice CODEC was enabled via CDCEN

Table 5-4. Register 38, Audio Tx (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
PGATXR0	14	R/W	RESETB	0	Transmit gain setting right from -8 dB to +23 dB 00000 lowest gain, 11111 highest gain, 01000 default (0 dB)
PGATXR1	15	R/W	RESETB	0	
PGATXR2	16	R/W	RESETB	0	
PGATXR3	17	R/W	RESETB	1	
PGATXR4	18	R/W	RESETB	0	
PGATXL0	19	R/W	RESETB	0	Transmit gain setting left from -8 dB to +23 dB 00000 lowest gain, 11111 highest gain, 01000 default (0 dB)
PGATXL1	20	R/W	RESETB	0	
PGATXL2	21	R/W	RESETB	0	
PGATXL3	22	R/W	RESETB	1	
PGATXL4	23	R/W	RESETB	0	

Table 5-5. Input Selection Contingency Matrix

AMC1REN	AMC2EN	ATXINEN	RXINREC	Input selected	AMC1LEN	RXINREC	Input selected
1	x	x	x	MC1RIN	1	x	MC1LIN
0	1	x	x	MC2IN	0	1	RXINL[1]
0	0	1	x	TXIN	0	0	None
0	0	0	1	RXINR			
0	0	0	0	None			
Note: Voice CODEC right channel enabled when CDCEN = 1. Voice CODEC left channel enabled when CDCEN AND (AMC1LEN OR RXINREC) = 1.							

[1] Only valid if right input selected is RXINR, else None.

Table 5-6. Register 39, SSI Network

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
Reserved	0	R/W	RESETB	0	For future use
Reserved	1	R/W	RESETB	0	For future use
CDCTXRXSLOT0	2	R/W	RESETB	0	CODEC timeslot assignment Defines the primary receive timeslot: 00 = TS0 01 = TS1 10 = TS2 11 = TS3
CDCTXRXSLOT1	3	R/W	RESETB	0	

Table 5-6. Register 39, SSI Network (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
CDCTXSECSLOT0	4	R/W	RESETB	0	CODEC secondary transmit timeslot Defines the secondary transmit timeslot 00 = TS0 01 = TS1 10 = TS2 11 = TS3
CDCTXSECSLOT1	5	R/W	RESETB	1	
CDCRXSECSLOT0	6	R/W	RESETB	1	CODEC secondary receive timeslot Defines the secondary receive timeslot 00 = TS0 01 = TS1 10 = TS2 11 = TS3
CDCRXSECSLOT1	7	R/W	RESETB	0	
CDCRXSECGAIN0	8	R/W	RESETB	0	CODEC secondary receive channel gain setting Defines the gain applied to the secondary receive timeslots: 00 = No mixing 01 = 0 dB 10 = -6 dB 11 = -12 dB
CDCRXSECGAIN1	9	R/W	RESETB	0	
CDCSUMGAIN	10	R/W	RESETB	0	CODEC summed receive signal gain setting Defines the gain applied to the summed timeslots: 0: 0 dB 1: -6 dB If CDCRXSECGAIN[1:0] = 00 then the applied gain is 0 dB
CDCFSDLY	11	R/W	RESETB	0	CODEC framesync delay 0 = No delay 1 = Delay the FS with respect to the BCL
STDCSLOTS0	12	R/W	RESETB	1	Stereo DAC number of timeslots select 00 = 8 (Left, Right, 6 other)* 01 = 8 (Left, Right, 6 other)* 10 = 4 (Left, Right, 2 other) 11 = 2 (Left, Right) (*) Not available for 64 kHz and 96 kHz sample rates
STDCSLOTS1	13	R/W	RESETB	1	
STDCRXSLOT0	14	R/W	RESETB	0	Stereo DAC time slot assignment
STDCRXSLOT1	15	R/W	RESETB	0	Defines the primary receive timeslots: 00 = TS0 and TS1 01 = TS2 and TS3 10 = TS4 and TS5 11 = TS6 and TS7
STDCRXSECSLOT0	16	R/W	RESETB	1	Stereo DAC secondary receive timeslot Defines the secondary receive timeslots: 00 = TS0 and TS1 01 = TS2 and TS3 10 = TS4 and TS5 11 = TS6 and TS7 STDCRXSLOT[1:0] and STDCRXSECSLOT[1:0] must fit in the STDCSLOTS[1:0] setting else no output signal is generated
STDCRXSECSLOT1	17	R/W	RESETB	0	

Table 5-6. Register 39, SSI Network (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
STDCRXSECGAIN0	18	R/W	RESETB	0	Stereo DAC secondary receive channel gain setting Defines the gain applied to the secondary receive timeslots: 00 = No mixing 01 = 0dB 10 = -6dB 11 = -12dB STDCRXSLOT[1:0] and STDCRXSECSLOT[1:0] must fit in the STDCSLOTS[1:0] setting else no output signal is generated
STDCRXSECGAIN1	19	R/W	RESETB	0	
STDCSUMGAIN	20	R/W	RESETB	0	Stereo DAC summed receive signal gain setting Defines the gain applied to the summed timeslots: 0 = 0 dB 1 = -6 dB
Reserved	21	R/W	RESETB	0	For future use
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Table 5-7. Register 40, Audio CODEC

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
CDCSSISEL	0	R/W	RESETB	1	CODEC SSI bus select 0 = Enable FS1, BCL1 and RX1 digital audio I/O paths. 1 = Enable FS2, BCL2 and RX2 digital audio I/O paths.
CDCCLKSEL	1	R/W	RESETB	1	CODEC clock input select 0 = Select CLIA. 1 = Select CLIB
CDCSM	2	R/W	RESETB	1	CODEC slave / master select 0 = CODEC acts as a master with BCL and FS driven as outputs 1 = CODEC acts as a slave with BCL and FS driven as inputs
CDCBCLINV	3	R/W	RESETB	0	CODEC bit clock inversion 0 = Serial interface clock not inverted 1 = Invert interface clock
CDCFSINV	4	R/W	RESETB	0	CODEC framesync inversion 0 = Framesync not inverted 1 = Invert the frame sync
CDCFS0	5	R/W	RESETB	1	Bus protocol selection 00 = Long FS with no offset: NOT SUPPORTED 01 = Short FS with -1 offset (Network) 10 = Long FS with -1 offset (I2S) 11 = Short FS with no offset: NOT SUPPORTED
CDCFS1	6	R/W	RESETB	0	
CDCCLK0	7	R/W	RESETB	0	CODEC clock setting Selects the CODEC clock input and output frequencies See Table 5-8
CDCCLK1	8	R/W	RESETB	0	
CDCCLK2	9	R/W	RESETB	0	

Table 5-7. Register 40, Audio CODEC (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
CDCFS8K16K	10	R/W	RESETB	0	CODEC framesync select 0 = 8 kHz sampling selected 1 = 16 kHz sampling selected See Table 5-8
CDCEN	11	R/W	RESETB	0	CODEC enable Selects CODEC power up states. 0 = CODEC disabled 1 = Enables the voice CODEC core and convertors except for the left channel voice CODEC ADC for which also AMC1LEN has to be set to a 1
CDCCLKEN	12	R/W	RESETB	0	CODEC clocking enable 0 = If programmed low, FS and BCL outputs are tri-stated 1 = If CDCTS is low, FS and BCL outputs are enabled when in master mode. Outputs enabled only for digital audio I/O path selected by CDCSSISEL bit Provides master clock capability when CODEC D/A converter, A/D converter and digital filters are powered down by CDCEN
CDCTS	13	R/W	RESETB	0	CODEC SSI tristate 0 = FS, TX and BCL are not tri-stated 1 = FS, TX and BCL are tri-stated Note that this control function will occur asynchronously
CDCDITH	14	R/W	RESETB	0	CODEC dithering 0 = Dithering is enabled. Dithering decorrelates the periodic modulator quantization noise of the output converter. 1 = dithering is disabled
CDCRESET	15	R/W	RESETB	0	CODEC filter reset CDCRESET resets the digital filter in the CODEC. This bit should be set to a one when BCL, AUDOHPF, or AUDIHPF are changed. This is a self-clearing bit that will clear at the falling edge of SPI CE.
CDCBYP	16	R/W	RESETB	0	CODEC bypass 0 = CODEC is not bypassed. Normal operation 1 = Whole CODEC is bypassed and the analog signal coming from the microphone amplifiers is injected to the PGA
CDCALM	17	R/W	RESETB	0	CODEC analog loopback 0 = Analog loop-back is disabled. Normal operation. 1 = Loop Sigma Delta output of the A/D path back to the input of the analog part of D/A path (bit stream analog D to A converter). Analog loop-back mode is used for testing.
CDCDLM	18	R/W	RESETB	0	CODEC digital loopback 0 = Digital loop-back is disabled. Normal operation. 1 = Loop the 13-bit DIGITAL output of the A/D converter back to the 13-bit DIGITAL input of the D/A converter. Digital loop-back mode is used for testing.
AUDIHPF	19	R/W	RESETB	1	Transmit high pass filter enable 0 = Audio Input High Pass Filter disabled 1 = Audio Input High Pass Filter enabled

Table 5-7. Register 40, Audio CODEC (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
AUDOHPF	20	R/W	RESETB	1	Receive high pass filter enable 0 = Audio Output High Pass Filter disabled 1 = Audio Output High Pass Filter enabled
Unused	21	R/W	RESETB	0	Not available
Unused	22	R/W	RESETB	0	Not available
Unused	23	R/W	RESETB	0	Not available

Table 5-8. Telephone CODEC Input Clock Selection SPI Bits

CDCFS8K16K	CDCCLK2	CDCCLK1	CDCCLK0	CLI (MHz)	FS (kHz)	BCLMaster (kHz)
0	0	0	0	13.0	8	520
0	0	0	1	15.36	8	512
0	0	1	0	16.8	8	560
0	0	1	1	NA		
0	1	0	0	26.0	8	520
0	1	0	1	NA		
0	1	1	0	NA		
0	1	1	1	33.6	8	560
1	0	0	0	13	16	1040
1	0	0	1	15.36	16	1024
1	0	1	0	16.8	16	1120
1	0	1	1	NA		
1	1	0	0	26.0	16	1040
1	1	0	1	NA		
1	1	1	0	NA		
1	1	1	1	33.6	16	1120

Table 5-9. Register 41, Audio Stereo DAC

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
STDCSSISEL	0	R/W	RESETB	0	Stereo DAC SSI bus select 0 = Enable FS1, BCL1 and RX1 digital audio I/O paths 1 = Enable FS2, BCL2 and RX2 digital audio I/O paths
STDCCLKSEL	1	R/W	RESETB	0	Stereo DAC clock input select 0 = Select CLIA. 1 = Select CLIB

Table 5-9. Register 41, Audio Stereo DAC (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
STDCSM	2	R/W	RESETB	1	Stereo DAC slave / master select 0 = The DAC acts as a master with BCL and FS driven as outputs. 1 = The DAC acts as a slave with BCL and FS driven as inputs. See Table 5-10
STDCBCLINV	3	R/W	RESETB	0	Stereo DAC bit clock inversion 0 = Serial interface clock not inverted 1 = Invert interface clock
STDCFSINV	4	R/W	RESETB	0	Stereo DAC framesync inversion 0 = Framesync not inverted 1 = Invert the frame sync
STDCFS0	5	R/W	RESETB	0	Bus protocol selection 00 = Long FS with no offset (Normal) 01 = Short FS with -1 offset (Network) 10 = Long FS with -1 offset (I2S) 11 = Short FS with no offset
STDCFS1	6	R/W	RESETB	0	
STDCCLK0	7	R/W	RESETB	0	Stereo DAC clock setting Selects the PLL clock input frequencies: CLI, MCL, FS or BCL. See Table 5-10
STDCCLK1	8	R/W	RESETB	0	
STDCCLK2	9	R/W	RESETB	0	
STDCFSDLYB	10	R/W	RESETB	0	Stereo DAC framesync delay bar 0 = Delay the FS with respect to the BCL (default state) 1 = No delay added
STDCEN	11	R/W	RESETB	0	Stereo DAC enable Controls power up state of the stereo DAC 1 = The DAC is enabled 0 = The DAC is disabled
STDCCLKEN	12	R/W	RESETB	0	Stereo DAC clocking enable 0 = FS and BCL outputs are tri-stated. 1 = FS and BCL outputs are enabled when in master mode. Outputs enabled only for digital audio I/O path selected by STDCSSISEL bit. Provides master clock capability when ST_DAC D/A converter, and digital filters are powered down by STDCEN.
Reserved	13	R/W	RESETB	0	For future use
Reserved	14	R/W	RESETB	0	For future use
STDCRESET	15	R/W	RESETB	0	Stereo DAC filter reset Resets the digital filters in the DAC. This bit should be set to a one when BCL or SR are changed. This will be a self-clearing bit that will clear at the falling edge of SPI CE.
SPDIF	16	R/W	RESETB	0	Stereo DAC SSI SPDIF mode. Mode no longer available.

Table 5-9. Register 41, Audio Stereo DAC (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
SR0	17	R/W	RESETB	1	Stereo DAC sample rate See Table 5-11
SR1	18	R/W	RESETB	1	
SR2	19	R/W	RESETB	1	
SR3	20	R/W	RESETB	0	
Unused	21	R/W	RESETB	0	Not available
Unused	22	R/W	RESETB	0	Not available
Unused	23	R/W	RESETB	0	Not available

Table 5-10. Stereo DAC Input Clock Selection SPI Bits

STDCSM	STDCCLK2	STDCCLK1	STDCCLK0	PLL input
0 = Master	0	0	0	CLI = 13.0 MHz
0 = Master	0	0	1	CLI = 15.36 MHz
0 = Master	0	1	0	CLI = 16.8 MHz
0 = Master	0	1	1	NA
0 = Master	1	0	0	CLI = 26.0 MHz
0 = Master	1	0	1	CLI = 12.0 MHz
0 = Master	1	1	0	CLI = 3.6864 MHz
0 = Master	1	1	1	CLI = 33.6 MHz
1 = Slave	0	X	X	NA
1 = Slave	1	0	0	NA
1 = Slave	1	0	1	CLI = MCL, PLL disabled
1 = Slave	1	1	0	FS
1 = Slave	1	1	1	BCL

Table 5-11. Stereo DAC Sample Rate Selection SPI Bits

SR3	SR2	SR1	SR0	FS	N_{FS}	MCL	N_B	BCL
0	0	0	0	8000	512	4096k	16	256k
0	0	0	1	11025	512	5644.8k	16	352.8k
0	0	1	0	12000	512	6144k	16	384k
0	0	1	1	16000	256	4096k	8	512k
0	1	0	0	22050	256	5644.8k	8	705.6k
0	1	0	1	24000	256	6144k	8	768k

Table 5-11. Stereo DAC Sample Rate Selection SPI Bits (continued)

SR3	SR2	SR1	SR0	FS	N_{FS}	MCL	N_B	BCL
0	1	1	0	32000	128	4096k	4	1024k
0	1	1	1	44100	128	5644.8k	4	1411.2k
1	0	0	0	48000	128	6144k	4	1536k
1	0	0	1	64000	64	4096k	2	2048k
1	0	1	0	96000	64	6144k	2	3072k
1011 to 1111 are reserved combinations.								
Note: The above values are valid for a single timeslot pair.								

Table 5-12. Register 42, Audio Spare

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
Unused	0	R		0	Not available
Unused	1	R		0	Not available
Unused	2	R		0	Not available
Unused	3	R		0	Not available
Unused	4	R		0	Not available
Unused	5	R		0	Not available
Unused	6	R		0	Not available
Unused	7	R		0	Not available
Unused	8	R		0	Not available
Unused	9	R		0	Not available
Unused	10	R		0	Not available
Unused	11	R		0	Not available
Unused	12	R		0	Not available
Unused	13	R		0	Not available
Unused	14	R		0	Not available
Unused	15	R		0	Not available
Unused	16	R		0	Not available
Unused	17	R		0	Not available
Unused	18	R		0	Not available
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available

Table 5-12. Register 42, Audio Spare (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
Unused	22	R		0	Not available
Unused	23	R		0	Not available

Chapter 6
Battery Interface and Control

Table 6-1. Register 48, Charger 0

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
VCHRG0	0	R/W	RESETB	0	Sets the charge regulator output voltage 000 = 4.050 V 001 = 4.375 V 010 = 4.150 V 011 = 4.200 V 100 = 4.250 V 101 = 4.300 V 110 = 3.800 V 111 = 4.500 V
VCHRG1	1	R/W	RESETB	0	
VCHRG2	2	R/W	RESETB	0	
ICHRG0	3	R/W	RESETB	0	Sets the main charger DAC current See Table 6-2
ICHRG1	4	R/W	RESETB	0	
ICHRG2	5	R/W	RESETB	0	
ICHRG3	6	R/W	RESETB	0	
ICHRGTR0	7	R/W	RESETB	0	Sets the internal trickle charger current 000 = 0 mA 001 = 9 mA 010 = 20 mA 011 = 36 mA 100 = 42 mA 101 = 50 mA 110 = 59 mA 111 = 68 mA
ICHRGTR1	8	R/W	RESETB	0	
ICHRGTR2	9	R/W	RESETB	0	
FETOVRD	10	R/W	RESETB	0	BATTFET and BPFET control mode 0= BATTFET and BPFET outputs are controlled by hardware 1 = BATTFET and BPFET are controlled by the state of the FETCTRL bit
FETCTRL	11	R/W	RESETB	0	BATTFET and BPFET control setting 0 = BPFET is driven low, BATTFET is driven high if FETOVRD is set 1 = BPFET is driven high, BATTFET is driven low if FETOVRD is set
Reserved	12	R/W	RESETB	0	For future use
RVRSMODE	13	R/W	RESETB	0	Reverse mode enable 0 = Reverse mode disabled 1 = Reverse mode enabled

Table 6-1. Register 48, Charger 0 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
Reserved	14	R/W	RESETB	0	For future use
OVCTRL0	15	R/W	RESETB	0	Overvoltage threshold select 00 = 5.83 V (Should not be used in separate input configurations, this will disable the overvoltage setting) 01 = 6.90 V 10 = 9.80 V 11 = 19.6 V
OVCTRL1	16	R/W	RESETB	0	
UCHEN	17	R/W	RESETB	0	Unregulated charge enable 0 = Unregulated charge disabled 0 = Unregulated charge enabled
CHRGLEDEN	18	R/W	RESETB	0	CHRGLED enable 0 = CHRGLED disabled 1 = CHRGLED enabled
CHRGRAWPDEN	19	R/W	RESETB	0	Enables a 5K pull down at CHRGRAW 1 = The 5K pull down at CHRGRAW enabled. To be used in the dual path charging configuration 0 = The 5K pull down at CHRGRAW disabled
Reserved	20	R/W	RESETB	0	For future use
Reserved	21	R/W	RESETB	0	For future use
Unused	22	R/W	RESETB	0	Not available
Unused	23	R/W	RESETB	0	Not available

Table 6-2. Charge Path Regulator Current Limit Characteristics

Parameter	Value	Charge Current (in mA)[1]		
		Min[2]	Nom[3]	Max[2]
ICHRG[3:0]	0000	0	0	0
	0001	55	70	85
	0010	161	177	195
	0011	242	266	293
	0100	322	355	390
	0101	403	443	488
	0110	484	532	585
	0111	564	621	683
	1000	645	709	780
	1001	725	798	878
	1010	806	886	975
	1011	886	975	1073

Table 6-2. Charge Path Regulator Current Limit Characteristics (continued)

Parameter	Value	Charge Current (in mA)[1]		
		Min[2]	Nom[3]	Max[2]
	1100	967	1064	1170
	1101	1048	1152	1268
	1110	1450	1596	1755
	1111	Fully On—Disallow battery FET to be turned on in hardware		

1 The charge current is the current through the sense resistor.

2 The spread is 10% with respect to nominal except for code 0001.

3 The nominal value is a multiple of 88.65 mA except for code 0001.

Chapter 7
ADC Subsystem

7.1 Starting/Reading Conversion

7.1.1 Starting Conversion

To convert multiple channels, start the conversion with the ASC bit, the following steps are executed:

1. Enable A/D (ADEN = 1). Set RAND to 0, and select the group of channels via ADSEL.
2. Start conversion at channel 0 by writing a 1 to the start conversion bit (ASC). The conversion will begin once ATO counts down to zero.
3. Wait for completion. (ASC will reset to zero and ADCDONEI will be set when complete.)
4. Write the result address (ADA1[2:0] and ADA2[2:0]).
5. Read conversion values.
6. Repeat steps 4 and 5 for all channel results.

To convert multiple channels, start the conversion with the rising edge of ADTRIG, the following steps are executed:

1. Enable A/D (ADEN = 1). Set RAND to 0, and select the group of channels via ADSEL. Note that ASC will go high with the rising edge of ADTRIG.
2. The conversion will automatically start at channel 0 once ATO counts down to zero.
3. Wait for completion. (ASC will reset to zero and ADCDONEI will be set when complete.)
4. Write the result address (ADA1[2:0] and ADA2[2:0]).
5. Read conversion values.
6. Repeat steps 4 and 5 for all channel results.

To convert a single channel, start the conversion with the ASC bit, the following steps are executed:

1. Enable A/D (ADEN = 1). Set RAND to 1. Set ADA1[2:0] to the desired channel.
2. Start conversion by writing a 1 to the start conversion bit (ASC). The conversion will begin once ATO counts down to zero.
3. Wait for completion. (ASC will reset to zero and ADCDONEI will be set when complete.) In this mode the A/D will perform 8 conversions of the selected channel and save the results in ADA[2:0].
4. Write the conversion number 0-7 (ADA1[2:0] and ADA2[2:0]).
5. Read conversion values.
6. Repeat steps 4 and 5 for all 8 results.

To convert a single channel, start the conversion with the rising edge of ADTRIG, the following steps are executed:

1. Enable A/D (ADEN = 1). Set RAND to 1. Set ADA1[2:0] to the desired channel. Note that ASC will go high with the rising edge of ADTRIG.
2. The conversion will automatically start once ATO counts down to zero.
3. Wait for completion. (ASC will reset to zero and ADCDONEI will be set when complete.) In this mode the A/D will perform 8 conversions of the selected channel and save the results in ADA[2:0].
4. Write the conversion number 0-7 (ADA1[2:0] and ADA2[2:0]).
5. Read conversion values.
6. Repeat steps 4 and 5 for all 8 results.

The ADC completely ignores either the ADTRIG or ASC pulses while ADEN is low. When reading conversion results, it is therefore preferable to make ADEN = 0.

To avoid that the ADTRIG input involuntarily triggers a conversion, the ADTRIGIGN bit can be set which will ignore any transition on the ADTRIG pin.

7.1.2 Reading Conversions

Once a series of (8) A/D conversions is complete, they are stored in one set of 8 internal registers and the values can be read out by software. In order to accomplish this, software must set the ADA1 and ADA2 address bits to indicate which values will be read out. Two sets of addressing bits allow any two readings to be read out which are stored in the 8 internal registers. For example, if it is desired to read the conversion values stored in addresses 2 and 6, the software will need to set ADA1[2:0] to 010 and ADA2[2:0] to 110. Any SPI read of the A/D result register will return the values of the conversions indexed by ADA1[2:0] and ADA2[2:0]. The ADD1[9:0] will contain the value indexed by ADA1[2:0], where as ADD2[9:0] will contain the conversion value indexed by ADA2[2:0].

An additional feature allows for automatic incrementing of the ADA addressing bits. This involves bits ADINC1 and ADINC2. When these bits are set, the ADA1 and ADA2 addressing bits will automatically increment during subsequent readings of the A/D result register. This allows for rapid reading of the A/D results registers with a minimum of SPI transactions. As an example, the below sequence of events will convert and read out 8 channels via the SPI bus.

1. Write setting ADEN = 1, RAND = 0, ADSEL = 0, ADA1[2:0] = 000 (channel 0), ADA2[2:0] = 100 (channel 4). All other bits are zeros.
2. Write setting ASC = 1, ADINC1 = 1, ADINC2 = 1. All other bits are zero. The conversion will start after the ATO delay since ASC was set to 1.
3. Wait for the interrupt line to go high and read from the interrupt register to verify ADCDONEI is set.
4. Read from the result register. The channel 0 data is in bits ADD1[9:0], and the channel 4 data is in bits ADD2[9:0]. ADINC1 and ADINC2 will still be high. ASC will be zero.
5. Read from the result register. The channel 1 data is in bits ADD1[9:0], and the channel 5 data is in bits ADD2[9:0].

6. Read from the result register. The channel 2 data is in bits ADD1[9:0], and the channel 6 data is in bits ADD2[9:0].
7. Read from the result register. The channel 3 data is in bits ADD1[9:0], and the channel 7 data is in bits ADD2[9:0].

Any intermediate reading from the result register while waiting for the interrupt during step 3 will already increment the ADA addressing bits and should therefore be avoided.

7.2 ADC Arbitration

The ADC convertor and its control is based on a single ADC convertor core with the possibility to store two requests and their results. This feature can be set by programming the ADCSEL[1:0] SPI bits to 01. These bits are located in the "arbitration peripheral audio" register which is only accessible via the primary SPI. These bits are set at startup and are not to be reconfigured dynamically during phone operation.

Figure 7-1 depicts the ADC configuration as a function of the arbitration setting ADSEL[1:0].

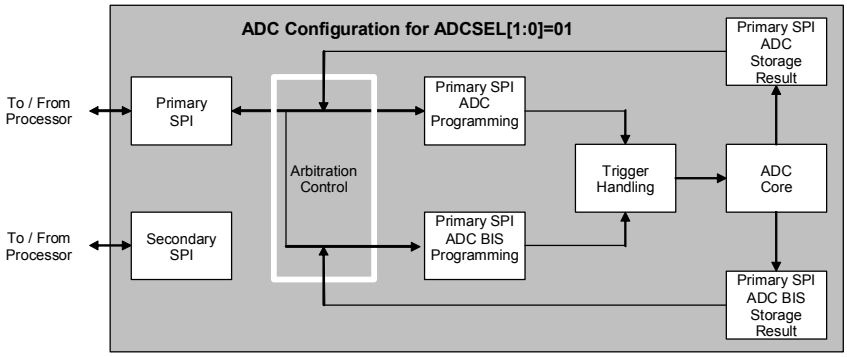

Figure 7-1. ADC Configurations

NOTE

Each of the ADC requests can be programmed for conversions of group 0 (channels 0-7, battery management related channels) or group 1 (channels 8-15, touchscreen and ambient light related channels).

In the case of single SPI access, the single SPI must have the ability to write to the two sets of ADC control, namely 'its own' ADC and 'the other' ADC or ADC BIS. The write access to the control of ADC BIS is handled via the ADCBISn bits located at bit position 23 of the ADC control registers. By setting this bit to a 1, the control bits which follow are destined for the ADC BIS. ADCBISn will always read back 0 and there is no read access to the ADCBIS control bits.

The read results from the ADC and ADC BIS conversions are available in two separate registers. This means that ADC software can be strictly identical independent if it runs via the primary or secondary SPI. It also means that in case of dual SPI control, the same result register address is used by both SPIs. In case of dual SPI control, so ADCSEL[1:0] = 00, the ADCBISn bit will have no function and are a don't care. Figure 7-2 schematically shows how the ADC control and result registers are set up.

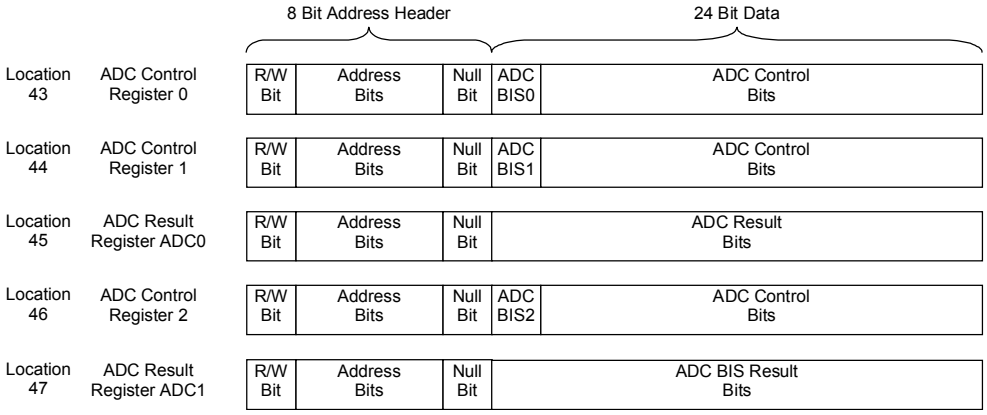

Figure 7-2. ADC Register Set for ADC BIS Access

There are two interrupts available to inform the processor when the ADC has finished its conversions. The ADCDONEI interrupt will go high after the conversion for ADC has finished, and ADCBISDONEI will go high after the conversion for ADC BIS has finished. Although both interrupts are available for both SPIs, only the interrupts to the SPI requesting the conversions are generated. This is depicted in Table 7-1. The interrupts can be masked.

There is only a single set of WHIGHI and WLOWI interrupt bits provided per SPI bus. This means that when queueing two ADC conversion requests on a single SPI, the WCOMP should only be used on the non BIS conversion requests.

When two requests are queued, the request for which the trigger event occurs the first will be converted the first. During the conversion of the first request, an ADTRIG trigger event of the other request is ignored if for the other request the TRIGMASK bit was set to 1. When this bit is set to 0, the other request ADTRIG trigger event is memorized, and the conversion will take place directly after the conversions of the first request are finished. It is not advised to use ADTRIG as a trigger event for two queued requests, this will lead to read out conflicts.

Figure 7-3 shows the influence of the TRIGMASK bit. The TRIGMASK bit is particularly of use when an ADC conversion has to be lined up to a periodically ADTRIG initiated conversion. In case of ASC initiated conversions, the TRIGMASK bit is of no influence.

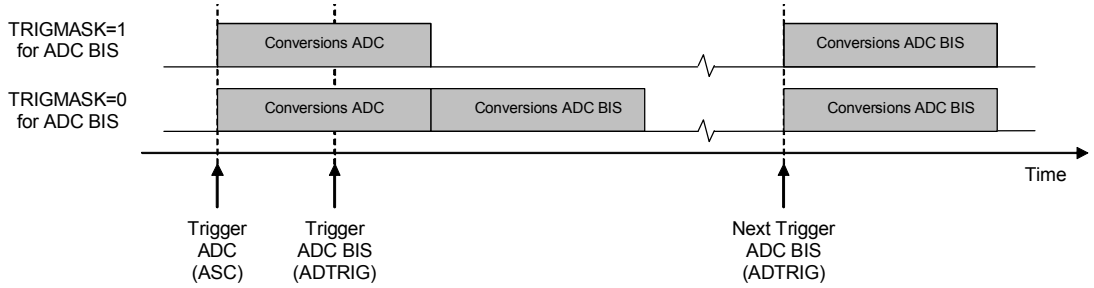

Figure 7-3. TRIGMASK Functional Diagram

To avoid that results of previous conversions get overwritten by a periodical ADTRIG signal, a single shot function is available which will make only a single set of conversions will be executed. The single shot function is enabled by setting the ADONESHOT bit to a one and in that case one and only one ADTRIG

trigger event is accepted. In order to perform a new single shot conversion, the ADONESHOT bit needs to be cleared followed by a dummy conversion. After the dummy conversion has finished, the ADC can again be reprogrammed for a single shot conversion via ADONESHOT.

NOTE

This bit is available for each of the conversion requests ADC or ADC BIS, so can be set independently.

One can distinguish 3 types of potential conflicting requests coming from the software when overwriting the current ADC control settings, so overwriting the same control bit locations. Conflicts could be avoided by a proper use of the interrupt mechanism. In below examples the programming occurs via the same SPI and for the same control bit locations with for example ADCBISn = 0.

Sequential Requests: The SPI has requested a conversion, the ADC starts the conversion, the ADC finishes, the SPI does a new request for a conversion. In this case the second request is executed and the results of the first request are overwritten. An ADCDONEI however was generated when the ADC finished the conversions of the first request.

Overlapping Requests: The SPI has requested a conversion, the ADC starts the conversion, the ADC is converting, the SPI does a new request for a conversion. In this case, writing to the SPI while the first ADC request is executed should be considered as a programming error since an ADCDONEI was yet not generated. Effectively, the contents of the SPI register get changed and therefore the behavior of the conversion which is ongoing.

Overruling Requests: The primary SPI has requested a conversion, the ADC did not start the conversion, the primary SPI does a new request for a conversion. In this case the first request does not get executed and only the second one. This could be the case for an ADTRIG based first request while the ADTRIG does not show up. Also in this case an ADCDONEI was not generated and an overruling request could therefore in practice become an overlapping request.

Table 7-1. Register 43, ADC 0

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
LICELLCON	0	R/W	RESETB	0	Enables lithium cell reading 0: ADC connected to ADC6 and not LICELL 1: ADC connected to LICELL and not ADIN6. Licell voltage readout calculation: 1 111 111 111 3.500 V 0 010 000 101 1.500 V 0 000 000 000 <1.200 V
CHRGICON	1	R/W	RESETB	0	Enables charge current reading 0: Charge current sense disabled 1: Charge current sense enabled Charger current readout calculation: 0 111 111 111 2.875A To battery 0 000 000 001 0.006A To battery 0 000 000 000 0A - 1 111 111 111 0.006A To charger 1 000 000 000 2.875A To charger

Table 7-1. Register 43, ADC 0 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
BATICON	2	R/W	RESETB	0	Enables battery current reading 0: Battery current sense disabled 1: Battery current sense enabled Charger current readout calculation: 0 111 111 111 2.875A From battery 0 000 000 001 0.006A From battery 0 000 000 000 0A - 1 111 111 111 0.006A To battery 1 000 000 000 2.875A To battery
RTHEN	3	R/W	RESETB	0	Enables thermistor reading 0: Disable the internal pull up current 1: Activate the internal pull up current to bias thermal resistor The reading of the thermistor value is optimized for a thermistor which changes -4.27% per degree according the formula 31.115 kOhm * 10^(-T/52.777) with T in °C. Typical values for the valid charging range are therefore 38 kOhm at -5 °C, 10 kOhm at +25 °C, and 2.2 kOhm at 60 °C.
DTHEN	4	R/W	RESETB	0	Enables die temperature reading 0: Disable die temperature sensor 1: Activate the die temperature sensor Die Temperature Read Out Code at 25 °C is 282 (decimal) Temperature change per LSB-1.14 °C
UIDEN	5	R/W	RESETB	0	Enables UID reading 0: Disable UID sensor 1: Enable UID sensor UID voltage readout calculation: 1 111 111 111 2.300 >2.555 0 000 000 000 0.000 0
ADOUTEN	6	R/W	RESETB	0	Enables the pulse at the ADOUT pin. See Figure 7-4 0: Disable pulse at ADOUT pin 1: Activate pulse at ADOUT pin
ADOUTPER	7	R/W	RESETB	0	Sets the ADOUT period. See Figure 7-4 0: The pulse will last for 4 conversions, 1: The pulse will last all conversions (8 conversions)
Reserved	8	R/W	RESETB	0	For future use
Reserved	9	R/W	RESETB	0	For future use
ADREFEN	10	R/W	RESETB	0	Enables the touchscreen reference 0: Disable ADREF touchscreen reference 1: Enable ADREF touchscreen reference
ADREFMODE	11	R/W	RESETB	0	Sets the touchscreen reference mode 0 = ADREF low power mode disabled 1 = ADREF low power mode enabled

Table 7-1. Register 43, ADC 0 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
TSMOD0	12	R/W	RESETB	0	Sets the touchscreen mode. See Table 7-2 for reading sequence 000: Inactive Mode - TSX1/TSX2/TSY1/TSY2 used as general purpose inputs. Input channels ADIN8-ADIN11 can be converted 001: Interrupt Mode - Generates an interrupt TSI when plates make contact. The ADEN bit does not need to be set to a 1 to enable this mode. TSI is dual edge sensitive and 30 ms debounced 010: Resistive Mode - Sequential reading of X and Y plate and contact resistance.Input channels ADIN8-ADIN11 are not converted 011: Position Mode - Sequential reading of X and Y coordinate pairs and contact resistance.Input channels ADIN8-ADIN11 are not converted 100: Inactive Mode - Same mode as for TSMOD[2:0]=000 101: Inactive Mode - Same mode as for TSMOD[2:0]=000 110: Inactive Mode - Same mode as for TSMOD[2:0]=000 111: Inactive Mode - Same mode as for TSMOD[2:0]=000
TSMOD1	13	R/W	RESETB	0	
TSMOD2	14	R/W	RESETB	0	
CHRGRAWDIV	15	R/W	RESETB	1	Sets CHRGRAW scaling to divide by 5 0: scaling factor is a divide by 10 1 111 111 111 23.000 1 101 111 001 20.000 0 000 000 000 0.000 (*) The max rating for CHRGRAW is 20 V 1: scaling factor is a divide by 5 1 111 111 111 11.500 1 101 111 001 10.000 0 000 000 000 0.000
ADINC1	16	R/W	RESETB	0	Auto increment for ADA1 0: Disable automatic incrementing of the ADA1 addressing bits 1: Enable automatic incrementing of the ADA1 addressing bits
ADINC2	17	R/W	RESETB	0	Auto increment for ADA2 0: Disable automatic incrementing of the ADA2 addressing bits 1: Enable automatic incrementing of the ADA2 addressing bits
WCOMP	18	R/W	RESETB	0	Normal conversion mode with limit comparison 0: Disable comparison mode 1: Enable comparison mode
Reserved	19	R/W	RESETB	0	For future use
Reserved	20	R/W	RESETB	0	For future use
Unused	21	R		0	Not available
Unused	22	R		0	Not available
ADCBIS0	23	W		0	Access to the ADCBIS control. See Chapter 7, “ADC Subsystem”. By setting to 1 this bit, the control bit of this register will be for the ADCBIS.

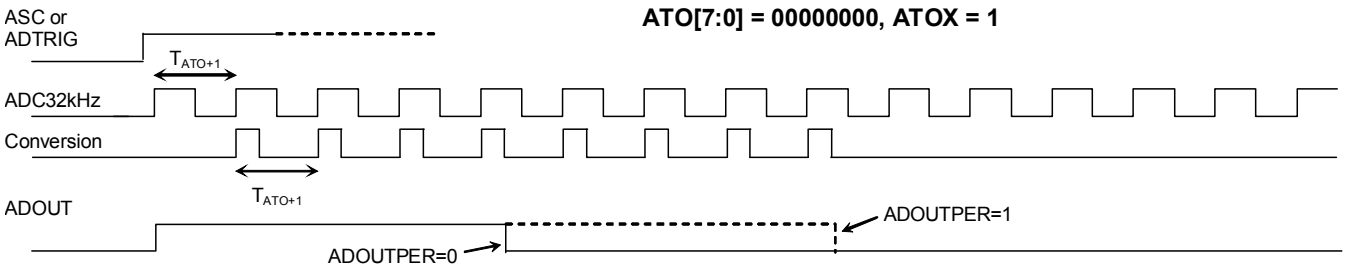

Figure 7-4. ADOUT Pulse Generator Behavior

Table 7-2. Touchscreen Reading Sequence

ADC Conversion	Signals Sampled in Resistive Mode	Signals Sampled in Position Mode	Readout Address[1]
0	X plate resistance	X position	000
1	X plate resistance	X position	001
2	X plate resistance	X position	010
3	Y plate resistance	Y position	011
4	Y plate resistance	Y position	100
5	Y plate resistance	Y position	101
6	Contact resistance	Contact resistance	110
7	Contact resistance	Contact resistance	111

1 Address as indicated by ADA1[2:0] and ADA2[2:0].

Table 7-3. Register 44, ADC 1

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
ADEN	0	R/W	RESETB	0	Enables the ADC 0: ADC is disabled 1: ADC is enabled
RAND	1	R/W	RESETB	0	Sets the single channel mode 0: the 8 channels will be converted one time 1: Same channel will be converted 8 times
Reserved	2	R/W	RESETB	0	For future use

Table 7-3. Register 44, ADC 1 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
ADSEL	3	R/W	RESETB	0	Selects the set of inputs 0: Group 0 is selected Battery Voltage Battery Current Application Supply (BP) Charger Voltage Charger Current ADIN5 or Battery Pack Thermistor ADIN6 or Backup Voltage (LICELL) ADIN7 or UID or Die Temperature 1: Group 0 is selected ADIN8 ADIN9 ADIN10 ADIN11 TSX1 or Touchscreen X-plate 1 TSX2 or Touchscreen X-plate 2 TSY1 or Touchscreen Y-plate 1 TSY2 or Touchscreen Y-plate 2
TRIGMASK	4	R/W	RESETB	0	Trigger event masking. See Chapter 7, “ADC Subsystem”. 0: The other request ADTRIG trigger event is memorized, and the conversion will take place directly after the conversions of the first request are finished. 1: During the conversion of the first request, an ADTRIG trigger event of the other request is ignored if for the other request the TRIGMASK bit was set to 1.
ADA10	5	R/W	RESETB	0	Channel selection 1 See Table 7-4
ADA11	6	R/W	RESETB	0	
ADA12	7	R/W	RESETB	0	
ADA20	8	R/W	RESETB	0	Channel selection 2 See Table 7-4
ADA21	9	R/W	RESETB	0	
ADA22	10	R/W	RESETB	0	
ATO0	11	R/W	RESETB	0	Delay before first conversion Programmable timer from 0 to 8 seconds (based on 32 kHz clock ~30.5 ms)
ATO1	12	R/W	RESETB	0	
ATO2	13	R/W	RESETB	0	
ATO3	14	R/W	RESETB	0	
ATO4	15	R/W	RESETB	0	
ATO5	16	R/W	RESETB	0	
ATO6	17	R/W	RESETB	0	
ATO7	18	R/W	RESETB	0	

Table 7-3. Register 44, ADC 1 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
ATOX	19	R/W	RESETB	0	Sets ATO delay for any conversion 0: ATO delay only before the fist conversion 1: ATO delay added before each conversion
ASC	20	R/W	RESETB	0	Starts conversion Put this bit to one to start conversion. Self clearing bit: ASC will reset to zero when complete conversions completed.
ADTRIGIGN	21	R/W	RESETB	0	Ignores the ADTRIG input 0: A rising edge transition of ADTRIG pin will trigger a conversion 1: Ignore any transition on the ADTRIG pin
ADONESHOT	22	R/W	RESETB	0	Single trigger event only 0: Disable oneshot function 1: Enable oneshot function. In that case one and only one ADTRIG trigger event is accepted
ADCBIS1	23	W	RESETB	0	Access to the ADCBIS control. See Chapter 7, “ADC Subsystem”. By setting to 1 this bit, the control bits of this register will be for the ADCBIS.

Table 7-4. ADC Inputs

	ADA	Signal Read
Group 0 – ADSEL = 0	0	Battery Voltage (BATT)
	1	Battery Current (BATT – BATTISNS)
	2	Application Supply (BP)
	3	Charger Voltage (CHRGRAW)
	4	Charger Current (CHRGISNSP-CHRGISNSN)
	5	General Purpose ADIN5 / Battery Pack Thermistor
	6	General Purpose ADIN6 / Backup Voltage (LICELL)
	7	General Purpose ADIN7 / UID / Die Temperature
Group 1 – ADSEL = 1	0	General Purpose ADIN8
	1	General Purpose ADIN9
	2	General Purpose ADIN10
	3	General Purpose ADIN11
	4	General Purpose TSX1 / Touchscreen X-plate 1
	5	General Purpose TSX2 / Touchscreen X-plate 2
	6	General Purpose TSY1 / Touchscreen Y-plate 1
	7	General Purpose TSY2 / Touchscreen Y-plate 2

Table 7-5. Register 45, ADC 2

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
Reserved	0	R	NONE	0	For future 12 bit use
Reserved	1	R	NONE	0	
ADD10	2	R	NONE	0	Results for channel selection 1
ADD11	3	R	NONE	0	
ADD12	4	R	NONE	0	
ADD13	5	R	NONE	0	
ADD14	6	R	NONE	0	
ADD15	7	R	NONE	0	
ADD16	8	R	NONE	0	
ADD17	9	R	NONE	0	
ADD18	10	R	NONE	0	
ADD19	11	R	NONE	0	
Reserved	12	R	NONE	0	For future use
Reserved	13	R	NONE	0	
ADD20	14	R	NONE	0	Results for channel selection 2
ADD21	15	R	NONE	0	
ADD22	16	R	NONE	0	
ADD23	17	R	NONE	0	
ADD24	18	R	NONE	0	
ADD25	19	R	NONE	0	
ADD26	20	R	NONE	0	
ADD27	21	R	NONE	0	
ADD28	22	R	NONE	0	
ADD29	23	R	NONE	0	

Table 7-6. Register 46, ADC 3

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
WHIGH0	0	R/W	RESETB	0	Comparator high level in WCOMP mode. A WHIGHI interrupt is generated for Vin > Vhigh. Note that the comparison is done by using only 6 MSB. For proper use, WLOW[5:0] < WHIGH[5:0].
WHIGH1	1	R/W	RESETB	0	
WHIGH2	2	R/W	RESETB	0	
WHIGH3	3	R/W	RESETB	0	
WHIGH4	4	R/W	RESETB	0	
WHIGH5	5	R/W	RESETB	0	
ICID0	6	R/W	NONE	0	MC13783 derivative
ICID1	7	R/W	NONE	1	
ICID2	8	R/W	NONE	0	
WLOW0	9	R/W	RESETB	0	Comparator low level in WCOMP mode. A WLOWI interrupt is generated for Vin < Vhigh. Note that the comparison is done by using only 6 MSB. For proper use, WLOW[5:0] < WHIGH[5:0].
WLOW1	10	R/W	RESETB	0	
WLOW2	11	R/W	RESETB	0	
WLOW3	12	R/W	RESETB	0	
WLOW4	13	R/W	RESETB	0	
WLOW5	14	R/W	RESETB	0	
Unused	15	R		0	Not available
Unused	16	R		0	Not available
Unused	17	R		0	Not available
Unused	18	R		0	Not available
Unused	19	R		0	Not available
Unused	20	R		0	Not available
Unused	21	R		0	Not available
Unused	22	R		0	Not available
ADCBIS2	23	W	RESETB	0	Access to the ADCBIS control. See Chapter 7, “ADC Subsystem”. By setting to 1 this bit, the control bits of this register will be for the ADCBIS.

Table 7-7. Register 47, ADC 4

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
Reserved	0	R	NONE	0	For future 12 bit use
Reserved	1	R	NONE	0	

Table 7-7. Register 47, ADC 4 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
ADDBIS10	2	R	NONE	0	Result for channel selection 1 of ADCBIS
ADDBIS11	3	R	NONE	0	
ADDBIS12	4	R	NONE	0	
ADDBIS13	5	R	NONE	0	
ADDBIS14	6	R	NONE	0	
ADDBIS15	7	R	NONE	0	
ADDBIS16	8	R	NONE	0	
ADDBIS17	9	R	NONE	0	
ADDBIS18	10	R	NONE	0	
ADDBIS19	11	R	NONE	0	
Reserved	12	R	NONE	0	For future use
Reserved	13	R	NONE	0	
ADDBIS20	14	R	NONE	0	Result for channel selection 2 of ADCBIS
ADDBIS21	15	R	NONE	0	
ADDBIS22	16	R	NONE	0	
ADDBIS23	17	R	NONE	0	
ADDBIS24	18	R	NONE	0	
ADDBIS25	19	R	NONE	0	
ADDBIS26	20	R	NONE	0	
ADDBIS27	21	R	NONE	0	
ADDBIS28	22	R	NONE	0	
ADDBIS29	23	R	NONE	0	

Chapter 8
Connectivity

Table 8-1. Register 49, USB 0

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
FSENB	0	R/W	RESETB	0	USB full speed mode select bar 0: USB full speed mode selected 1: USB low speed mode selected
USBSUSPEND	1	R/W	RESETB	0	USB suspend mode enable 0: USB Suspend mode disabled 1: USB Suspend mode enabled
USBPU	2	R/W	RESETB	0	Switches in variable 1.5K UDP/UDM pull-up 1: Variable 1.5K pull-up switched in 0: Variable 1.5K pull-up switched out
UDPPD	3	R/W	RESETB	0	Switches in 15K UDP pull-down 0: 15K UDP pull-down switched out 1: 15K UDP pull-down switched in
UDMPD	4	R/W	RESETB	0	Switches in 15K UDM pull-down 0: 15K UDM pull-down switched out 1: 15K UDM pull-down switched in
DP150KPU	5	R/W	RESETB	1	Switches in 150K UDP pull-up 0: 150K UDP pull-up switched out 1: 150K UDP pull-up switched in
VBUS70KPDENB	6	R/W	RESETB	1	Turns off VBUS pull-down NMOS switch 0: VBUS pull-down NMOS switch is ON if VBUSEN=0, OFF otherwise 1: VBUS pull-down NMOS switch is OFF
VBUSPULSETMR0	7	R/W	RESETB	0	VBUS regulator current limit control 000: current limit set to 200 mA 001: current limit set to 910 uA for 10 msec 010: current limit set to 910 uA for 20 msec 011: current limit set to 910 uA for 30 msec 100: current limit set to 910 uA for 40 msec 101: current limit set to 910 uA for 50 msec 110: current limit set to 910 uA for 60 msec 111: current limit set to 910 uA The 010 to 110 settings are self clearing at end of timer
VBUSPULSETMR1	8	R/W	RESETB	0	
VBUSPULSETMR2	9	R/W	RESETB	0	
DLPSRP	10	R/W	RESETB	0	DLP Timer enable 0: DLP Timer disabled 1: DLP Timer enabled, self clearing at end of pulse

Table 8-1. Register 49, USB 0 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
SE0CONN	11	R/W	RESETB	0	SE0 automatically connects UDP pull-up 0: variable UDP pull-up is not automatically connected when SE0 is detected 1: variable UDP pull-up is automatically connected when SE0 is detected
USBXCVREN	12	R/W	RESETB	0	USB transceiver enable 0: USB transceiver disabled if USBEN is low or if USBCNTRL = 0 1: USB transceiver enabled if CONMODE[2:0] = 000 and RESETB is high
PULLOVR	13	R/W	RESETB	0	Variable pull-up / pull-downs disconnect 0: variable 1k5 pull-up and UDP/UDM pull-downs are connected when UTXENB is active low 1: variable 1k5 pull-up and UDP/UDM pull-downs are disconnected when UTXENB is active low
CONMODE0	14	R/W	RESETB	0	Connectivity Interface mode select: 000: USB mode 001: RS232 mode 1 010: RS232 mode 2 011: reserved 100: mono audio mode 101: stereo audio mode 110: Test mode right mode 111: Test mode left mode
CONMODE1	15	R/W	RESETB	0	
CONMODE2	16	R/W	RESETB	0	
DATSE0	17	R/W	NONE	*	USB single ended / differential mode 0: Differential USB mode 1: Single ended USB mode
BIDIR	18	R/W	NONE	*	USB unidirectional / bidirectional transmission 0: unidirectional USB transmission 1: bidirectional USB transmission
USBCNTRL	19	R/W	RESETB	1	USB transceiver and pull-up control 0: USB mode of operation controlled by SPI 1: USB mode of operation controlled by USBEN pin
IDPD	20	R/W	RESETB	0	Switches in UID pull-down 0: UID pull-down switched out 1: UID pull-down switched in
IDPULSE	21	R/W	RESETB	0	Pulses UID to ground 0: UID line not pulsed 1: pulse to gnd on the UID line generated This bit is a self clearing bit and will always read back 0

Table 8-1. Register 49, USB 0 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
IDPUCNTRL	22	R/W	RESETB	0	UID pin pull up source select 0: UID pin pulled high through 220K resistor 1: UID pin pulled high by 5uA current source
DMPULSE	23	R/W	RESETB	0	Generates positive pulse on the UDM line 0: UDM line not pulsed 1: A positive pulse on the UDM line is generated. This bit is a self clearing bit and will always read back 0

Table 8-2. Register 50, Charger USB 1

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
VUSBIN0	0	R/W	RESETB	0	VUSB regulator input source control Controls the input source for the VUSB regulator. The default input is BP. 00:input = Boost via VINBUS, default in boot mode 01:input = VBUS 10:input = BP (VINVIB), default in non boot modes 11:input = VBUS
VUSBIN1	1	R/W	RESETB	1	
VUSB	2	R/W	RESETB	1	VUSB output voltage setting 0: VUSB output voltage set to 3.2 V 1: VUSB output voltage set to 3.3 V
VUSBEN	3	R/W	NONE	*	VUSB enable 0: VUSB output is disabled (unless USBEN pin is asserted high) 1: VUSB output is enabled (regardless of USBEN pin)
Reserved	4	R/W	RESETB	0	For future use
VBUSEN	5	R/W	NONE	*	VBUS enable 0: VBUS output is disabled (unless VBUSPULSETMR[2:0] <> 0) 1: VBUS output is enabled (regardless of VBUSPULSETMR[2:0])
RSPOL	6	R/W	RESETB	0	Swaps TX and RX in RS232 mode 0: RS232 TX on UDM, RX on UDP 1: RS232 TX on UDP, RX on UDM
RSTRI	7	R/W	RESETB	0	Tristates TX in RS232 mode 0: No effect 1: TX forced to Tristate in RS232 mode only
ID100KPU	8	R/W	RESETB	0	Switches in 100K UID pull-up 0: 100K UID pull up resistor not switched in 1: 100K UID pull up resistor switched in
Unused	9	R		0	Not used
Unused	10	R		0	Not used
Unused	11	R		0	Not used

Table 8-2. Register 50, Charger USB 1 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
Unused	12	R		0	Not used
Unused	13	R		0	Not used
Unused	14	R		0	Not used
Unused	15	R		0	Not used
Unused	16	R		0	Not used
Unused	17	R		0	Not used
Unused	18	R		0	Not used
Unused	19	R		0	Not used
Unused	20	R		0	Not used
Unused	21	R		0	Not used
Unused	22	R		0	Not used
Unused	23	R		0	Not used

Chapter 9
Lighting System

9.1 SPI Control for Ramp Modes

Due to the computational requirements of the flexible ramping scheme, special timing considerations should be adhered to for ramp-associated SPI writes. For ramp up initiation on any of the backlight or tri-color driver channels, the ramp up request should first be issued via SPI (LED Control Register 0 for Backlight drivers, LED Control 1 for TC drivers). This request is latched by the system, which awaits the ending PWM setting so the algorithm can interpolate a smooth PWM sweep. The ending PWM duty cycle that is intended for the ramped driver to settle at after the ramp should be sent with a second SPI write within 30 us of the ramp up SPI command. The control logic will allow only a single ramp up cycle even if a given channel's RAMPUP bit is not manually cleared. A manual clear should be done if a subsequent ramp cycle is desired.

By way of example, following is a sample SPI sequence to initiate ramping up on the key pad driver.

Example for keypad backlight ramp up; SLEWLIM disabled, ending PWM is 10/15, final KP current level is set for 60 mA.

1. Write to Register 51 for master enable of the LED drivers (enables core bias circuitry) and the Ramp Up enable on KP: MSB(.....000.100.1)LSB. Note that Ramp Up and Ramp Down bits should not be simultaneously activated.
2. Within 30 us, write to Register 53 to program the ending PWM duty cycle that is desired after completion of the ramp: MSB (0.00.1010. ....101.000.000) LSB. KP is set to ending duty cycle of 10/15; bits related to KP duty rate should remain the same during the ramp-up (500 ms) and after. Current level is set for 60 mA.

For Ramp down initiation on any of the backlight or tri-color driver channels, a given lighting zone will already be programmed to its starting point PWM, so the SPI write to enable the ramp down is all that is needed to initiate the sequence, i.e., the algorithm already has the necessary information to calculate the appropriate step sizes since the starting point duty cycle is pre-programmed, and it will ramp down to 0% duty cycle. There are still timing considerations to be respected as indicated in the following example.

Example for Keypad Backlight Ramp Down; Register 53 contains the initial PWM settings: MSB (0.00.1111. ....101.000.000) LSB, SLEWLIM disabled, Starting PWM is 15/15, KP Current Level is set for 60 mA.

1. Write to Register 51 to enable Ramp Down on KP: MSB (.....100.000.1) LSB. KP Ramp Down is requested. Note that Ramp Up and Ramp Down bits should not be simultaneously activated.
2. Wait 100 us to 500 ms; SPI can do other transactions during this period.
3. Write to Register 53 to set ending PWM settings: MSB (0.00.0000. ....000.000.000) LSB.

Bits related to the KP duty rate in Register 53 should remain the same during for ~100 us after the Ramp Down command is sent, but should be changed to PWM of 0/15 before the Ramp Down is completed (500ms). This assures that the backlight will ramp down and stay off at the end of the ramp.

9.2 SPI Bits

Table 9-1. Register 51, LED Control 0

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
LEDEN	0	R/W	RESETB	0	Master Enable for BL and TC LED Bias 0: Disable BL/TC LED bias 1: Enable BL/TC LED bias
LEDMDRAMPUP	1	R/W	RESETB	0	Ramp Up Main Display Backlight channel 0: Disable ramp up of main display backlight 1: Enable ramp up of main display backlight
LEDADRAMPUP	2	R/W	RESETB	0	Ramp Up Auxiliary Display Backlight channel 0: Disable ramp up of auxiliary display backlight 1: Enable ramp up of auxiliary display backlight
LEDKPRAMPUP	3	R/W	RESETB	0	Ramp Up Key Pad Backlight channel 0: Disable ramp up of keypad backlight 1: Enable ramp up of keypad backlight
LEDMDRAMPDOWN	4	R/W	RESETB	0	Ramp Down Main Display Backlight channel 0: Disable ramp down of main display backlight 1: Enable ramp down of main display backlight
LEDADRAMPDOWN	5	R/W	RESETB	0	Ramp Down Auxiliary Display Backlight channel 0: Disable ramp down of auxiliary display backlight 1: Enable ramp down of auxiliary display backlight
LEDKPRAMPDOWN	6	R/W	RESETB	0	Ramp Down Key Pad Backlight channel 0: Disable ramp down of keypad backlight 1: Enable ramp down of keypad backlight
TRIODEMD	7	R/W	RESETB	0	Triode Mode for Main Display Backlight Drivers 0: Disable triode mode for main display backlight drivers 1: Enable triode mode for main display backlight drivers
TRIODEAD	8	R/W	RESETB	0	Triode Mode for Auxiliary Display Backlight Drivers 0: Disable triode mode for auxiliary display backlight drivers 1: Enable triode mode for auxiliary display backlight drivers
TRIODEKP	9	R/W	RESETB	0	Triode Mode for Key Pad Backlight Driver 0: Disable triode mode for key pad backlight driver 1: Disable triode mode for key pad backlight driver
BOOSTEN	10	R/W	RESETB	0	Forced Enable for Boost 0: Sate of the SW3 defined by sw3 SPI control bits located in register 29 1: Force SW3 to be ON independently of the state of the SPI control bits of SW3 located in register 29

Table 9-1. Register 51, LED Control 0 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
ABMODE0	11	R/W	RESETB	0	Adaptive Boost Mode Selection Bits 000: Adaptive Boost Disabled 001: Monitor Channel LEDMD1 010: Monitor Channels LEDMD1,2 011: Monitor Channels LEDMD1,2,3 100: Monitor Channels LEDMD1,2,3,4 101: Monitor Channels LEDMD1,2,3,4 and LEDAD1 110: Monitor Channels LEDMD1,2,3,4 and LEDAD1,2 111: Monitor Channel LEDMD1 with LEDAD active
ABMODE1	12	R/W	RESETB	0	
ABMODE2	13	R/W	RESETB	0	
ABREF0	14	R/W	RESETB	0	Adaptive Boost reference level to set driver headroom voltage 00: ABREF = 200 mV 01: ABREF = 400 mV 10: ABREF = 600 mV 11: ABREF = 800 mV
ABREF1	15	R/W	RESETB	0	
Reserved	16	R/W	RESETB	0	Reserved for future use by the adaptive boost
FLPATTRN0	17	R/W	RESETB	0	Fun Light Pattern Selection Bits See Table 9-2
FLPATTRN1	18	R/W	RESETB	0	
FLPATTRN2	19	R/W	RESETB	0	
FLPATTRN3	20	R/W	RESETB	0	
FLBANK1	21	R/W	RESETB	0	Tri-Color Bank 1 Activation for Fun Light Pattern 0: Tri-color bank 1 fun light pattern in progress is stopped 1: Latches selected fun light pattern and activates it on tri-color bank 1
FLBANK2	22	R/W	RESETB	0	Tri-Color Bank 2 Activation for Fun Light Pattern 0: Tri-color bank 2 fun light pattern in progress is stopped 1: Latches selected fun light pattern and activates it on tri-color bank 2
FLBANK3	23	R/W	RESETB	0	Tri-Color Bank 3 Activation for Fun Light Pattern 0: Tri-color bank 3 fun light pattern in progress is stopped 1: Latches selected fun light pattern and activates it on tri-color bank 3

Table 9-2. Fun Light Pattern Decoding Map

FLPATTRN[3:0]				Fun Light Pattern	Pattern Description
3	2	1	0		
0	0	0	0	Blended_Ramps_Slow	Cycles LEDR, LEDG, and LEDB through overlapping Ramp Up / Ramp Down cycles with 1 second ramp rates
0	0	0	1	Blended_Ramps_Fast	Cycles LEDR, LEDG, and LEDB through overlapping Ramp Up / Ramp Down cycles with 400 ms ramp rates
0	0	1	0	Saw_Ramps_Slow	Cycles LEDR, LEDG, and LEDB through non-overlapping Ramp Up cycles with 1 second ramp rates

Table 9-2. Fun Light Pattern Decoding Map (continued)

FLPATTRN[3:0]				Fun Light Pattern	Pattern Description
3	2	1	0		
0	0	1	1	Saw_Ramps_Fast	Cycles LEDR, LEDG, and LEDB through non-overlapping Ramp Up cycles with 400 ms ramp rates
0	1	0	0	Blended_Inverse_Ramps_slow	Cycles LEDR, LEDG, and LEDB through overlapping Ramp Down / Ramp Up cycles with 1 second ramp rates
0	1	0	1	Blended_ Inverse Ramps_FAST	Cycles LEDR, LEDG, and LEDB through overlapping Ramp Up / Ramp Down cycles with 400 ms ramp rates
0	1	1	0	Chasing_Lights_RGB_Slow	Cycles each Tri-Color channel in RGB sequence for 500 ms on, 1000 ms off. Each channel is set to the programmed current levels and duty cycles when cycled on.
0	1	1	1	Chasing_Lights_RGB_Fast	Cycles each Tri-Color channel in RGB sequence for 200 ms on, 400 ms off. Each channel is set to the programmed current levels and duty cycles when cycled on.
1	0	0	0	Chasing_Lights_BGR_Slow	Cycles each Tri-Color channel in BGR sequence for 500 ms on, 1000 ms off. Each channel is set to the programmed current levels and duty cycles when cycled on.
1	0	0	1	Chasing_Lights_BGR_Fast	Cycles each Tri-Color channel in BGR sequence for 200 ms on, 400 ms off. Each channel is set to the programmed current levels and duty cycles when cycled on.
1	0	1	0	Unassigned	
1	0	1	1	Unassigned	
1	1	0	0	Unassigned	
1	1	0	1	Unassigned	
1	1	1	0	Unassigned	
1	1	1	1	Unassigned	

Table 9-3. Register 52, LED Control 1

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
LEDR1RAMPUP	0	R/W	RESETB	0	Ramp Up Tri-Color 1 Red Channel 0: Disable ramp-up control of LEDR1 1: Enable ramp-up control of LEDR1
LEDG1RAMPUP	1	R/W	RESETB	0	Ramp Up Tri-Color 1 Green Channel 0: Disable ramp-up control of LEDG1 1: Enable ramp-up control of LEDG1
LEDB1RAMPUP	2	R/W	RESETB	0	Ramp Up Tri-Color 1 Blue Channel 0: Disable ramp-up control of LEDB1 1: Enable ramp-up control of LEDB1 See SPI Control for Ramp Modes chapter

Table 9-3. Register 52, LED Control 1 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
LEDR1RAMPDOWN	3	R/W	RESETB	0	Ramp Down Tri-Color 1 Red Channel 0: Disable ramp-down control of LEDR1 1: Enable ramp-down control of LEDR1 See SPI Control for Ramp Modes chapter
LEDG1RAMPDOWN	4	R/W	RESETB	0	Ramp Down Tri-Color 1 Green Channel 0: Disable ramp-down control of LEDG1 1: Enable ramp-down control of LEDG1 See SPI Control for Ramp Modes chapter
LEDB1RAMPDOWN	5	R/W	RESETB	0	Ramp Down Tri-Color 1 Blue Channel 0: Disable ramp-down control of LEDB1 1: Enable ramp-down control of LEDB1 See SPI Control for Ramp Modes chapter
LEDR2RAMPUP	6	R/W	RESETB	0	Ramp Up Tri-Color 2 Red Channel 0: Disable ramp-up control of LEDR2 1: Enable ramp-up control of LEDR2 See SPI Control for Ramp Modes chapter
LEDG2RAMPUP	7	R/W	RESETB	0	Ramp Up Tri-Color 2 Green Channel 0: Disable ramp-up control of LEDG2 1: Enable ramp-up control of LEDG2 See SPI Control for Ramp Modes chapter
LEDB2RAMPUP	8	R/W	RESETB	0	Ramp Up Tri-Color 2 Blue Channel 0: Disable ramp-up control of LEDB2 1: Enable ramp-up control of LEDB2 See SPI Control for Ramp Modes chapter
LEDR2RAMPDOWN	9	R/W	RESETB	0	Ramp Down Tri-Color 2 Red Channel 0: Disable ramp-down control of LEDR2 1: Enable ramp-down control of LEDR2 See SPI Control for Ramp Modes chapter
LEDG2RAMPDOWN	10	R/W	RESETB	0	Ramp Down Tri-Color 2 Green Channel 0: Disable ramp-down control of LEDG2 1: Enable ramp-down control of LEDG2 See SPI Control for Ramp Modes chapter
LEDB2RAMPDOWN	11	R/W	RESETB	0	Ramp Down Tri-Color 2 Blue Channel 0: Disable ramp-down control of LEDB2 1: Enable ramp-down control of LEDB2 See SPI Control for Ramp Modes chapter
LEDR3RAMPUP	12	R/W	RESETB	0	Ramp Up Tri-Color 3 Red Channel 0: Disable ramp-up control of LEDR3 1: Enable ramp-up control of LEDR3 See SPI Control for Ramp Modes chapter
LEDG3RAMPUP	13	R/W	RESETB	0	Ramp Up Tri-Color 3 Green Channel 0: Disable ramp-up control of LEDG3 1: Enable ramp-up control of LEDG3 See SPI Control for Ramp Modes chapter

Table 9-3. Register 52, LED Control 1 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
LEDB3RAMPUP	14	R/W	RESETB	0	Ramp Up Tri-Color 3 Blue Channel 0: Disable ramp-up control of LEDB3 1: Enable ramp-up control of LEDB3 See SPI Control for Ramp Modes chapter
LEDR3RAMPDOWN	15	R/W	RESETB	0	Ramp Down Tri-Color 3 Red Channel 0: Disable ramp-down control of LEDR3 1: Enable ramp-down control of LEDR3 See SPI Control for Ramp Modes chapter
LEDG3RAMPDOWN	16	R/W	RESETB	0	Ramp Down Tri-Color 3 Green Channel 0: Disable ramp-down control of LEDG3 1: Enable ramp-down control of LEDG3 See SPI Control for Ramp Modes chapter
LEDB3RAMPDOWN	17	R/W	RESETB	0	Ramp Down Tri-Color 3 Blue Channel 0: Disable ramp-down control of LEDB3 1: Enable ramp-down control of LEDB3 See SPI Control for Ramp Modes chapter
TC1HALF	18	R/W	RESETB	0	Half Current Mode for Tri-Color 1 Driver Channels 0: Full current activated 1: Half current activated
Reserved	19	R/W	RESETB	0	Reserved
Reserved	20	R/W	RESETB	0	Reserved
Reserved	21	R/W	RESETB	0	Reserved
Reserved	22	R/W	RESETB	0	Reserved
SLEWLIMTC	23	R/W	RESETB	0	Master Enable for Tri-Color Analog Edge Slowing 0: Disable analog slow analog edge 1: Activate analog slow analog edge

Table 9-4. Register 53, LED Control 2

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
LEDMD0	0	R/W	RESETB	0	Current Level Programming for the Main Display Backlight Driver 000: 0 mA 001: 3 mA 010: 6 mA 011: 9 mA 100: 12 mA 101: 15 mA 110: 18 mA 111: 21 mA
LEDMD1	1	R/W	RESETB	0	
LEDMD2	2	R/W	RESETB	0	

Table 9-4. Register 53, LED Control 2 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
LEDAD0	3	R/W	RESETB	0	Current Level Programming for the Auxiliary Display Backlight Driver 000: 0 mA 001: 3 mA 010: 6 mA 011: 9 mA 100: 12 mA 101: 15 mA 110: 18 mA 111: 21 mA
LEDAD1	4	R/W	RESETB	0	
LEDAD2	5	R/W	RESETB	0	
LEDKP0	6	R/W	RESETB	0	Current Level Programming for the Keypad Backlight Driver 000: 0 mA 001: 12 mA 010: 24 mA 011: 36 mA 100: 48 mA 101: 60 mA 110: 72 mA 111: 84 mA
LEDKP1	7	R/W	RESETB	0	
LEDKP2	8	R/W	RESETB	0	
LEDMDDC0	9	R/W	RESETB	0	Duty Cycle Control for the Main Display Backlight Driver From 0/15 (code 0000) to 15/15 (code 1111) with 1/15 steps
LEDMDDC1	10	R/W	RESETB	0	
LEDMDDC2	11	R/W	RESETB	0	
LEDMDDC3	12	R/W	RESETB	0	
LEDADDC0	13	R/W	RESETB	0	Duty Cycle Control for the Auxiliary Display Backlight Driver From 0/15 (code 0000) to 15/15 (code 1111) with 1/15 steps
LEDADDC1	14	R/W	RESETB	0	
LEDADDC2	15	R/W	RESETB	0	
LEDADDC3	16	R/W	RESETB	0	
LEDKPDC0	17	R/W	RESETB	0	Duty Cycle Control for the Keypad Backlight Driver From 0/15 (code 0000) to 15/15 (code 1111) with 1/15 steps
LEDKPDC1	18	R/W	RESETB	0	
LEDKPDC2	19	R/W	RESETB	0	
LEDKPDC3	20	R/W	RESETB	0	
BLPERIOD0	21	R/W	RESETB	0	Period Control for Backlight 00: 0.01 seconds 01: 0.1 seconds 10: 0.5 seconds 11: 2 seconds
BLPERIOD1	22	R/W	RESETB	0	
SLEWLIMBL	23	R/W	RESETB	0	Master Enable for Backlight Analog Edge Slowing 0: Disable analog slow analog edge 1: Activate analog slow analog edge

Table 9-5. Register 54, LED Control 3

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
LEDR10	0	R/W	RESETB	0	Current Level Programming for the Red channel of Tri-Color Bank 1 If TC1HALF = 0 00: 12 mA 01: 18 mA 10: 30 mA 11: 42 mA If TC1HALF = 1 00: 6 mA 01: 9 mA 10: 15 mA 11: 21 mA
LEDR11	1	R/W	RESETB	0	
LEDG10	2	R/W	RESETB	0	Current Level Programming for the Green channel of Tri-Color Bank 1 00: 12 mA 01: 18 mA 10: 30 mA 11: 42 mA If TC1HALF = 1 00: 6 mA 01: 9 mA 10: 15 mA 11: 21 mA
LEDG11	3	R/W	RESETB	0	
LEDB10	4	R/W	RESETB	0	Current Level Programming for the Blue channel of Tri-Color Bank 1 00: 12 mA 01: 18 mA 10: 30 mA 11: 42 mA If TC1HALF = 1 00: 6 mA 01: 9 mA 10: 15 mA 11: 21 mA
LEDB11	5	R/W	RESETB	0	
LEDR1DC0	6	R/W	RESETB	0	Duty Cycle Control for the Red channel of Tri-Color Bank 1 From 0/31 (code 00000) to 31/31 (code 01111) with 1/31 steps
LEDR1DC1	7	R/W	RESETB	0	
LEDR1DC2	8	R/W	RESETB	0	
LEDR1DC3	9	R/W	RESETB	0	
LEDR1DC4	10	R/W	RESETB	0	

Table 9-5. Register 54, LED Control 3 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
LEDG1DC0	11	R/W	RESETB	0	Duty Cycle Control for the Green channel of Tri-Color Bank 1 From 0/31 (code 00000) to 31/31 (code 01111) with 1/31 steps
LEDG1DC1	12	R/W	RESETB	0	
LEDG1DC2	13	R/W	RESETB	0	
LEDG1DC3	14	R/W	RESETB	0	
LEDG1DC4	15	R/W	RESETB	0	
LEDB1DC0	16	R/W	RESETB	0	Duty Cycle Control for the Blue channel of Tri-Color Bank 1 From 0/31 (code 00000) to 31/31 (code 01111) with 1/31 steps
LEDB1DC1	17	R/W	RESETB	0	
LEDB1DC2	18	R/W	RESETB	0	
LEDB1DC3	19	R/W	RESETB	0	
LEDB1DC4	20	R/W	RESETB	0	
TC1PERIOD0	21	R/W	RESETB	0	Period Control for Tri-Color Bank 1 00: 0.01 seconds 01: 0.1 seconds 10: 0.5 seconds 11: 2 seconds
TC1PERIOD1	22	R/W	RESETB	0	
TC1TRIODE	23	R/W	RESETB	0	Triode Mode for Tri-Color Bank 1 Channels 0: Disable triode mode for tri-color bank 1 channels 1: Enable triode mode for tri-color bank 1 channels

Table 9-6. Register 55, LED Control 4

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
LEDR20	0	R/W	RESETB	0	Current Level Programming for the Red channel of Tri-Color Bank 2 00: 6 mA 01: 9 mA 10: 15 mA 11: 21 mA
LEDR21	1	R/W	RESETB	0	
LEDG20	2	R/W	RESETB	0	Current Level Programming for the Green channel of Tri-Color Bank 2 00: 6 mA 01: 9 mA 10: 15 mA 11: 21 mA
LEDG21	3	R/W	RESETB	0	
LEDB20	4	R/W	RESETB	0	Current Level Programming for the Blue channel of Tri-Color Bank 2 00: 6 mA 01: 9 mA 10: 15 mA 11: 21 mA
LEDB21	5	R/W	RESETB	0	

Table 9-6. Register 55, LED Control 4 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
LEDR2DC0	6	R/W	RESETB	0	Duty Cycle Control for the Red channel of Tri-Color Bank 2 From 0/31 (code 00000) to 31/31 (code 01111) with 1/31 steps
LEDR2DC1	7	R/W	RESETB	0	
LEDR2DC2	8	R/W	RESETB	0	
LEDR2DC3	9	R/W	RESETB	0	
LEDR2DC4	10	R/W	RESETB	0	
LEDG2DC0	11	R/W	RESETB	0	Duty Cycle Control for the Green channel of Tri-Color Bank 2 From 0/31 (code 00000) to 31/31 (code 01111) with 1/31 steps
LEDG2DC1	12	R/W	RESETB	0	
LEDG2DC2	13	R/W	RESETB	0	
LEDG2DC3	14	R/W	RESETB	0	
LEDG2DC4	15	R/W	RESETB	0	
LEDB2DC0	16	R/W	RESETB	0	Duty Cycle Control for the Blue channel of Tri-Color Bank 2 From 0/31 (code 00000) to 31/31 (code 01111) with 1/31 steps
LEDB2DC1	17	R/W	RESETB	0	
LEDB2DC2	18	R/W	RESETB	0	
LEDB2DC3	19	R/W	RESETB	0	
LEDB2DC4	20	R/W	RESETB	0	
TC2PERIOD0	21	R/W	RESETB	0	Period Control for Tri-Color Bank 2 00: 0.01 seconds 01: 0.1 seconds 10: 0.5 seconds 11: 2 seconds
TC2PERIOD1	22	R/W	RESETB	0	
TC2TRIODE	23	R/W	RESETB	0	Triode Mode for Tri-Color Bank 2 Channels 0: Disable triode mode for tri-color bank 2 channels 1: Enable triode mode for tri-color bank 2 channels

Table 9-7. Register 56, LED Control 5

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
LEDR30	0	R/W	RESETB	0	Current Level Programming for the Red Channel of Tri-Color Bank 3 00: 6 mA 01: 9 mA 10: 15 mA 11: 21 mA
LEDR31	1	R/W	RESETB	0	
LEDG30	2	R/W	RESETB	0	Current Level Programming for the Green Channel of Tri-Color Bank 3 00: 6 mA 01: 9 mA 10: 15 mA 11: 21 mA
LEDG31	3	R/W	RESETB	0	

Table 9-7. Register 56, LED Control 5 (continued)

Name	Bit #	R/W	Reset	Default	Description Vector Bits are MSB First
LEDB30	4	R/W	RESETB	0	Current Level Programming for the Blue Channel of Tri-Color Bank 3 00: 6 mA 01: 9 mA 10: 15 mA 11: 21 mA
LEDB31	5	R/W	RESETB	0	
LEDR3DC0	6	R/W	RESETB	0	Duty Cycle Control for the Red Channel of Tri-Color Bank 3 From 0/31 (code 00000) to 31/31 (code 01111) with 1/31 steps
LEDR3DC1	7	R/W	RESETB	0	
LEDR3DC2	8	R/W	RESETB	0	
LEDR3DC3	9	R/W	RESETB	0	
LEDR3DC4	10	R/W	RESETB	0	
LEDG3DC0	11	R/W	RESETB	0	Duty Cycle Control for the Green Channel of Tri-Color Bank 3 From 0/31 (code 00000) to 31/31 (code 01111) with 1/31 steps
LEDG3DC1	12	R/W	RESETB	0	
LEDG3DC2	13	R/W	RESETB	0	
LEDG3DC3	14	R/W	RESETB	0	
LEDG3DC4	15	R/W	RESETB	0	
LEDB3DC0	16	R/W	RESETB	0	Duty Cycle Control for the Blue Channel of Tri-Color Bank 3 From 0/31 (code 00000) to 31/31 (code 01111) with 1/31 steps
LEDB3DC1	17	R/W	RESETB	0	
LEDB3DC2	18	R/W	RESETB	0	
LEDB3DC3	19	R/W	RESETB	0	
LEDB3DC4	20	R/W	RESETB	0	
TC3PERIOD0	21	R/W	RESETB	0	Period Control for Tri-Color Bank 3 00: 0.01 seconds 01: 0.1 seconds 10: 0.5 seconds 11: 2 seconds
TC3PERIOD1	22	R/W	RESETB	0	
TC3TRIODE	23	R/W	RESETB	0	Triode Mode for Tri-Color Bank 3 Channels 0: Disable triode mode for tri-color bank 3 channels 1: Enable triode mode for tri-color bank 3 channels

Appendix A
MC13783 SPI Bitmap

MC13783 SPI Bitmap Rev 3.4										Color Coding:		PRI/SEC each their own register/bits with independent R/W and Arbitration				PRI/SEC use same register with parallel read access				PRI only		Assigned to PRI or SEC for write/read access per thick outlined area				Assigned to PRI or SEC for write access per thick outlined area, read access for both				PRI only, access with ICTEST is high			
		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register	Register Label	R/W R/T	Address 5:0						Null	Data [23:16]												Data[15:7]				Data[7:0]								
0	Interrupt Status 0	R/W	0	0	0	0	0	0	0	UDMI	CKDETI	SE1I	0	IDI	0	0	USBI	UDPI	LOBATLI	BPONI	CHGCURRI	CCCVI	CHGSHORTI	CHGREVI	CHGCVI	CHGDETI	Reserved	WLOWI	WHIGHI	TSI	ADCBISDONEI	ADCDONEI
1	Interrupt Mask 0	R/W	0	0	0	0	0	0	1	UDMIM	CKDETM	SE1M	1	IDM	1	1	USBM	UDPM	LOBATHM	LOBATLM	BPONM	CHGCURRM	CCCVM	CHGSHORTM	CHGREVM	CHGCVM	CHGDETM	Reserved	WLOWM	WHIGHM	TSM	ADCBISDONEM	ADCDONEM
2	Interrupt Sense 0	R	0	0	0	0	0	1	0	UDMS	CKDETS	SE1S	IDGNDS	IDFLOATS	USBVBS	USB2VBS	USB1VBS	UDPS	LOBATHS	LOBATLS	BPONS	CHGCURRS	CCCVS	CHGSHORTS	CHGREVS	CHGCVS	CHGDETS	Reserved	0	0	0	0	0
3	Interrupt Status 1	R/W	0	0	0	0	0	1	1	Reserved	Reserved	AHSSHORT1I	ALSPTHI	HSLI	HSDETI	MC2BI	Reserved	SEMAFI	CLKI	THWARN1H	THWARN1L	PWRRDY1I	MEMHLDI	WARM1I	PCI	RTCRSTI	SYSRSTI	ONOFD3I	ONOFD2I	ONOFD1I	Reserved	TODAI	1HZI
4	Interrupt Mask 1	R/W	0	0	0	0	0	1	0	Reserved	Reserved	AHSSHORT1M	ALSPTHM	HSLM	HSDETM	MC2BM	Reserved	SEMAFM	CLKM	THWARN1M	THWARN1L	PWRRDY1M	MEMHLDM	WARM1M	PCM	RTCRSTM	SYSRSTM	ONOFD3M	ONOFD2M	ONOFD1M	Reserved	TODAM	1HZM
5	Interrupt Sense 1	R	0	0	0	0	1	0	1	Reserved	Reserved	AHSSHORTS	ALSPTHS	HSLS	HSDETS	MC2BS	Reserved	0	CLKS	THWARN1S	THWARN1L	PWRRDYS	0	0	0	0	0	ONOFD3S	ONOFD2S	ONOFD1S	Reserved	0	0
6	Power Up Mode Sense	R	0	0	0	0	1	1	0						Reserved	Reserved	SW2ABS	SW1ABS	USBENS	UMODS[1:0]		CHRGMOD1S[1:0]		CHRGMOD0S[1:0]		PUMPS3S[1:0]		PUMPS2S[1:0]		PUMPS1S[1:0]		CLKSELS	ICTESTS
7	Identification	R	0	0	0	1	1	1	0												FAB[1:0]		FIN[1:0]			ICID[2:0]		Reserved	REVB[1:0]				
8	Semaphore	R/W	0	0	1	0	0	0	0	SEMRD6[5:0]						SEMRD4[3:0]				SEMWRT6[5:0]						SEMWRT4[3:0]				Reserved	SEMCTRLB	Reserved	SEMCTRLA
9	Arbitration Peripheral Audio	R/W	0	0	1	0	0	1	0					Reserved	ADAPTSEL	TCLEDSEL	BLLEDSEL	CHRGSEL	USBSEL	ADCSEL[1:0]		RTCSEL	Reserved	BIASSEL[1:0]		AUDIOSTDCSEL	AUDIOCDCSEL	RXGAINSEL	AUDIORXSEL[1:0]	TXGAINSEL	AUDIOTXSEL[1:0]		
10	Arbitration Switchers	R/W	0	0	1	0	1	0	0								Reserved	PWGT2SEL	PWGT1SEL	Reserved	PLLSEL	SW3SEL1	SW2BSEL	SW2ASEL	SW1BSEL	SW1ASEL	SW2ABDVS	SW1ABDVS	SW3SEL0	SW2BSTBYAND	SW2ASTBYAND	SW1BSTBYAND	SW1ASTBYAND
11	Arbitration Regulators 0	R/W	0	0	1	0	1	1	0	VRFIBGSEL[1:0]		VCAMSEL[1:0]		VESIMSEL[1:0]		VSIMSEL[1:0]		VRFCPSEL[1:0]		VRTREFSEL[1:0]		VRFDIGSEL[1:0]		VGENSEL[1:0]		VDIGSEL[1:0]		VIOLOSEL[1:0]		VIOHSEL[1:0]		VAUDIOSEL[1:0]	
12	Arbitration Regulators 1	R/W	0	0	1	1	0	0	0			GPO4SEL[1:0]		GPO3SEL[1:0]		GPO2SEL[1:0]		GPO1SEL[1:0]		Reserved		Reserved		VMMC2SEL[1:0]		VMMC1SEL[1:0]		VRF2SEL[1:0]		VRF1SEL[1:0]		VVIBSEL[1:0]	
13	Power Control 0	R/W	0	0	1	1	0	1	0	COINCHEN		VCOIN[2:0]		BATTDETEN	EOLSEL	BPDET[1:0]		VBKUP2[1:0]		VBKUP2AUTOUG	VBKUP2EN	VBKUP1[1:0]		VBKUP1AUTO	VBKUP1EN	VBKUP2AUTOMH	CLKG3KMCUEN	USEROFFCLK	USEROFFSPI	WARMEN	PCCOUNTEN	PCEN	
14	Power Control 1	R/W	0	0	1	1	1	0	0				MEMALLON		MEMTMR[3:0]				PCMAXCNT[3:0]			PCCOUNT[3:0]				PCT[7:0]						
15	Power Control 2	R/W	0	0	1	1	1	1	0													STANDBYSECINV	STANDBYPRIINV	ON3BDBNC[1:0]		ON2BDBNC[1:0]		ON1BDBNC[1:0]		ON3BRSTEN	ON2BRSTEN	ON1BRSTEN	RESTARTEN
16	Regen Assignment	R/W	0	0	1	0	0	0	0	VMMC2ESIMEN	VMMC1ESIMEN	VESIMESIMEN	REGENINV	GPO4REGEN	GPO3REGEN	GPO2REGEN	GPO1REGEN	Reserved	Reserved	VMMC2REGEN	VMMC1REGEN	VRF2REGEN	VRF1REGEN	VRFBGREGEN	VCAMREGEN	VRFCPREGEN	VRFREFREGEN	VRFDIGREGEN	VGENREGEN	VDIGREGEN	VIOLOREGEN	VIOHREGEN	VAUDIOREGEN
17	Control Spare	R/W	0	1	0	0	0	1	0																								
18	Memory A	R/W	0	1	0	0	1	0	0	MEMA[7:0]																							
19	Memory B	R/W	0	1	0	0	1	1	0	MEMB[7:0]																							
20	RTC Time	R/W	0	1	0	1	0	0	0	TOD[16:0]																							
21	RTC Alarm	R/W	0	1	0	1	0	1	0	TODA[16:0]																							
22	RTC Day	R/W	0	1	0	1	1	0	0	DAY[14:0]																							
23	RTC Day Alarm	R/W	0	1	0	1	1	1	0	DAYA[14:0]																							
24	Switchers 0	R/W	0	1	1	0	0	0	0	Reserved						SW1ASTBY[5:0]				SW1ADVS[5:0]						SW1A[5:0]							
25	Switchers 1	R/W	0	1	1	0	0	1	0							SW1BSTBY[5:0]				SW1BDVS[5:0]						SW1B[5:0]							
26	Switchers 2	R/W	0	1	1	0	1	0	0	Reserved						SW2ASTBY[5:0]				SW2ADVS[5:0]						SW2A[5:0]							
27	Switchers 3	R/W	0	1	1	0	1	1	0							SW2BSTBY[5:0]				SW2BDVS[5:0]						SW2B[5:0]							
28	Switchers 4	R/W	0	1	1	1	0	0	0	Reserved	Reserved	PLLX[2:0]			PLLEN	SW1BSFST	SW1BPANIC	SW1BDVSSPEED[1:0]		SW1BSTBYMODE[1:0]		SW1BMODE[1:0]		SW1ASFST	SW1APANIC	SW1ADVSSPEED[1:0]		Reserved		SW1ASTBYMODE[1:0]		SW1AMODE[1:0]	
29	Switchers 5	R/W	0	1	1	1	0	1	0	Reserved	SW3MODE	SW3STBY	SW3EN	SW2[1:0]		SW2BSFST	SW2BPANIC	SW2BDVSSPEED[1:0]		SW2BSTBYMODE[1:0]		SW2BMODE[1:0]		SW2ASFST	SW2APANIC	SW2ADVSSPEED[1:0]		Reserved		SW2ASTBYMODE[1:0]		SW2AMODE[1:0]	
30	Regulator Setting 0	R/W	0	1	1	1	1	0	0					Reserved		VCAM[2:0]		VESIM	VSIM	VRFCP		VRFREF[1:0]		VRFDIG[1:0]		VGEN[2:0]		VDIG[1:0]		VIOLO[1:0]		Reserved	Reserved
31	Regulator Setting 1	R/W	0	1	1	1	1	1	0									Reserved		Reserved		VMMC2[2:0]				VMMC1[2:0]		VRF2[1:0]		VRF1[1:0]		VVIB[1:0]	
32	Regulator Mode 0	R/W	1	0	0	0	0	0	0	VRFCPMODE	VRFCPSTBY	VRFCPEN	VRFREFMODE	VRFREFSTBY	VRFREFEN	VRFDIGMODE	VRFDIGSTBY	VRFDIGEN	VGENMODE	VGENSTBY	VGENEN	VDIGMODE	VDIGSTBY	VDIGEN	VIOLOMODE	VIOLOSTBY	VIOLOEN	VIOHMODE	VIOHSTBY	VIOHEN	VAUDIOMODE	VAUDIOSTBY	VAUDIOEN
33	Regulator Mode 1	R/W	1	0	0	0	0	0	1	VMMC2MODE	VMMC2STBY	VMMC2EN	VMMC1MODE	VMMC1STBY	VMMC1EN	VRF2MODE	VRF2STBY	VRF2EN	VRF1MODE	VRF1STBY	VRF1EN	VVIBEN	VRFBGSTBY	VRFBGEN	VCAMMODE	VCAMSTBY	VCAMEN	VESIMMODE	VESIMSTBY	VESIMEN	VSIMMODE	VSIMSTBY	VSIMEN
34	Power Miscellaneous	R/W	1	0	0	0	1	0	0						Reserved	PWGT1SPIEN	PWGT2SPIEN	VIBPINCTRL		GPO4STBY	GPO4EN	GPO3STBY	GPO3EN	GPO2STBY	GPO2EN	GPO1STBY	GPO1EN	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved		
35	Power Spare	R/W	1	0	0	0	1	1	0																								
36	Audio Rx 0	R/W	1	0	0	1	0	0	0	ADDRXIN	ADDSTDC	ADDCDC	Reserved	HSLDETEN	CDCOUTEN	ARXOUTSEL	ARXOUTLEN	ARXOUTREN	HSDETAUTOB	HSDETEN	HSPGDIS	AHSSEL	AHSLEN	AHSREN	LSPLEN	ALSPSEL	ALSPREF	ALSPEN	ASPSEL	ASPEN	BIASSPEED	BIASEN	VAUDIOON
37	Audio Rx 1	R/W	1	0	0	1	0	0	1		BALLR	BAL[2:0]			MONO[1:0]		PGARXIN[3:0]			ARXIN	ARXINEN	PGAST[3:0]				PGASTEN		PGARX[3:0]			PGARXEN	
38	Audio Tx	R/W	1	0	0	1	1	0	0	PGATX[4:0]				PGATXR[4:0]				RXINREC	ATXOUTEN	ATXINEN	AMC2TOV	AMC2EN	AMC1LITOV	AMC1LIEN	AMC1RTOV	AMC1REN	Reserved	MC2BDETEN	MC2BDETDBNC	MC2BEN	MC1BEN	
39	SSI Network	R/W	1	0	0	1	1	1	0			Reserved	STDCSUMGAIN	STDCRXSECGAIN[1:0]		STDCRXSECSLOT[1:0]		STDCRXSLOT[1:0]		STDCSLOTS[1:0]		CDCFSDLY	CDCSUMGAIN	CDCRXSECGAIN[1:0]		CDCRXSECSLOT[1:0]		CDCTXSECSLOT[1:0]		CD:CTXRXSLOT[1:0]		Reserved	Reserved
40	Audio Codec	R/W	1	0	0	1	0	0	0			AUDCHPF	AUDHPF	CDCLM	CDCALM	CDCBYP		CDCRESET	CDCSYNTH	CDCTS	CDCCLKEN	CDCEN	CDCFSINV	CDCCLK[2:0]		CDCFS1	CDCFS0	CDCBCLINV	CDCSM	CDCCLKSEL	CDCSSISEL	
41	Audio Stereo DAC	R/W	1	0	0	1	0	1	0	SR[3:0]					SPDIF	STDCRESET		Reserved	Reserved	STDCCLKEN		STDCEN	STDCFSOLYB	STDCCLK[2:0]		STDCFS1	STDCFS0	STDCBCLINV	STDCSM	STDCCLKSEL	STDCSSISEL		
42	Audio Spare	R/W	1	0	0	1	0	1	0																								
43	ADC 0	R/W	1	0	1	0	1	1	0	ADCBIS0			Reserved	Reserved	WCOMP	ADINC2	ADINC1	CHRGRAWDIV		TSMOD[2:0]		ADREFMODE	ADREFEN	Reserved	Reserved	ADOUTPER	ADOUTEN	UIDEN		DTHEN	RTHEN	BATICON	CHRGICON	LICELLCON
44	ADC 1	R/W	1	0	1	0	1	0	0	ADCBIS1	ADONESHOT	ADTRIGIGN	ASC	ATOX				ATO[7:0]				ADA2[2:0]				ADA1[2:0]			TRIGMASK	ADSEL	Reserved	RAND	ADEN
45	ADC 2	R	1	0	1	1	0	1	0	ADD2[9:0]										Reserved	Reserved	ADD1[9:0]										Reserved	Reserved
46	ADC 3	R/W	1	0	1	1	1	0	0	ADCBIS2										WLOW[5:0]					ICID[2:0]			WHIGH[5:0]					
47	ADC 4	R	1	0	1	1	1	1	0	ADDBIS2[9:0]										Reserved	Reserved	ADDBIS1[9:0]										Reserved	Reserved
48	Charger 0	R/W	1	1	0	0	0	0	0			Reserved	Reserved	CHRGRAWPDEN	CHRGLEDEN	UCHEN	OVCTRL[1:0]		Reserved	RVRSMODE	Reserved	FETCTRL	FETOVRD	ICHRGTR[2:0]				ICHRG[3:0]			VCHRG[2:0]		
49	USB 0	R/W	1	1	0	0	0	1	0	DMPULSE	IDPUCNTRL	IDPULSE	IDPD	USBCNTRL	BIDIR	DATSE0	CONMOD[2:0]			PULLOVR	USBXCVREN	SE0CONN	DLPSRP	VBUSPULSETMR[2:0]			VBUS750KPDENB	DP150KPU	UDMPD	UDPPD	USBPU	USBSUSPEND	RSENB
50	Charger USB 1	R/W	1	1	0	0	1	0	0																ID100KPU	RSTRI	RSPOL	VBUSEN	Reserved	VUSBEN	VUSB	VUSBIN1	VUSBIN0
51	LED Control 0	R/W	1	1	0	0	1	1	0	FLBANK3	FLBANK2	FLBANK1	FLPATTRN[3:0]				Reserved	ASREF[1:0]		ABMODE[2:0]			BOOSTEN	TRIODEXP	TRIODEAD	TRIODEMD	LEDKPRAMPDOWN	LEDADRAMPDOWN	LEDMDRAMPDOWN	LEDKPRAMPUP	LEDADRAMPUP	LEDMDRAMPUP	LEDEN
52	LED Control 1	R/W	1	1	0	0	1	0	0	SLEWLIMTC	Reserved	Reserved	Reserved	Reserved	TC1HALF	LEDB3RAMPDOWN	LED3RAMPDOWN	LED1RRAMPDOWN	LED1GRAMPDOWN	LED1BRAMPUP	LED1RRAMPUP	LED2B2RAMPDOWN	LED2R2RAMPDOWN	LED2G2RAMPDOWN	LED2B2RAMPUP	LED2G2RAMPUP	LED2R2RAMPUP	LED2B1RAMPDOWN	LED2G1RAMPDOWN	LED2R1RAMPDOWN	LED1B1RAMPUP	LED1G1RAMPUP	LED1R1RAMPUP
53	LED Control 2	R/W	1	1	0	1	0	1	0	SLEWLIMBL	BLPERIOD[1:0]		LEDKPDC[3:0]			LEDADDC[3:0]				LEDMDDC[3:0]						LEDKPC[2:0]				LEDADC[2:0]			LEDMDC[2:0]
54	LED Control 3	R/W	1	1	0	1	1	0	0	TC1TRIODE	TC1PERIOD[1:0]			LEDB1DC[4:0]				LEDG1DC[4:0]				LEDR1DC[4:0]				LEDB1[1:0]		LEDG1[1:0]		LEDR1[1:0]			
55	LED Control 4	R/W	1	1	0	1	1	1	0	TC2TRIODE	TC2PERIOD[1:0]			LEDB2DC[4:0]				LEDG2DC[4:0]				LEDR2DC[4:0]				LEDB2[1:0]		LEDG2[1:0]		LEDR2[1:0]			
56	LED Control 5	R/W	1	1	1	0	0	0	0	TC3TRIODE	TC3PERIOD[1:0]			LEDB3DC[4:0]				LEDG3DC[4:0]				LEDR3DC[4:0]				LEDB3[1:0]		LEDG3[1:0]		LEDR3[1:0]			
57	Spare	R/W	1	1	1	0	0	1	0																								
58	Trim 0	R/W	1	1	1	0	1	0	0	TRIM[23:0]																							
59	Trim 1	R/W	1	1	1	0	1	1	0	TRIM[47:24]																							
60	Test 0	R/W	1	1	1	1	0	0	0	TEST[23:0]																							
61	Test 1	R/W	1	1	1	1	0	1	0	TEST[47:24]																							
62	Test 2	R/W	1	1	1	1	1	0	0	TEST[71:48]																							
63	Test 3	R/W	1	1	1	1	1	1	0	TEST[95:72]																							

NOTES