Freescale Semiconductor
Reference Manual Addendum

MCF5373RMAD
Rev. 1.3, 05/2007

MCF5373 Reference Manual Errata

by: Microcontroller Division

This errata document describes corrections to the *MCF5373 Reference Manual*, order number MCF5373RM. For convenience, the addenda items are grouped by revision. Please check our website at http://www.freescale.com/coldfire for the latest updates.

The current version available of the *MCF5373 Reference Manual* is Revision 1.

Table of Contents

1 Errata for Revision 1

Table 1. MCF5373RM Rev 1 Errata

Location	Description
Table 2-1/Page 2-2	Change D[31:0] signal direction from output (O) to input/output (I/O).
Table 2-16/Page 2-17	Change USBOTG_PU_EN to an output and change the description to the following: Enables an external pull-up on the USBOTG_DP line. This signal is controlled by the UOCSR[BVLD] bit.
Table 3-1/Page 3-5	Change PC's Reset Value entry to "Contents of Location 0x0000_0004" and Written with MOVEC entry to "No". Change OTHER_A7's Reset Value entry to "Contents of Location 0x0000_0000".
Figure 3-5/Page 3-7	Change "Access: User read-only" to "Access: read/write". Change CCR[4:0] to read/write.
Table 3-2/Page 3-8	Remove last sentence in C bit field description.
Figure 3-8/Page 3-9	Change SR[4:0] to read/write.
Section 3.4/Page 3-11	Change last bullet to "Use of separate system stack pointers for user and supervisor modes"
Section 3.4/Page 3-11	Change last sentence in step #2 to "The IACK cycle is mapped to special locations within the interrupt controller's address space with the interrupt level encoded in the address."
Section 3.4/Page 3-11	Delete second and third sentences in step #3. Delete the clause "For processors...pointers" from the fourth sentence in step #3.
Figure 4-4/Page 4-5	Change MACSR[3:0] to R/W.
Figure 4-5/Page 4-10	Change upper 16 bits of the MASK register to read-only, with a read and reset value of 1.
Equation 4-3/Page 4-13	Add minus sign to the exponent so that it is "–(i + 1 – N)".
Table 5-2/Page 5-4	Change reset value of ACR0, ACR1 to "See Section" since some of the bits are defined after reset.
Section 5.3.2/Page 5-6	Add the following note: **NOTE** Peripheral space (0xE000_0000-0xFFFF_FFFF) should not be cached. The combination of the CACR defaults and the two ACR*n* registers must define the non-cacheable attribute for this address space.
Section 5.4.6/Page 5-14	Change first sentence from "Ways 0 and 1 of the data cache can be locked by setting CACR[DHLCK]; likewise, ways 0 and 1 of the instruction cache can be locked by setting CACR[IHLCK]." to ""Ways 0 and 1 of the cache can be locked by setting CACR[HLCK]."
Figure 5-8/Page 5-15	Change sentence near top of figure from "B) CACR[DHLCK] is set, locking ways 0 and 1." to "B) CACR[HLCK] is set, locking ways 0 and 1."
Table 8-9/Page 8-8	Added the following note to the LPCR[FWKUP] (fast wake-up) bit description: **Note:** Setting this bit is potentially dangerous and unreliable. The system may behave unpredictably when using an unlocked clock, since the clock frequency could overshoot the maximum frequency of the device.
Section 9.3.5/Page 9-6	The CDR[SSIDIV] field is a 6-bit field. Expand the field in the figure and bit description table from bits 3–0 to bits 5–0
Section 11.2.8/Page 11-10	Combine all BCR[7:0] fields into a single slave burst enable field, SBE. The only valid values for this field are 0x00 and 0xFF. All other values are reserved.

Table 1. MCF5373RM Rev 1 Errata (continued)

Location	Description
Table 13-1/Page 13-4	Change D[31:0] signal direction from output (O) to input/output (I/O).
Section 17.4.4 & 17.4.5	In figure 17-8 through figure 17-33 add 'ADDR[31:0]' label to first cycle of data signals.
Section 17.4.4.1/Page 17-12	Change last note on page from "The processor drives the data lines during the first clock cycle of the transfer. However, this should be ignored by the connected device." to: "The processor drives the data lines during the first clock cycle of the transfer with the full 32-bit address. This may be ignored by standard connected devices using non-multiplexed address and data buses. However, some applications may find this feature beneficial."
Figure 17-27/Page 17-24	Remove internal termination dashed lines for $\overline{\text{FB\_CS}}$, $\overline{\text{FB\_BE/BWE}}$, and $\overline{\text{FB\_OE}}$ signals.
Figure 17-31/Page 17-26	Remove internal termination dashed lines for $\overline{\text{FB\_CS}}$, $\overline{\text{FB\_BE/BWE}}$, and $\overline{\text{FB\_OE}}$ signals.
Figure 17-33/Page 17-27	Remove internal termination dashed lines for $\overline{\text{FB\_CS}}$, $\overline{\text{FB\_BE/BWE}}$, and $\overline{\text{FB\_OE}}$ signals.
Chapter 18	Only one SD_CS signal is available on this device. Remove mention of two chip selects throughout.
Table 18-1/Page 18-5	In the SD_DQS table entry add the following note: **Note:** If a read is attempted from a DDR SDRAM chip select when there is no memory to respond with the appropriate SD_DQS pulses, then the bus cycle will hang. Since there is no high level bus monitor on the device, a reset is the only way to exit this error condition.
Figure 18-2/Page 18-11	Replace figure with Figure 1 from AN2982 "System Design Using the ColdFire MCF5208 Split Bus Architecture" found at http://www.freescale.com/coldfire since it is more thorough.
Figure 18-2/Page 18-12	SD_D[31:0], DQ[31:0], SD_DQS[3:0], and DQS[3:0] should be SD_D[31:16], DQ[31:16], SD_DQS[3:2], and DQS[3:2], respectively, as the device does not support a 32-bit DDR bus. Replace figure with Figure 2 from AN2982 "System Design Using the ColdFire MCF5208 Split Bus Architecture" found at http://www.freescale.com/coldfire since it is more thorough.
Section 18.3.5/Page 18-13	Remove this entire section, as the device does not support a 32-bit wide DDR bus.
Table 18-8/Page 18-17	DQS_OE field should match the corresponding register diagram and be only 2 bits wide at locations 11–10. Change third sentence from "The DSQ_OE[3] bit enables SD_DQS3 and the DSQ_OE[2] bit enables SD_DQS2, and so on." to ""The DSQ_OE[1] bit enables SD_DQS3 and the DSQ_OE[0] bit enables SD_DQS2." Consequently, the reserved bit field currently at location 7–3 should be extended to bits 9–3.
Table 18-9/Page 18-19	Correct equations and examples in SDCFG1[ACT2RW, PRE2ACT, REF2ACT] fied descriptions. Change ACT2RW to the following and change PRE2ACT and REF2ACT similarly. "Suggested value = (t_{RCD} x f_{SD_CLK}) - 1 (Round up to nearest integer) Example: If t_{RCD} = 20ns and f_{SD_CLK} = 99 MHz Suggested value = (20ns x 99 MHz) - 1 = 0.98; round to 1."

Table 1. MCF5373RM Rev 1 Errata (continued)

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Section 18.4.5/Page 18-20</td><td>Add the following note:
NOTE
The user should not probe memory on a DDR chip select to determine if memory is connected. If a read is attempted from a DDR SDRAM chip select when there is no memory to respond with the appropriate DQS pulses, then the bus cycle will hang. Since there is no high level bus monitor on the device, a reset is the only way to exit the error condition.</td></tr>
<tr><td>Table 19-2/Page 19-6</td><td>Correct MIB block counters end address to 0xFC03_02FF.</td></tr>
<tr><td>Table 19-3/Page 19-6</td><td>Correct ECR reset value from 0xF000_0002 to 0xF000_0000.</td></tr>
<tr><td>Table 19-3/Page 19-7</td><td>Correct register name typo in FEC memory map at address 0xFC03_0124. This should be the Descriptor Group Lower Address Register (GALR).</td></tr>
<tr><td>Table 19-4/Page 19-8</td><td>Add RMON_R_DROP to the MIB counter memory map at address 0xFC03_0280 with a description of ‘Count of frames not counted correctly.’</td></tr>
<tr><td>Figure 19-6/Page 19-13</td><td>Correct ECR reset value from 0xF000_0002 to 0xF000_0000.</td></tr>
<tr><td>Section 19.4.7/Page 19-35</td><td>Add the following subsection entitled “Duplicate Frame Transmission”:
The FEC fetches transmit buffer descriptors (TxBDs) and the corresponding transmit data continuously until the transmit FIFO is full. It does not determine whether the TxBD to be fetched is already being processed internally (as a result of a wrap). As the FEC nears the end of the transmission of one frame, it begins to DMA the data for the next frame. In order to remain one BD ahead of the DMA, it also fetches the TxBD for the next frame. It is possible that the FEC will fetch from memory a BD that has already been processed but not yet written back (that is, it is read a second time with the R bit still set). In this case, the data is fetched and transmitted again. Using at least three TxBDs fixes this problem for large frames, but not for small frames. To ensure correct operation for either large or small frames, one of the following must be true:
• The FEC software driver ensures that there is always at least one TxBD with the ready bit cleared.
• Every frame uses more than one TxBD and every TxBD but the last is written back immediately after the data is fetched.
• The FEC software driver ensures a minimum frame size, n. The minimum number of TxBDs is then (Tx FIFO Size ÷ (n + 4)) rounded up to the nearest integer (though the result cannot be less than three). The default Tx FIFO size is 192 bytes; this size is programmable.</td></tr>
<tr><td>Table 21-2/Page 21-6</td><td>Change USBOTG_PU_EN entry to the following.
<table>
<tr><th>Signal</th><th>I/O</th><th colspan="2">Description</th></tr>
<tr><td rowspan="3">USBOTG_PU_EN</td><td rowspan="3">O</td><td colspan="2">Enables an external pull-up on the USBOTG_DP line. This signal is controlled by the UOCSR[BVLD] bit.</td></tr>
<tr><td>State Meaning</td><td>Asserted—Pull-up enabled. UOCSR[BVLD] set.
Negated—Pull-up disabled. UOCSR[BVLD] cleared.</td></tr>
<tr><td>Timing</td><td>Asynchronous</td></tr>
</table></td></tr>
<tr><td>Section 21.3.3.1/Page 21-18</td><td>Move USBCMD[ATDTW] from bit location 14 to 12 in both the register figure and bit description table. Bit 14 is reserved and must be cleared.</td></tr>
<tr><td>Table 21-19/Page 21-23</td><td>Delete last sentence in UEI bit description.
Add the following sentence to the end of the PCI bit description: “The device controller detects resume signaling only.”</td></tr>
</table>

Table 1. MCF5373RM Rev 1 Errata (continued)

Location	Description
Table 21-43/Page 21-49	Change ZLT bit description to the following: “Zero length termination select. This bit is ignored in isochronous transfers. Clearing this bit enables the hardware to automatically append a zero length packet when the following conditions are true: • The packet transmitted equals maximum packet length • The dTD has exhausted the field Total Bytes After this the dTD will be retired. When the device is receiving, if the last packet length received equals the maximum packet length and the total bytes is zero, it will wait for a zero length packet from the host to retire the current dTD. Setting this bit disables the zero length packet. When the device is transmitting, the hardware will not append any zero length packet. When receiving, it will not require a zero length packet to retire a dTD whose last packet was equal to the maximum packet length packet. The dTD is retired as soon as Total Bytes field goes to zero, or a short packet is received. 0 Enable zero length packet (default). 1 Disable the zero length packet. **Note:** Each transfer is defined by one dTD, so the zero length termination is for each dTD. In some software application cases, the logic transfer does not fit into just one dTD, so it does not make sense to add a zero length termination packet each time a dTD is consumed. On those cases we recommend to disable the ZLT feature, and use software to generate the zero length termination.”
Chapter 23	Rescind errata regarding 2HZ/2SEC bitfield name. The interrupt is, in fact, a 2 Hz interrupt.
Figure 22-15/Page 22-15	Correct register name in top of register figure from SISRR to SSI_ISR.
Figure 22-18/Page 22-20	Add R/W RXDIR bit to bit location 5 in SSI_RCR register.
Table 22-11/Page 22-21	Add RXDIR bit to bit location 5 with the following description: Gated clock enable. In synchronous mode, this bit enables gated clock mode. 0 Gated clock mode disabled. 1 Gated clock mode enabled.
Section 24.2/Page 24-2	Previous errata from revision 0 has crept in: Add a 0x20 offset to all PWM register addresses in the memory map table. Register addresses should be from 0xFC09_0020 to 0xFC09_0044. Also fix address for the PWMSDN register description to 0xFC09_0044.
Figure 25-1/Page 25-2	Change 8192 divider to 4096.
Section 25.2.3/Page 25-4	Change 8192 multiplier in equation 20-1 and text below it to 4096. As a result the maximum timeout frequency changes from 6.71 to 3.36 seconds.
Figure 26-4/Page 26-5	Remove “IPSBAR Offset” from PCNTR*n* register diagram.
Section 29.2 / Page 29-3	Changed "An internal interrupt request signal notifies the interrupt controller..." to "A request signal is provided to notify the interrupt controller...".
Table 29-6 / Page 29-9	Changed “DTIN” to “DT*n*IN” (to maintain consistent signal names throughout chapter).
Section 29.4.5.2 / Page 29-26	Changed "...complete normally without exception processing..." to "...complete normally without an error termination...".
Figure 35-3/Page 35-4	Updated the IDCODE register figure to indicate that the reset values for both PRN and PIN are device-dependent.

2 Errata for Revision 0.1

Table 2. MCF5373RM Rev 0.1 Errata

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Throughout</td><td>Remove any mention of ULPI from manual, as it is not supported on this device.</td></tr>
<tr><td>Table 2-1/Page 2-1</td><td>Change the pin number for signal A10 in the 160 QFP packaging from 11 to 117.</td></tr>
<tr><td>Table 2-1/Page 2-2</td><td>Add “Voltage Domain” column indicated the domain for each signal. The USB signals are USB_VDD, FlexBus and SDRAM signals are SD_VDD, while all the rest are EVDD.</td></tr>
<tr><td>Table 2-1/Page 2-2</td><td>Add the following footnote to the SD_BA[1:0], SD_A[13:11], SD_A[9:0], and $\overline{\text{SD\_DQM}}$[3:0] signals:
The SDRAM functions of these signals are not programmable by the user. They are dynamically switched by the processor when accessing SDRAM memory space and are included here for completeness.</td></tr>
<tr><td>Figure 2-1/Page 2-2</td><td>Remove ULPI signals as alternate 1 functions on the FEC pins. ULPI is not supported on this device.
Change FEC GPIO signal names:
<table>
<tr><th colspan="2">Original</th></tr>
<tr><th>Signal Name</th><th>GPIO</th></tr>
<tr><td>FEC_COL</td><td>PFECH4</td></tr>
<tr><td>FEC_CRS</td><td>PFECH0</td></tr>
<tr><td>FEC_RXCLK</td><td>PFECH3</td></tr>
<tr><td>FEC_RXDV</td><td>PFECH2</td></tr>
<tr><td>FEC_RXD[3:1]</td><td>PFECL[3:1]</td></tr>
<tr><td>FEC_RXD0</td><td>PFECH1</td></tr>
<tr><td>FEC_RXER</td><td>PFECL0</td></tr>
<tr><td>FEC_TXCLK</td><td>PFECL7</td></tr>
<tr><td>FEC_TXEN</td><td>PFECL6</td></tr>
<tr><td>FEC_TXER</td><td>PFECL4</td></tr>
<tr><td>FEC_TXD[3:1]</td><td>PFECL[7:5]</td></tr>
<tr><td>FEC_TXD0</td><td>PFECH5</td></tr>
</table>
<table>
<tr><th colspan="2">Corrected</th></tr>
<tr><th>Signal Name</th><th>GPIO</th></tr>
<tr><td>FEC_COL</td><td>PFECH7</td></tr>
<tr><td>FEC_CRS</td><td>PFECH6</td></tr>
<tr><td>FEC_RXCLK</td><td>PFECH5</td></tr>
<tr><td>FEC_RXDV</td><td>PFECH4</td></tr>
<tr><td>FEC_RXD[3:0]</td><td>PFECH[3:0]</td></tr>
<tr><td>FEC_RXER</td><td>PFECL7</td></tr>
<tr><td>FEC_TXCLK</td><td>PFECL6</td></tr>
<tr><td>FEC_TXEN</td><td>PFECL5</td></tr>
<tr><td>FEC_TXER</td><td>PFECL4</td></tr>
<tr><td>FEC_TXD[3:0]</td><td>PFECL[3:0]</td></tr>
</table>
</td></tr>
</table>

Table 2. MCF5373RM Rev 0.1 Errata (continued)

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Table 2-1/Page 2-6</td><td>Remove alternate functions of the FEC pins (except for the FEC_MDC and FEC_MDIO signals), as these are reserved.
Change FEC GPIO signal names:
<table>
<tr><th colspan="2">Original</th><th colspan="2">Corrected</th></tr>
<tr><th>Signal Name</th><th>GPIO</th><th>Signal Name</th><th>GPIO</th></tr>
<tr><td>FEC_COL</td><td>PFECH4</td><td>FEC_COL</td><td>PFECH7</td></tr>
<tr><td>FEC_CRS</td><td>PFECH0</td><td>FEC_CRS</td><td>PFECH6</td></tr>
<tr><td>FEC_RXCLK</td><td>PFECH3</td><td>FEC_RXCLK</td><td>PFECH5</td></tr>
<tr><td>FEC_RXDV</td><td>PFECH2</td><td>FEC_RXDV</td><td>PFECH4</td></tr>
<tr><td>FEC_RXD[3:1]</td><td>PFECL[3:1]</td><td>FEC_RXD[3:0]</td><td>PFECH[3:0]</td></tr>
<tr><td>FEC_RXD0</td><td>PFECH1</td><td></td><td></td></tr>
<tr><td>FEC_RXER</td><td>PFECL0</td><td>FEC_RXER</td><td>PFECL7</td></tr>
<tr><td>FEC_TXCLK</td><td>PFECL7</td><td>FEC_TXCLK</td><td>PFECL6</td></tr>
<tr><td>FEC_TXEN</td><td>PFECL6</td><td>FEC_TXEN</td><td>PFECL5</td></tr>
<tr><td>FEC_TXER</td><td>PFECL4</td><td>FEC_TXER</td><td>PFECL4</td></tr>
<tr><td>FEC_TXD[3:1]</td><td>PFECL[7:5]</td><td>FEC_TXD[3:0]</td><td>PFECL[3:0]</td></tr>
<tr><td>FEC_TXD0</td><td>PFECH5</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>Table 2-1/Page 2-7</td><td>Change USBHOST_VSS entry to USB_VSS and USBOTG_VDD entry to USB_VDD.</td></tr>
<tr><td>Table 2-6/Page 2-10</td><td>Correct description of the $\overline{\text{BE/BWE}n}$ signals: Remove “SRAM and” from second sentence of first paragraph, Remove SDRAM paragraph and add reference to Table 2-7.</td></tr>
<tr><td>Table 2-7/Page 2-11</td><td>Add the following to the SD_DQM[3:0] entry description:
“These pins are multiplexed with the $\overline{\text{BE/BWE}n}$ pins.
The SD_DQMn should be connected to individual SDRAM DQM signals. Note that most SDRAMs associate DQM3 with the MSB, in which case SD_DQM3 should be connected to the SDRAM's DQM3 input.”</td></tr>
<tr><td>Section 3.2.5/Page 3-7</td><td>Change bit 7 of the CCR register from a reserved bit to a read/write bit labeled ‘P’. In corresponding bit description table, add a row for the P bit with the below description:

Branch prediction bit. Alters the static prediction algorithm used by the branch acceleration logic in the IFP on forward conditional branches.
0 Predicted as not taken.
1 Predicted as taken.</td></tr>
<tr><td>Figure 3-9/Page 3-10</td><td>Change bit 7 from a reserved bit to a read/write bit labeled ‘P’.</td></tr>
<tr><td>Figure 5.2/Page 5-2</td><td>Change TAG definition label from “TAG—21-bit address tag” to “TAG—20-bit address tag”.</td></tr>
</table>

Table 2. MCF5373RM Rev 0.1 Errata (continued)

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Table 9-10/Page 9-10</td><td>Correct boot port size (D[4:3]) settings. They should match Table 9-3.
<table>
<tr><th>D[4:3]</th><th>Boot Device</th></tr>
<tr><td>00</td><td>External with 32-bit port[3] (default)</td></tr>
<tr><td>01</td><td>External with 16-bit port</td></tr>
<tr><td>10</td><td>External with 8-bit port</td></tr>
<tr><td>11</td><td>External with 32-bit port</td></tr>
</table></td></tr>
<tr><td>Table 11-1/Page 11-2</td><td>Change reset values of MPR0 to 0x7777_7777.
Change reset value of PACRA to 0x5444_4444.
Change reset values of the other PACRs to 0x4444_4444.
Change CFDTR register address from 0xFC04_0078 to 0xFC04_007C.</td></tr>
<tr><td>Figure 11-1/Page 11-3</td><td>Change reset value of MPR0 from 0x7000_0007 to 0x7777_7777.</td></tr>
<tr><td>Section 11.2.3/Page 11-4</td><td>Change reset values of PACRA to 0x5444_4444 and of the rest of the PACRs to 0x4444_4444.</td></tr>
<tr><td>Section 11.2.4/Page 11-7</td><td>Change next to last sentence in second paragraph from “...an interrupt to the interrupt controller is generated if the CFLOC[ECFEI] bit is set.” to ““...an interrupt to the interrupt controller is generated if the CFIER[ECFEI] bit is set.”</td></tr>
<tr><td>Section 11.2.8/Page 11-10</td><td>Change last sentence in first paragraph from “There is a enable bit...” to “There is an enable bit...”</td></tr>
<tr><td>Figure 11-22/Page 11-14</td><td>Change CFDTR register address from 0xFC04_0078 to 0xFC04_007C.</td></tr>
</table>

Table 2. MCF5373RM Rev 0.1 Errata (continued)

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Table 12-1/Page 12-2</td><td>For the slave modules add a column for each slave's address range, as well as two footnotes as shown below:

Table 12-1. Cross-bar Switch Master/Slave Assignments

<table>
<tr><th colspan="3">Master Modules</th></tr>
<tr><th>Cross-bar Port</th><th colspan="2">Module</th></tr>
<tr><td>Master 0 (M0)</td><td colspan="2">ColdFire Core</td></tr>
<tr><td>Master 1 (M1)</td><td colspan="2">eDMA Controller</td></tr>
<tr><td>Master 2 (M2)</td><td colspan="2">Fast Ethernet Controller</td></tr>
<tr><td>Master 4 (M4)</td><td colspan="2">Reserved</td></tr>
<tr><td>Master 5 (M5)</td><td colspan="2">USB Host</td></tr>
<tr><td>Master 6 (M6)</td><td colspan="2">USB On-the-Go</td></tr>
<tr><td>Master 7 (M7)</td><td colspan="2">Reserved for Factory Test</td></tr>
<tr><th colspan="3">Slave Modules</th></tr>
<tr><th>Cross-bar Port</th><th>Module</th><th>Address Range[1]</th></tr>
<tr><td>Slave 1 (S1)</td><td>Flexbus

SDRAM Controller</td><td>0x0000_0000–0x3FFF_FFFF &
0xC000_0000–0xDFFF_FFFF
0x4000_0000–0x7FFF_FFFF</td></tr>
<tr><td>Slave 4 (S4)</td><td>Internal SRAM Backdoor</td><td>0x8000_0000–0x8FFF_FFFF</td></tr>
<tr><td>Slave 6 (S6)</td><td>Cryptography Modules (RNG, SKHA, MDHA)</td><td>0xE000_0000–0xEFFF_FFFF[2]</td></tr>
<tr><td>Slave 7 (S7)</td><td>Other On-chip Peripherals</td><td>0xF000_0000–0xFFFF_FFFF[2]</td></tr>
</table>
[1] Unused address spaces are reserved.
[2] See the various peripheral chapters for their memory maps. Any unused space by these peripherals within this memory range is reserved and should not be accessed.</td></tr>
<tr><td>Section 12.1/Page 12-2</td><td>Add the following note below the above added table.

NOTE

This memory map provides two disjoint regions mapped to the FlexBus controller to support glueless connections to external memories (e.g., flash and SRAM) as well as a second space with one (or more) unique chip-selects that can be used for non-cacheable, non-memory devices (addresses 0xC000_0000–0xDFFF_FFFF). Additionally, this mapping is selected since it easily maps into the ColdFire access control registers, which provide a coarse association between memory addresses and their attributes (e.g., cacheable, non-cacheable). For this device, one possible configuration defines the default memory attribute as non-chacheable, and one ACR is then used to identify cacheable addresses, e.g., ADDR[31]=0 identifies the cacheable space.</td></tr>
<tr><td>Table 13-1/Page 13-1</td><td>Change the pin number for signal A10 in the 160 QFP packaging from 11 to 117.</td></tr>
</table>

Table 2. MCF5373RM Rev 0.1 Errata (continued)

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<tr><td>FEC_CRS</td><td>PFECH0</td></tr>
<tr><td>FEC_RXCLK</td><td>PFECH3</td></tr>
<tr><td>FEC_RXDV</td><td>PFECH2</td></tr>
<tr><td>FEC_RXD[3:1]</td><td>PFECL[3:1]</td></tr>
<tr><td>FEC_RXD0</td><td>PFECH1</td></tr>
<tr><td>FEC_RXER</td><td>PFECL0</td></tr>
<tr><td>FEC_TXCLK</td><td>PFECL7</td></tr>
<tr><td>FEC_TXEN</td><td>PFECL6</td></tr>
<tr><td>FEC_TXER</td><td>PFECL4</td></tr>
<tr><td>FEC_TXD[3:1]</td><td>PFECL[7:5]</td></tr>
<tr><td>FEC_TXD0</td><td>PFECH5</td></tr>
</table>
<table>
<tr><th colspan="2">Corrected</th></tr>
<tr><th>Signal Name</th><th>GPIO</th></tr>
<tr><td>FEC_COL</td><td>PFECH7</td></tr>
<tr><td>FEC_CRS</td><td>PFECH6</td></tr>
<tr><td>FEC_RXCLK</td><td>PFECH5</td></tr>
<tr><td>FEC_RXDV</td><td>PFECH4</td></tr>
<tr><td>FEC_RXD[3:0]</td><td>PFECH[3:0]</td></tr>
<tr><td>FEC_RXER</td><td>PFECL7</td></tr>
<tr><td>FEC_TXCLK</td><td>PFECL6</td></tr>
<tr><td>FEC_TXEN</td><td>PFECL5</td></tr>
<tr><td>FEC_TXER</td><td>PFECL4</td></tr>
<tr><td>FEC_TXD[3:0]</td><td>PFECL[3:0]</td></tr>
</table>
</td></tr>
</table>

Table 2. MCF5373RM Rev 0.1 Errata (continued)

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Table 13-1/Page 13-6</td><td>Remove alternate functions of the FEC pins (except for the FEC_MDC and FEC_MDIO signals), as these are reserved.
Change FEC GPIO signal names:
<table>
<tr><th colspan="2">Original</th><th colspan="2">Corrected</th></tr>
<tr><th>Signal Name</th><th>GPIO</th><th>Signal Name</th><th>GPIO</th></tr>
<tr><td>FEC_COL</td><td>PFECH4</td><td>FEC_COL</td><td>PFECH7</td></tr>
<tr><td>FEC_CRS</td><td>PFECH0</td><td>FEC_CRS</td><td>PFECH6</td></tr>
<tr><td>FEC_RXCLK</td><td>PFECH3</td><td>FEC_RXCLK</td><td>PFECH5</td></tr>
<tr><td>FEC_RXDV</td><td>PFECH2</td><td>FEC_RXDV</td><td>PFECH4</td></tr>
<tr><td>FEC_RXD[3:1]</td><td>PFECL[3:1]</td><td>FEC_RXD[3:0]</td><td>PFECH[3:0]</td></tr>
<tr><td>FEC_RXD0</td><td>PFECH1</td><td></td><td></td></tr>
<tr><td>FEC_RXER</td><td>PFECL0</td><td>FEC_RXER</td><td>PFECL7</td></tr>
<tr><td>FEC_TXCLK</td><td>PFECL7</td><td>FEC_TXCLK</td><td>PFECL6</td></tr>
<tr><td>FEC_TXEN</td><td>PFECL6</td><td>FEC_TXEN</td><td>PFECL5</td></tr>
<tr><td>FEC_TXER</td><td>PFECL4</td><td>FEC_TXER</td><td>PFECL4</td></tr>
<tr><td>FEC_TXD[3:1]</td><td>PFECL[7:5]</td><td>FEC_TXD[3:0]</td><td>PFECL[3:0]</td></tr>
<tr><td>FEC_TXD0</td><td>PFECH5</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>Table 13-1/Page 13-10</td><td>Change USBHOST_VSS entry to USB_VSS and USBOTG_VDD entry to USB_VDD.</td></tr>
<tr><td>Table 13-3/Page 13-9</td><td>Correct the various FEC GPIO register addresses.
<table>
<tr><th>Register</th><th>Original Address</th><th>Corrected Address</th></tr>
<tr><td>PODR_FECH</td><td>0xFC0A_4000</td><td>0xFC0A_400E</td></tr>
<tr><td>PODR_FECL</td><td>0xFC0A_4001</td><td>0xFC0A_400F</td></tr>
<tr><td>PDDR_FECH</td><td>0xFC0A_4014</td><td>0xFC0A_4022</td></tr>
<tr><td>PDDR_FECL</td><td>0xFC0A_4015</td><td>0xFC0A_4023</td></tr>
<tr><td>PPDSDR_FECH</td><td>0xFC0A_4028</td><td>0xFC0A_4036</td></tr>
<tr><td>PPDSDR_FECL</td><td>0xFC0A_4029</td><td>0xFC0A_4037</td></tr>
<tr><td>PCLRR_FECH</td><td>0xFC0A_403C</td><td>0xFC0A_404A</td></tr>
<tr><td>PCLRR_FECL</td><td>0xFC0A_403D</td><td>0xFC0A_404B</td></tr>
<tr><td>PAR_FEC</td><td>0xFC0A_4050</td><td>0xFC0A_405D</td></tr>
</table></td></tr>
<tr><td>Figure 13-3/Page 13-12</td><td>Correct PODR_FECH register address to 0xFC0A_400E.
Correct PODR_FECL register address to 0xFC0A_400F.</td></tr>
<tr><td>Figure 13-9/Page 14-14</td><td>Correct PDDR_FECH register address to 0xFC0A_4022.
Correct PDDR_FECL register address to 0xFC0A_4023.</td></tr>
</table>

Table 2. MCF5373RM Rev 0.1 Errata (continued)

Location	Description
Figure 13-15/Page 13-16	Correct PPDSDR_FECH register address to 0xFC0A_4036. Correct PPDSDR_FECL register address to 0xFC0A_4037.
Figure 13-21/Page 13-18	Correct PCLRR_FECH register address to 0xFC0A_404A. Correct PCLRR_FECL register address to 0xFC0A_404B.
Figure 13-33/Page 13-23	Correct PAR_FECH register address to 0xFC0A_405D. Change PAR_FEC_7W to a one-bit field at bit number 3. Change PAR_FEC_MII to a one-bit field at bit number 1.
Table 13-15/Page 13-24	Change PAR_FEC_7W to a one-bit field at bit number 3. Change PAR_FEC_7W bit description to: “FEC 7-wire pin assignment. These bit fields configure the FEC_COL, FEC_RXCLK, FEC_RXDV, FEC_RXD0, FEC_TXCLK, FEC_TXD0, and FEC_TXEN pins for their primary FEC function or GPIO. 0 Above pins configured as GPIO. 1 Above pins configured as FEC.”
Table 13-15/Page 13-24	Change PAR_FEC_MII to a one-bit field at bit number 1. Change PAR_FEC_MII bit description to: “FEC MII pin assignment. These bit fields configure the FEC_CRS, FEC_RXD3, FEC_RXD2, FEC_RXD1, FEC_RXER, FEC_TXD3, FEC_TXD2, FEC_TXD1 and FEC_TXER pins for their primary FEC function or GPIO. 0 Above pins configured as GPIO. 1 Above pins configured as FEC.”
Figure 13-28/Page 13-20	Change figure title to “Chip Select Pin Assignment Register (PAR_CS)”
Table 13-10/Page 13-20	Correct table title to “PAR_CS Field Descriptions” Correct bit field names for bit 5 and bit 4. Bit 5 field should be PAR_CS5 and bit field 4 should be PAR_CS4. The corresponding bit descriptions are correct.
Table 14-15/Page 14-12	Correct source #25, “Flag clearing mechanism” entry from “Write CWIR[CWIC]=1” to “Write SCMISR[CWIC]=1”.
Figure 15-3/Page 15-4	Change register diagram from 16-bit to 8-bit as shown below: Address: 0xFC09_4002 (EPDDR) Access: Supervisor read/write 7 6 5 4 3 2 1 0 R EPDD7 EPDD6 EPDD5 EPDD4 EPDD3 EPDD2 EPDD1 0 W Reset 0 0 0 0 0 0 0 0 **Figure 15-3. EPORT Data Direction Register (EPDDR)**
Throughout Chapter 17	In all timing diagrams within the FlexBus chapter, the address and data signals stop driving the bus one clock cycle sooner than shown. Because of this, in the diagrams illustrating address hold, the address hold state is swapped with the S3 state.
Figure 17-28/Page 17-23	Insert a single clock cycle for address setup at the beginning of each data transfer, between S0 and S1 states.
Figure 17-29/Page 17-24	Insert a single clock cycle for address setup at the beginning of each data transfer, between S0 and S1 states.
Section 18.5.2/Page 18-23	Remove “Perform a single read/write to any of the SDRAM chip select address spaces to issue the command.” sentence from steps 5 and 9 of Section 18.6, “Initialization/Application Information.” This is not recommended or necessary.

Table 2. MCF5373RM Rev 0.1 Errata (continued)

Location	Description
Table 19-2/Page 19-5	Change reset value of ECR register from 0x0000_0000 to 0xF000_0002.
Section 19.2.3/Page 19-6	Change second sentence in first paragraph from “These fall in the 0xFC03_0200-0xFC03_03FF address offset range.” to “These fall in the 0xFC03_0200-0xFC03_02FF address range.”
Figure 19-6/Page 19-12	Change reset value of ECR register from 0x0000_0000 to 0xF000_0002.
Table 19-11/Page 19-15	Change 80MHz entry for MSCR[MII_SPEED] from 0xF to 0x10.
Section 21.3.3.15/Page 21-37	Change bit 2 in the USBMODE register from a reserved bit to a read/write bit labeled ‘ES’. In corresponding bit description table, change bit 2 to the ES bit with the below description: Endian select. Controls the byte ordering of the transfer buffers to match the host microprocessor bus architecture. The bit fields in the register interface and the DMA data structures (including the setup buffer within the device QH) are unaffected by the value of this bit, because they are based upon 32-bit words. 0 Little endian. First byte referenced in least significant byte of 32-bit word. 1 Big endian. First byte referenced in most significant byte of 32-bit word. For proper operation, this bit must be set for this ColdFire device.
Table 34-5/Page 34-8	Clarify in CSR field descriptions that the read-only bits can only be accessed via the BDM port and not read via the processor. The CSR is supervisor write-only from the processor.

3 Errata for Revision 0

Table 3. MCF5373RM Rev 0 Errata

<table>
<tr><th>Location</th><th>Description</th></tr>
<tr><td>Table 2-2/Page 2-7</td><td>Replace the table with the following. Notice the addition of the D0 entry:
Table 2-2. Internal Pull-up/down Resistors
<table>
<tr><th>Pin Name</th><th>Pull-Up</th><th>Pull-Down</th><th>Comment</th></tr>
<tr><td>RESET</td><td>x</td><td></td><td>Always, except JTAG mode</td></tr>
<tr><td>TEST</td><td></td><td>x</td><td>Always, except JTAG mode</td></tr>
<tr><td>RCON</td><td>x</td><td></td><td>Always, except JTAG mode</td></tr>
<tr><td>XTAL</td><td>x</td><td></td><td>When not in crystal oscillator mode (intended for factory test)</td></tr>
<tr><td>IRQ[7:1]</td><td>x</td><td></td><td></td></tr>
<tr><td>TA</td><td>x</td><td></td><td>Only when used as TA</td></tr>
<tr><td>D0</td><td>x</td><td></td><td>During reset only</td></tr>
<tr><td>QSPI_DOUT</td><td>x</td><td></td><td>I^{2}C mode only (I2C_SDA)</td></tr>
<tr><td>QSPI_CLK</td><td>x</td><td></td><td>I^{2}C mode only (I2C_SCL)</td></tr>
<tr><td>FEC_MDIO</td><td>x</td><td></td><td>I^{2}C mode only (I2C_SDA)</td></tr>
<tr><td>FEC_MDC</td><td>x</td><td></td><td>I^{2}C mode only (I2C_SCL)</td></tr>
<tr><td>I2C_SDA</td><td>x</td><td></td><td>I^{2}C mode only (I2C_SDA)</td></tr>
<tr><td>I2C_SCL</td><td>x</td><td></td><td>I^{2}C mode only (I2C_SCL)</td></tr>
<tr><td>DT0IN</td><td>x</td><td></td><td>When used as DREQ0</td></tr>
<tr><td>U1RXD</td><td>x</td><td>x</td><td>When used as SSI_RXD, configured by the MISCCR register in the CCM</td></tr>
<tr><td>U1TXD</td><td>x</td><td>x</td><td>When used as SSI_TXD, configured by the MISCCR register in the CCM</td></tr>
<tr><td>JTAG_EN</td><td></td><td>x</td><td></td></tr>
<tr><td>TDI</td><td>x</td><td></td><td>JTAG mode only</td></tr>
<tr><td>TMS</td><td>x</td><td></td><td>JTAG mode only</td></tr>
<tr><td>TRST</td><td>x</td><td></td><td>JTAG mode only</td></tr>
<tr><td>TCLK</td><td>x</td><td></td><td>JTAG mode only</td></tr>
</table></td></tr>
<tr><td>Section 5.3.1/Page 5-4</td><td>Change CACR bit 4 from reserved to EUSP in register figure and bit description table. Add the following for EUSP’s bit description:

Enable user stack pointer. See Section 3.2.3, “Supervisor/User Stack Pointers (A7 and OTHER_A7),” for more information on the dual stack pointer implementation.
0 Disable the processor’s use of the User Stack Pointer
1 Enable the processor’s use of the User Stack Pointer</td></tr>
</table>

Table 3. MCF5373RM Rev 0 Errata (continued)

Location	Description
Section 5.4.4/Page 5-12	Change last sentence from: “Therefore, on-chip DMA channels cannot access local memory and do not maintain coherency with the unified cache.” to: “Therefore, on-chip DMA channels should not access cached local memory locations, as coherency is not maintained with the unified cache.”
Section 5.5/Page 5-16	Remove cache code examples from section, as they are incorrect. Cache code examples can be found within sample projects in the ‘MCF532XSC.ZIP’ file available at the device web site at http://www.freescale.com/coldfire
Table 6-1/Page 6-2	Remove ‘1’ from RAMBAR register name and mnemonic.
Section 6.2.1/Page 6-2	Add the following two notes: **Note:** By default the RAMBAR is invalid, but the back door is enabled. In this state, any core accesses to the SRAM will be routed through the backdoor. Therefore the SRAM is accessible by the core, but it will not have a single-cycle access time. In order to insure that the core will have single-cycle access to the SRAM, the RAMBAR[V] bit should be set. **Note:** Any access within the memory range allocated for the on-chip SRAM (0x8000_0000-0x8FFF_FFFF) will "hit" in the SRAM even if the address is beyond the defined size for the SRAM. This creates a ghosting effect for the on-chip SRAM memory. For example, writes to addresses 0x8000_0000 and 0x8000_8000 will actually modify the exact same memory location. System software should ensure that SRAM address pointers do not exceed the size of the SRAM in order to prevent unwanted overwriting of SRAM.
Figure 6-1/Page 6-2	Change the reset value for the RAMBAR[BDE] bit from 0 to 1.
Table 11-1/Page 11-2	Correct BCR register address from 0xFC04_002A to 0xFC04_0024.
Figure 11-17/Page 11-10	Correct BCR register address from 0xFC04_002A to 0xFC04_0024.
Chapter 12	Add reserved masters used only for factory test purposes at location M4 and M7. The XBS_PRS*n*[M4,M7] fields must comply with the restriction that their value must be unique to the other M*n* fields.
Section 12.4.1/Page 12-4	The possible values for the XBS_PRS*n* fields depend on the number of masters available on the device. Since the device contains seven masters (including reserved masters) then valid values are ‘000’ to ‘110’. Unpredictable results will occur when using the reserved 111 setting. Update reset values accordingly to 0x6543_0210.
Table 13-1/Page 13-4	Update footnotes in table to correspond to corrections in Table 2-2 as indicated above.
Table 13-14/Page 13-23	In the bit descriptions for the PAR_U0CTS and PAR_U0RTS bits, the description for the bit being set incorrectly refers to UART1 while it should refer to the UART0 port.
Section 17.3.1.1/Page 17-4	Change next to last sentence in section to “For example, a 16-bit address/16-bit data device would connect its addr[15:0] to A[16:1] and data[15:0] to D[31:16].”
Section 17.4.2/Page 17-9	Change the end of the first sentence of the second paragraph from: “...if a longword is transferred for three port sizes when not in split but mode.” to “...if a longword is transferred for three port sizes when not in split bus mode.”
Figure 19-24/Page 19-23	Correct EMRBR register address from 0xFC03_01B8 to 0xFC03_0188
Section 21.1.3/Page 21-4	Add the following sub-bullet under the “USB device mode” bullet: — Supports full-speed operation via the on-chip transceiver and FS/HS operation using an external ULPI transceiver

Table 3. MCF5373RM Rev 0 Errata (continued)

Location	Description
Section 21.1.3/Page 21-5	Change the following sub-bullet: “External ULPI transceiver supports high speed (480 Mbps), full speed, and low speed” to — External ULPI transceiver supports high-speed (480 Mbps), full-speed, and low-speed operation in host mode and high-speed and full-speed operation in device mode.
Table 21-40/Page 21-45	Change “USB Device FS/LS” entry to “USB Device FS”. Change “Host/Device ULPI HS/FS/LS” to “Host/Device ULPI HS/FS”.
Section 21.4.4.1/Page 21-45	In the note, change the second sentence of the second paragraph from “Device operation requires a 1.5kΩ pull-up resistor on either DP (full-speed operation) or DN (low-speed operation) ports.” to “Device operation requires a 1.5kΩ pull-up resistor on DP (full-speed operation).” since low-speed operation is not supported in device mode.
Section 23.3/Page 23-3	Add 0xFC0A_0800 to each register address.
Section 23.3.6/Page 23-6	Change RTC_ISR[2HZ] bit field name to 2SEC as it more accurately describes the bit definition.
Section 23.3.7/Page 23-7	Change RTC_IER[2HZ] bit field name to 2SEC as it more accurately describes the bit definition.
Section 24.2/Page 24-2	Add a 0x20 offset to all PWM register addresses throughout section. Register addresses should be from 0xFC09_0020 to 0xFC09_0044.
Table 34-21/Page 34-35	Remove ‘1’ from RAMBAR register name and mnemonic.

4 Revision History

Table 4 provides a revision history for this document.

Table 4. Revision History Table

Rev. Number	Substantive Changes	Date of Release
The below errata were added for MCF5373RM Revision 0		
0	Initial release. • Added “Signal Descriptions” chapter errata. • Added cache coherency section errata. • Added RAMBAR section errata. • Added RAMBAR[BDE] reset value errata. • Added BCR register address errata. • Added internal pull-up/down corrections. • Added PAR_U0CTS & PAR_U0RTS bit description errata. • Added Flexbus typo regarding split bus mode.	12/2005
0.1	• Added USB OTG chapter errata regarding device mode not supporting low-speed operation.	12/2005
0.2	• Added CACR[EUSP] bit errata. • Added PWM register address errata. • Added FEC EMRBR address errata. • Added cross-bar reserved masters and restriction on the M*n* bit field settings. • Added RTC_I*x*R[2HZ] bit name errata. • Added RTC register address errata. • Added Flexbus 16-bit address connection example errata. • Added FlexCAN IMASK register address errata and register suffix errata. • Added RAMBAR1 errata in SRAM and Debug chapters.	02/2006

Table 4. Revision History Table (continued)

Rev. Number	Substantive Changes	Date of Release
The below errata were added for MCF5373RM Revision 0.1		
0.3	• Added CCR[P] bit errata. • Added USBMODE[ES] bit errata.	02/2006
0.4	• Added $\overline{\text{BE}}$/$\overline{\text{BWE}}$*n* and SD_DQM*n* signal description errata. • Added edge port EPDDR register figure errata. • Added FEC MSCR programming example table errata. • Added FEC ECR register reset value. • Added cache code example errata.	02/2006
0.5	• Added PAR_CS[5,4] field name and figure/table title errata. • Added FEC MIB memory map address range errata. • Added TAG description labe errata in cache chapter. • Added CFLOC-> CFIER register errata in SCM chapter. • Added typo in BCR section in SCM chapter. • Added flag clearing mechanism errata for source #25 in interrupt source table. • Added CFDTR register address errata. • Added boot port size errata. • Added CSR read-only clarification. • Added FlexCAN wake-up interrupt source errata.	03/2006
0.6	• Added GPIO signal name assignment errata for FEC pins. • Added ULPI errata. • Added MPR0 reset value errata. • Added Flexbus burst-inhibited transfer timing diagram errata.	05/2006
0.7	• Added 160QFP A10 signal pin location errata. • Added voltage domain column, USB_VDD/USB_VSS name change errata, and SDRAM signal footnotes to pin-muxing table. • Added crossbar switch slave address range errata. • Added FlexBus diagrams errata regarding address & data lines. • Added SDRAM initialization sequence errata regarding PALL command.	07/2006
The below errata were added for MCF5373RM Revision 1		
1	• Added notes regarding SDRAM bus hanging if the memory does not respond with appropriate DQS pulses. • Added five SDRAM chapter errata regarding 32-bit DDR bus.	08/2006
1.1	• Added PCNTR*n* register diagram errata. • Added D[31:0] direction errata in Table 2-1 and Table 13-1. • Added note to LPCR[FWKUP] bit. • Added CDR[SSIDIV] field width errata. • Added SSI_ISR register mnemonic errata. • Rescinded errata regarding 2HZ/2SEC bitfield name. • Added cache lock errata.	10/2006

Table 4. Revision History Table (continued)

Rev. Number	Substantive Changes	Date of Release
1.2	• Added SSI_RCR[RXDIR] errata. • Added RMON_R_DROP counter in FEC MIB counters memory map. • Added ADDR[31:0] label on FlexBus figures and note explaining this clock cycle. • Added PWM memory map errata.	11/2006
1.3	• Added various core, EMAC, cache, RAMBAR, and debug chapters errata. • Added SCM's BCR errata. • Added 2 FEC memory map typos. • Added FEC ECR reset value errata. • Added watchdog timer multiplier errata. • Added "Duplicate Frame Transmission" section to FEC chapter. • Added internal termination figure errata for longword write bursts. • Added USBOTG_PU_EN signal description errata. • Added USBCMD[ATDTW] errata. • Added USBSTS[UEI,PCI] and ZLT bit description errata. • Added SDCFG1 field description errata. • Added various UART errata. • Updated the IDCODE register figure to indicate that the reset values for both PRN and PIN are device-dependent. • Added SDCFG1 field description errata. • Added SDRAM chip select errata.	05/2007

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