DEMO9S08SF4

Demonstration Board for Freescale MC9S08SF4
Microcontroller

USER GUIDE

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REVISION

Date	Rev	Comments
June 9, 2009	A	Initial Release

CAUTIONARY NOTES

1) Electrostatic Discharge (ESD) prevention measures should be used when handling this product. ESD damage is not a warranty repair item.

2) Axiom Manufacturing does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under patent rights or the rights of others.

3) EMC Information on the DEMO9S08SF4 board:

   a) This product as shipped from the factory with associated power supplies and cables, has been verified to meet with requirements of CE and the FCC as a CLASS A product.

   b) This product is designed and intended for use as a development platform for hardware or software in an educational or professional laboratory.

   c) In a domestic environment, this product may cause radio interference in which case the user may be required to take adequate prevention measures.

   d) Attaching additional wiring to this product or modifying the products operation from the factory default as shipped may effect its performance and cause interference with nearby electronic equipment. If such interference is detected, suitable mitigating measures should be taken.

TERMINOLOGY

This development module utilizes option select jumpers to configure default board operation. Terminology for application of the option jumpers is as follows:

Jumper – a plastic shunt that connects 2 terminals electrically

Jumper on, in, or installed – jumper is a plastic shunt that fits across 2 pins and the shunt is installed so that the 2 pins are connected with the shunt.

Jumper off, out, or idle – jumper or shunt is installed so that only 1 pin holds the shunt, no 2 pins are connected, or jumper is removed. It is recommended that the jumpers be placed idle by installing on 1 pin so they will not be lost.

Cut-Trace – a circuit trace connection between component pads. The circuit trace may be cut using a knife to break the default connection. To reconnect the circuit, simply install a suitably sized 0-ohm resistor or attach a wire across the pads.

 Signal names followed by an asterisk (*) denote active-low signals.

FEATURES

The DEMO9S08SF4 is a demonstration board for the MC9S08SF4 microcontroller. Application development is quick and easy with the integrated, Open-Source, USB-BDM, sample software tools, and examples. An optional BDM_PORT port is also provided to allow use of a BDM_PORT cable. One, 40-pin connector provides access to all IO signals on the target MCU.

- MC9S08SF4, 20 TSSOP
  - 4K Bytes Flash
  - 128 Bytes RAM
- Integrated Open-Source, USB-BDM
- BDM_PORT header for external BDM cable support
- MCU_PORT pin header for access to MCU IO signals
- Power from USB-BDM or MCU_PORT connector
- USB-BDM Power Options include +5.0VDC and +3.3VDC
- Power Input Selection Jumpers
  - Voltage Output Select from USB-BDM
  - Power input from Connector J1
  - Optional Power output through Connector J1
- User Components Provided
  - 3 Push Switches; 2 User, 1 Reset
  - 5 LED Indicators; 2 User, VDD, STATUS, TPWR
  - 5K ohm POT w /LP Filter
  - 2300 Hz Piezo Buzzer w/ External Drive Circuit
- User Option Jumpers to disconnect Peripherals
- Connectors
  - 40-pin MCU I/O Pin Header
  - BDM_PORT Connector for External BDM Cable (not installed)
  - USB Connector
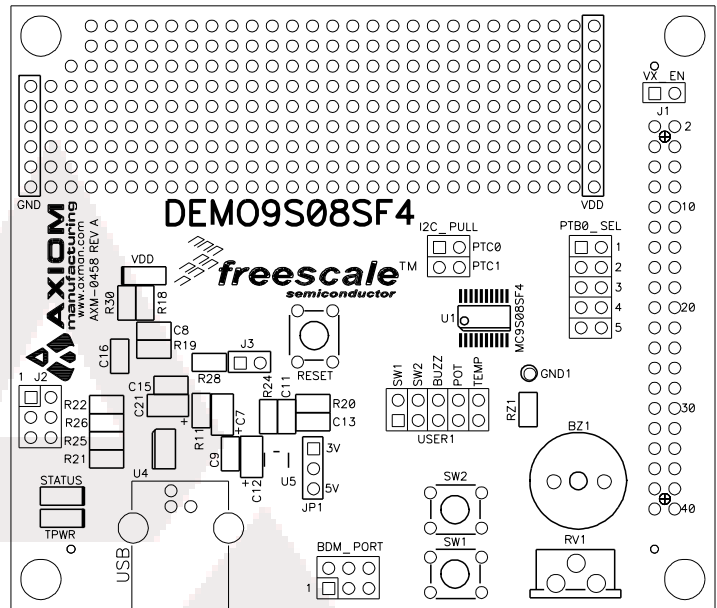
Specifications:
Board Size 3.5" x 3.0"

REFERENCES

The following reference documents are available on the CD or DVD provided with this board in Acrobat Reader format. These documents are also available at www.axman.com/support.

DEMO9S08SF4_UG.doc   DEMO9S08SF4 User Guide (this document)
DEMO9S08SF4_SCH_A.pdf   DEMO9S08SF4 Schematic Rev. A
DEMO9S08SF4_Silk_A.pdf   DEMO9S08SF4 Top Silk, Rev A
DEMO9S08SF4_Assy_A.pdf   DEMO9S08SF4 Default Shunt Placement
DEMO9S08SF4.zip   DEMO9S08SF4 Demo Application

MEMORY MAP

Figure 1 below shows the default memory map for the MC9S08SV16 and the MC9S08FL16 immediately out of reset.   Refer to the MC9S08SF4 Reference Manual (RM) for further details.

Figure 1: Memory Map

Address	Region
$0000	Direct Page Registers
$007F	
$0080	RAM 128 bytes
$00FF	
$0100	Unimplemented
$017F	
$1800	High Page Registers
$185F	
$1860	Unimplemented
$EFFF	
$D000	FLASH 4096 bytes
$FFFF	

NOTE: The memory map above applies to the MC9S08SV16 and MC9S08FL16 microcontrollers

SOFTWARE DEVELOPMENT

Software development requires the use of a compiler or an assembler supporting the HCS08 instruction set and a host PC operating a debug interface. CodeWarrior Development Studio for Microcontrollers is supplied with this board for application development and debug.   Refer to the supporting CodeWarrior documentation for details on use and capabilities.

DEVELOPMENT SUPPORT

Application development and debug for the target MC9S08SF4 is supported through the integrated, Open-Source Background Debug Mode (USB-BDM) interface. An optional 6-pos BDM_PORT header allows connecting an external HCS12/HCS08 BDM cable. This header is not installed in default configurations.

Integrated BDM

The DEMO9S08SF4 board features an integrated Open Source BDM (USB-BDM) based on the Freescale MC9S08JM60 MCU. The integrated USB BDM supports application development and debugging via background debug mode and provides primary power to the development module. The integrated BDM is fully supported by CodeWarrior development tools.

The integrated USB BDM provides power and ground to the target board eliminating the need to power the board externally. Power from the USB BDM is derived from the USB bus. The integrated USB BDM is designed to sink a maximum of 300mA of current from the USB bus. Therefore, total current consumption for the target board, and connected circuitry, **must not exceed 300mA**. This current limit describes the current supplied by the USB cable to the BDM circuit, the target board, and any connected circuitry. Excessive current drain will violate the USB specification causing the bus to disconnect. Damage to the host PC USB hub or the target board may result.

BDM_PORT Header

A compatible HCS12 BDM cable may also attach to the 6-pin BDM interface header (BDM_PORT). Figure 2 below shows the pin-out for the BDM_PORT header.

Figure 2: BDM_PORT Header

BKGD | **1** | **2** | GND   See the MC9S08SF4 Reference Manual for details
     | **3** | **4** | RESET*
     | **5** | **6** | VDD

NOTE: The BDM_PORT header is not installed in default configuration.

POWER

The DEMO9S08SF4 may be powered from the integrated USB-BDM or from the MCU IO connector at J1. The USB-BDM is designed to supply either +5VDC or +3.3VDC to the target MCU. The VOUT_SEL option jumper at JP1 selects the desired output voltage.

Power may also be applied to connector J1 or the board may be configured to supply power from connector J1 to external circuitry.

> ### CAUTION:
>
> Damage to the board may result if voltages greater than +5.5V are applied at connector J1 input.

POWER SELECT

Power may be applied to the board through the integrated BDM circuitry, or through connector J1. Power selection is achieved using 2 selection headers: the VOUT_SEL option header and the VX_EN option header. Optionally, power may be sourced to external circuitry through connector J1.

VOUT_SEL

The PWR_SEL option header allows the user to select power input either from either an external power source connected to the VIN connector or from the integrated USB-BDM. Figure 3 below details the PWR_SEL header connections.

Figure 3: VOUT_SEL Option Header

3V

5V   Enables +5VDC to target MCU (default)

3V   Enables +3.3VDC to target MCU

5V
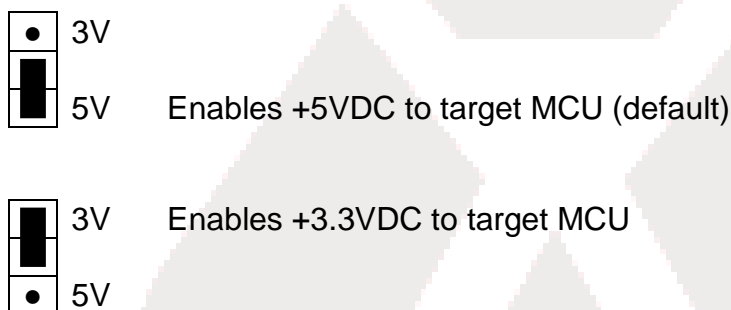
> ### CAUTION:
>
> Do not configure the target board to draw more than 300mA when powered from the integrated USB BDM. Damage to the target board or host PC may result otherwise.

Power from the integrated BDM is drawn from the USB bus and is limited to **300 mA**. This current limit accounts for the total current supplied over the USB cable to the BDM circuit, the target board, and any connected circuitry. Current drain in excess of value violates the USB specification and will cause the USB bus to disconnect. This may cause the board to exhibit power cycling where the board appears to turn off and back on continually. Damage to the host PC or the target board may result.

VX_EN

The VX_EN option header is a 2-pin jumper that connects or disconnects input J1-1 directly to the target board voltage rail. J1-3 connects directly to the target board ground plane. Use of this feature requires a regulated input power source. This power input is decoupled to minimize noise but is not regulated or protected. Care should be exercised when using this feature; no protection is applied on this input and damage to the target board may result if excessive voltage is applied. Also, do not attempt to power the target board through this connector while also applying power through the USB BDM or the PWR connector; damage to the board may result.

Power may also be sourced to off-board circuitry through the J1 connector. The current supplied from the USB bus limits current available to external circuitry. Excessive current drain may damage the target board, the host PC USB hub. The figure below details the VX_EN header connections.

Figure 4: VX_EN Option Header


```
              ON        OFF
           Enabled   Disabled
VX_EN
```
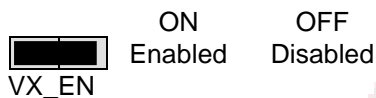
CAUTION:
Do not exceed available current from USB-BDM when sourcing power through connector J1 to external circuitry.

RESET SWITCH

The RESET switch applies an asynchronous RESET to the MCU. The RESET switch is connected directly to the RESET* input on the MCU. Pressing the RESET switch applies a low voltage level to the RESET* input. A pull-up bias resistor allows normal MCU operation. Shunt capacitance smoothes the reset pulse and ensures adequate pulse width.

The MC9S08SF4 MCU applies a multiplexed RESET* input. To use the RESET switch, the RESET pin must be enabled (SOPT1_RSTPE). Refer to the MC9S08SF4 Reference Manual for details on configuring using the RESET* input.

LOW VOLTAGE RESET

The MC9S08SF4 applies an internal Low Voltage Detect (LVD) circuitry. The LVD holds the MCU in reset until applied voltage reaches the appropriate level. The LVD also protects against under-voltage conditions. Consult the MC9S08SF4 Reference Manual for details on LVD operation.

TIMING

Default timing for the DEMO9S08SF4 is provided by the MC9S08SF4 internal timing source which is active out of RESET. Refer to the MC9S08SF4 Reference Manual for details on configuring the timing source.

COMMUNICATIONS

The MC9S08SF4 does not support serial communications. No board support for this functionality is provided.

USER OPTIONS

The DEMO9S08SF4 includes various input and output devices to aid application development and debug. User I/O includes 2 momentary pushbutton switches, 1 potentiometer, 1 temperature sensor, and 1 piezo buzzer. Each device may be enabled or disabled individually with the USER1 option header. Each user enable is clearly marked as to functionality.

Pushbutton Switches

Two push button switches provide momentary, active-low input, for user applications. Pull-ups internal to the MCU must be enabled to provide error free operation. Pushbutton switches SW1 and SW2 are enabled to the MCU I/O ports by the USER1 option bank. Figure 5 below shows the user jumper settings and MCU connections.

Potentiometer

A 5k ohm, thumb-wheel type, potentiometer at RV1 provides variable resistance input for user applications. The output is the result of a voltage divider that changes as the thumb-wheel is turned. The potentiometer is connected between VDD and GND with the center tap providing the divider output. Figure 5 below shows the user jumper settings and MCU connection.

Temperature Sensor

A surface-mount, NTC thermistor (B = 3900) is installed at location RZ1. This component provides a voltage input to the MCU inversely proportional to temperature. Figure 5 below shows the user jumper settings and MCU connections.

Buzzer

An externally modulated piezo-buzzer, with a center frequency of 2300 Hz for audible applications is applied. A push-pull drive circuit allows the target MCU to easily drive the buzzer. Figure 5 below shows the user jumper settings and MCU connections.

Figure 5: User Option Jumper Settings

Jumper	On	Off	MCU PORT
SW1	Enable SW1	Disable SW1	PTA2/KBIP2/TPM1C0/FDSOUT0
SW2	Enable SW2	Disable SW2	PTA3/KBIP3/TPM1C1/FDSOUT1
BUZZ	Enable BUZZ	Disable BUZZ	PTB0/TMP2CH0/FDSOUT6
POT	Enable POT	Disable POT	PTC0/SCL/ADC6
TEMP	Enable TEMP	Disable TEMP	PTC1/SDA/ADC7

PTB0_SEL

The Fault Detect and Shutdown Output 6 (FDSOUT6) is applied to 5 separate locations on connector J1. The PTB0_SEL option header allows the user to select the desired location for use. Refer to the MC9S08SF4 Reference Manual for details on use and configuration of the Fault Detect and Shutdown module. Figure 6 below shows the connections for thePTB0_SEL option header.

Figure 6: PTB0_SEL Option Header

■■		1	Select PTB0_A (J1-13)
●	●	2	Select PTB0_B (J1-15)
●	●	3	Select PTB0_C (J1-17)
●	●	4	Select PTB0_D (J1-19)
●	●	5	Select PTB0_E (J1-33)

MCU I/O PORT

The MCU I/O PORT connector provides access to the MC9S08SF4 I/O signals. **Error! Reference source not found.** below show the pin-out for the MCU I/O connector.

Figure 7: MCU I/O PORT – J1

VDD	1	2	PTA0/KBI0/TCLK/IRQ
VSS	3	4	PTA1/KBI1/RESET
PTC0/SCL/ADC6	5	6	PTB7/BKGD/MS
PTC1/SDA/ADC7	7	8	
PTA2/KBI2/TPM1C0/FDSOUT0	9	10	PTB1/ACMP5/ADC0
PTA3/KBI3/TPM1C1/FDSOUT1	11	12	PTB2/ACMP4/ADC1
PTB0_A	13	14	PTB3/ACMP3/ADC2
PTB0_B	15	16	
PTB0_C	17	18	PTB4/ACMP2/ADC3
PTB0_D	19	20	PTB5/ACMP1/ADC4
PTC0/SCL/ADC6	21	22	PTB6/ACMP0/ADC5
PTC1/SDA/ADC7	23	24	
	25	26	PTC1/SDA/ADC7
	27	28	PTC0/SCL/ADC6
	29	30	PTA4/TPM1C2/FDSOUT2
	31	32	PTA5/TPM1C3/FDSOUT3
PTB0_E	33	34	PTA6/TPM1C4/FDSOUT4
	35	36	PTA7/TPM1C5/FDSOUT5
	37	38	
	39	40	