SGTL5000 Evaluation Platform

User's Guide

v2.0.0

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1. SCOPE

The evaluation platform is designed to allow the user to test the features and performance of the SGTL5000 audio codec. The evaluation board can be used as a demo or development platform.

SGTL5000 is an audio codec that utilizes two analog inputs (LINEIN and MIC IN), two analog outputs (LINEOUT and HPOUT), one digital input (I2S IN) and one digital output (I2S OUT). Communication to the chip is performed through either I2C or SPI. SGTL5000 comes in 2 packages: 3x3mm 20-pin QFN, and 5x5mm 32-pin QFN. The information in this document applies to both packages.

2. GETTING STARTED

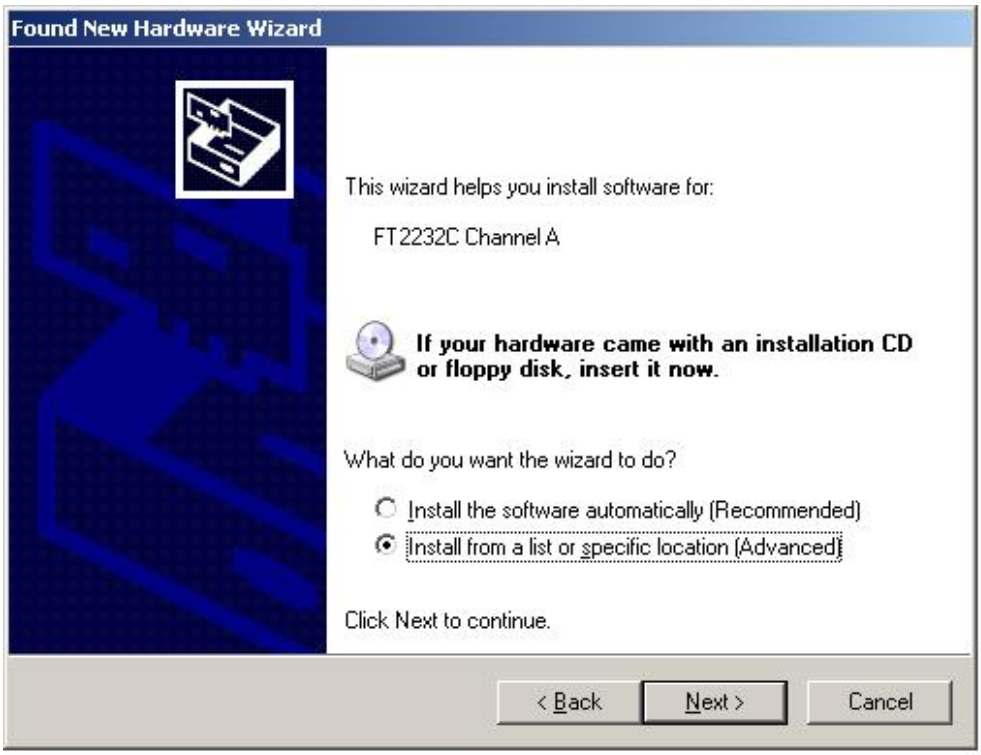
2.1. Software Installation

- Copy the following from the CD to any location on your hard drive:
  - StereoCodecControlSoftware.exe
  - FTC Drivers folder
- Copy SGTL5000_CA1_Init_Script.txt from the CD to C:\ drive (directly to C:).

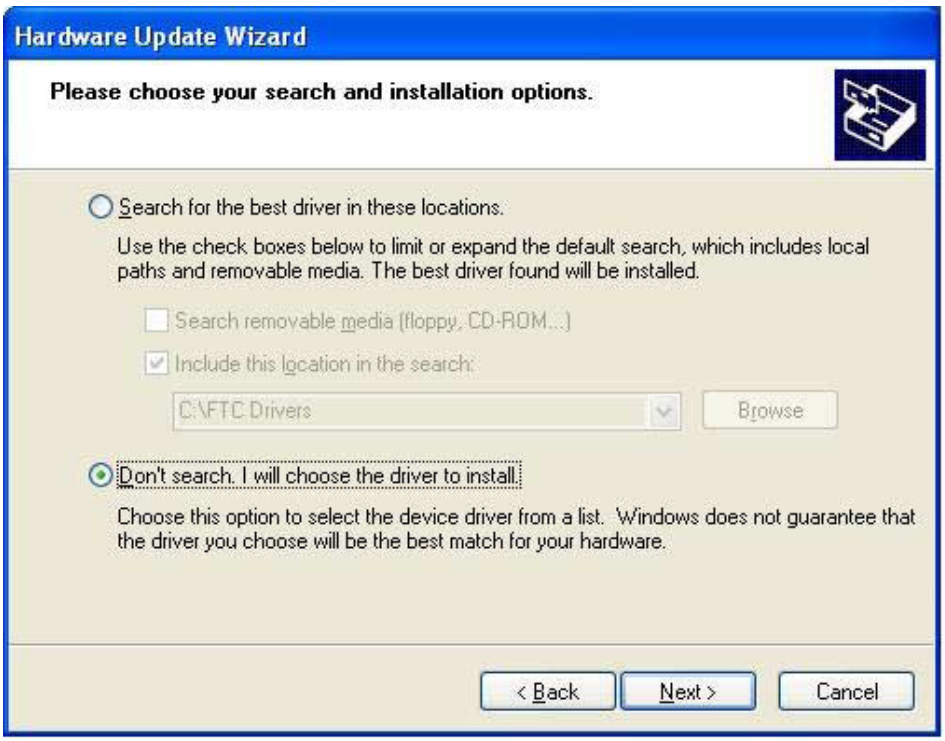
2.2. USB Driver Installation

- Make sure that the evaluation board jumpers are configured correctly (refer to section 3.1). The jumpers are pre-configured before shipping so that the board is ready to be used.
- Connect the USB cable from the PC to the board.
- Connect the 5V power supply to the board and turn on the board.
- Windows will detect the new device and automatically launch the "**Add Hardware Wizard**"

- Select option **"Install from a list or Specific Location (Advanced)"** and click **Next**.

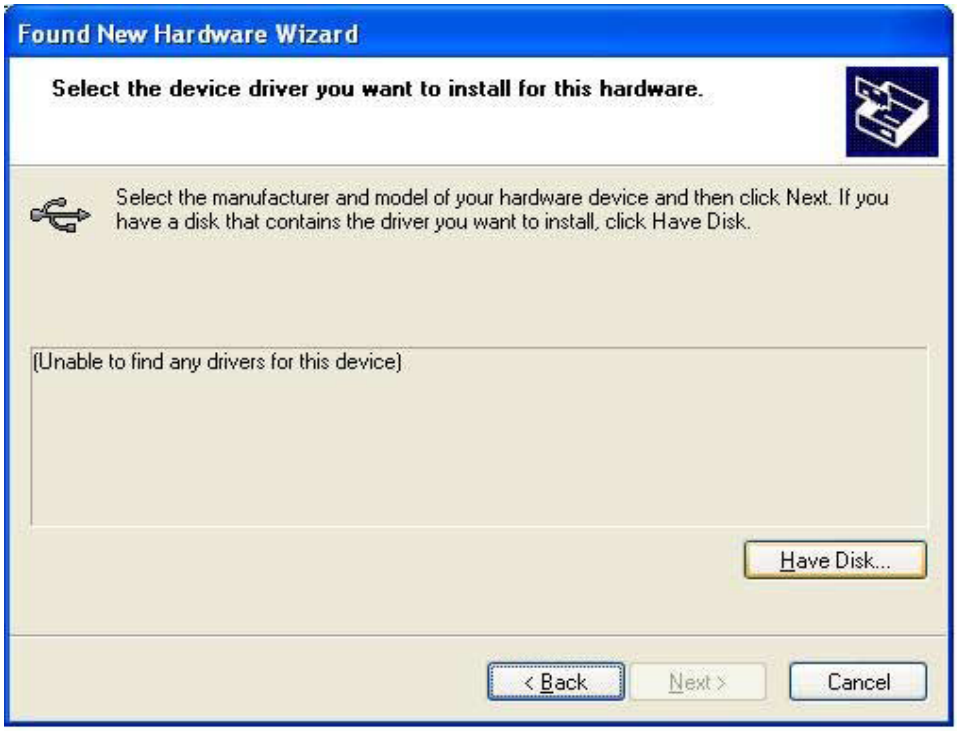


- Select option **"Search for the best driver** in **these locations"** and select **"Don't Search. I will choose the driver to install".** Click on **Next**.

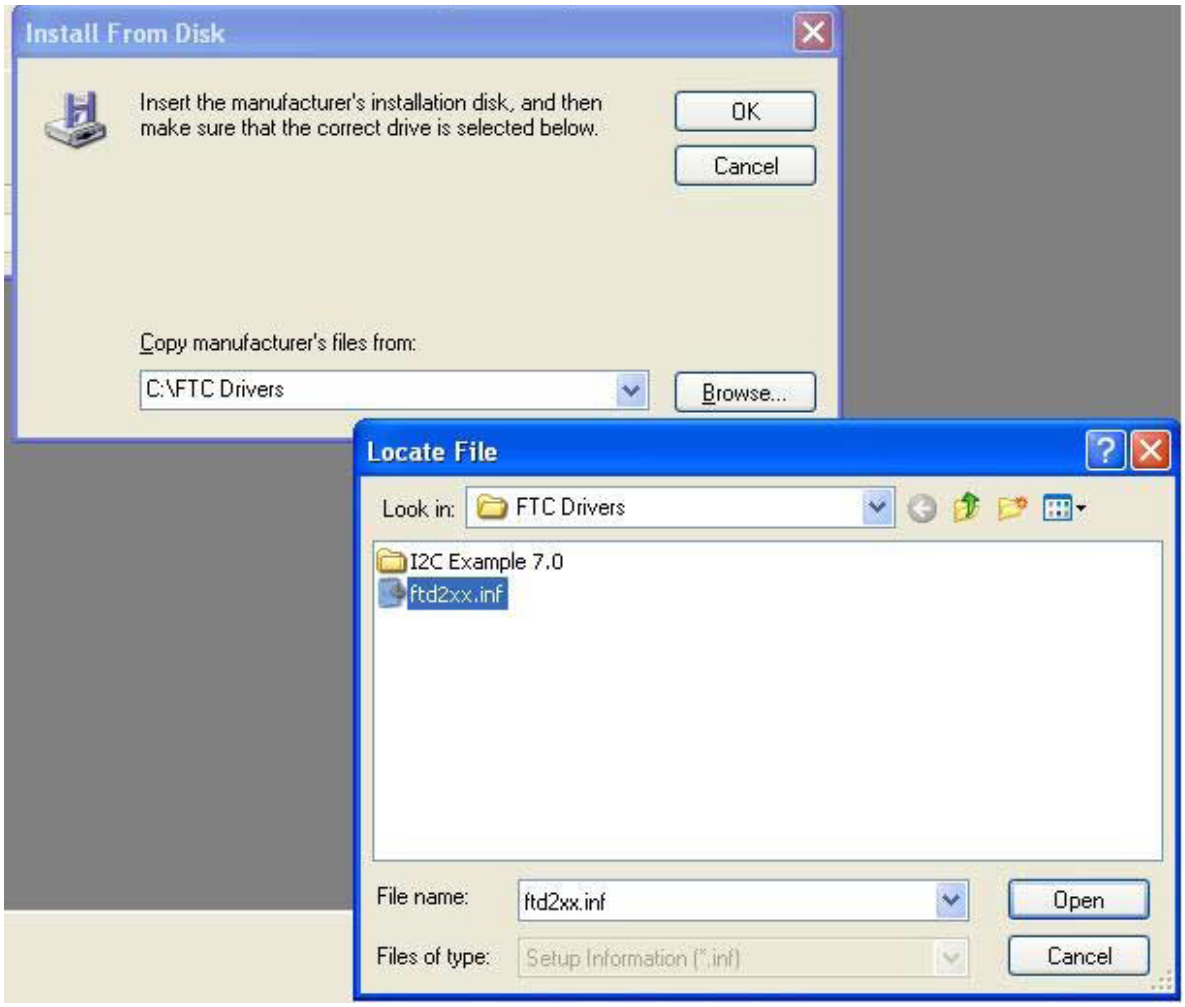


- Select "**Universal Serial Bus Controllers**" from the list.

- Select on "**Have Disk**".



- Browse to "**FTC Drivers**" folder unzipped from the **SGTV58XXControl.zip** and select "**ftd2xxx.inf**" file. Click "**Open**". Click "**Next"** in the next window.



- Windows will now detect the device **FT2232C Channel A**. Windows logo testing window will pop-up. Click **Continue Anyway**.

- **FT2232C Channel B** will be detected next. Windows logo testing window will pop-up. Click **Continue Anyway**.
- Now your eval board is ready to be used.

3. BOARD SETUP PROCEDURE

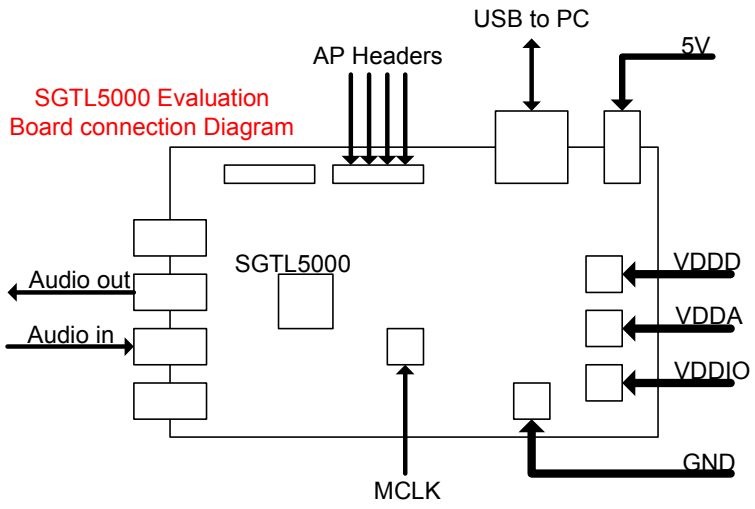
3.1. Jumper Options

SGTL5000 Evaluation Board provides users with various stuffing options in order to use different features of the board.

- **External power (JP3, JP4, JP5):** Jumper pins 1, 2 to use external voltage source using banana plugs for each rail. Jumper pins 2, 3 to use internal regulators
- **MCLK Source (JP2):** Jumper pins 1, 4 to use onboard oscillator. Jumper pins 2, 5 to use external MCLK via SMB connector (J10). Jumper pins 3, 6 to use MCLK provided by an Audio Precision PSIA via I2S Headre (J2)
- **MIC select (JP1):** Jumper pins 1, 2 for onboard microphone (X1). Jumper pins 2, 3 to use microphone jack (J6)

3.2. Board Connections

The following connection may be used as a guide.



3.3. Example Setup

- Connect power and input/outputs according to the aforementioned connections jumper settings and connection diagram
- Open Audio Precision software
  - Set up digital i/o for PSIA, and configure for I2S frame clock and bit clock output, and MCLK out
- Open SGTL5000 control software
  - Select I2C connection type, hit Connect
  - Select 256*Fs, 48kHz, Slave mode. Hit initialize
  - Configure an I2S input to DAC and I2S outputs
  - Select Program Route
  - Unmute DAC output
- Perform any necessary testing

4. HARDWARE

4.1. Evaluation Board Features

- SGTL5000 Audio Codec
- LINEIN RCA analog input jack
- LINEOUT RCA analog output jack
- Selectable mini-jack or onboard microphone input
- Stereo headphone mini-jack analog output, with optional capless design cir cuitry
- Two-row headers for buffered I2S digital input/output
- Support for onboard or external MCLK source
- USB to I2C/SPI communication port
- 5V input voltage through either internal LDO regulators, or external individual supplies

4.2. Evaluation Board Layout

The following shows the physical layout and placement of components of the SGTL5000 evaluation board. (Please note that the picture shown below is for SGTL5000 32QFN evaluation board. SGTL5000 20QFN evaluation board is blue in color. The information in this document applies to both SGTL5000 packages)

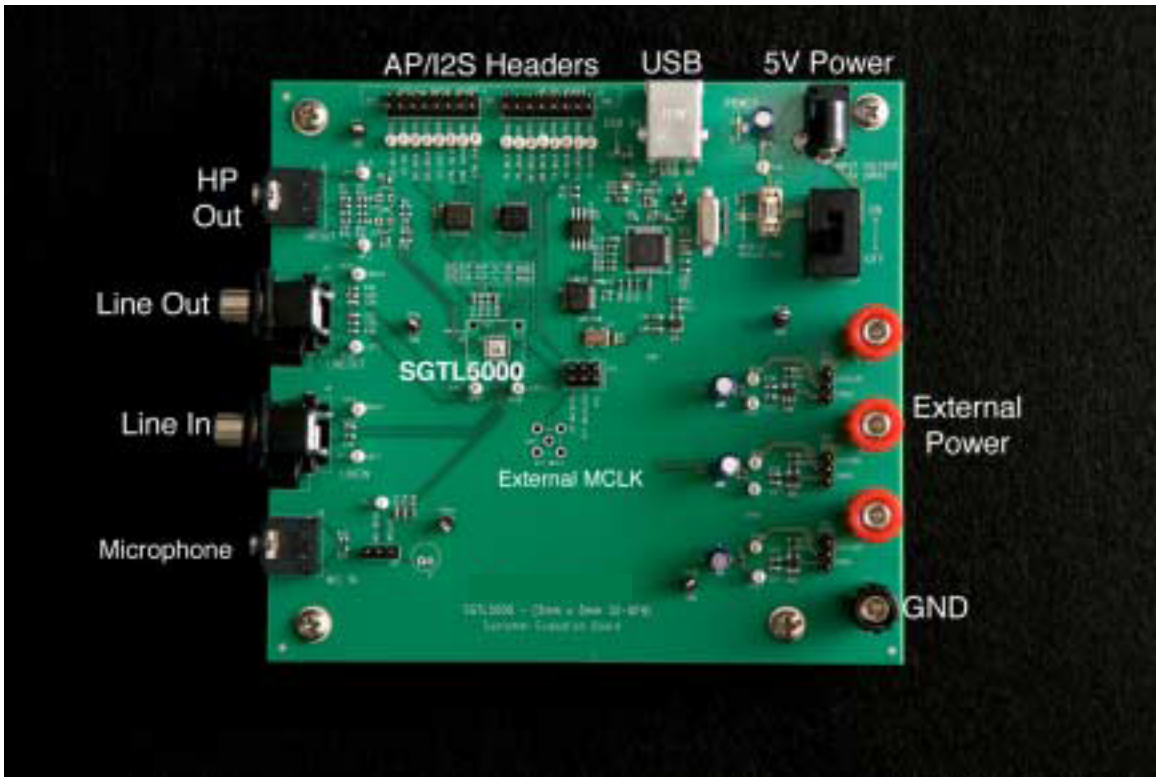


Figure 1. SGTL5000 Evaluation Board with Components Identified

- Inputs include one RCA connector for LINEIN, and one mono microphone input 3.5mm mini-jack for external MIC. The board also has anan be either 3.5mm mini-jack or on-board microphone.
- Outputs include one RCA connector for LINEOUT, and one stereo 3.5mm mini-jack for HP OUT.
- AP I2S headers are a 2x8 pin array for Audio Precision PSIA connectors. These headers are provided to connect Audio Precision's frame clk, bit clk, master clk and data to the chip.
- USB jack to connect the board to the PC via a USB cable. The software sends commands to the board via USB and the FTDI chip on the board converts it to I2C/SPI to talk to the chip. The FTDI chip is powered by the USB and a green LED indicates that.
- 5V power is a 2.1mm positive-center connector for the 5V wall-wart supply provided with the kit. When the power switch is turned on, a blue LED indicates that the board is powered on.
- Individual external power can be supplied to the board via either bare wires, or banana-type connectors
- MCLK is supplied via I2S header, onboard oscillator, or SMB connector.

4.3. Power linear regulators

If only a 5V board power supply is connected, the supplies for VDDD, VDDA, and VDDIO must be switched to use the onboard regulators. These regulators are Analog Devices ADP1712AUJZ.

By default, the regulator outputs are as follows:

Power Rail	Output Voltage (V)
VDDD	1.8
VDDA	1.8
VDDIO	3.3

Table 1. Linear regulator output voltages

The output for each regulator is determined by the formula

$V^{OUT} = 0.8\ V\ (1 + R1/R2)$

where:

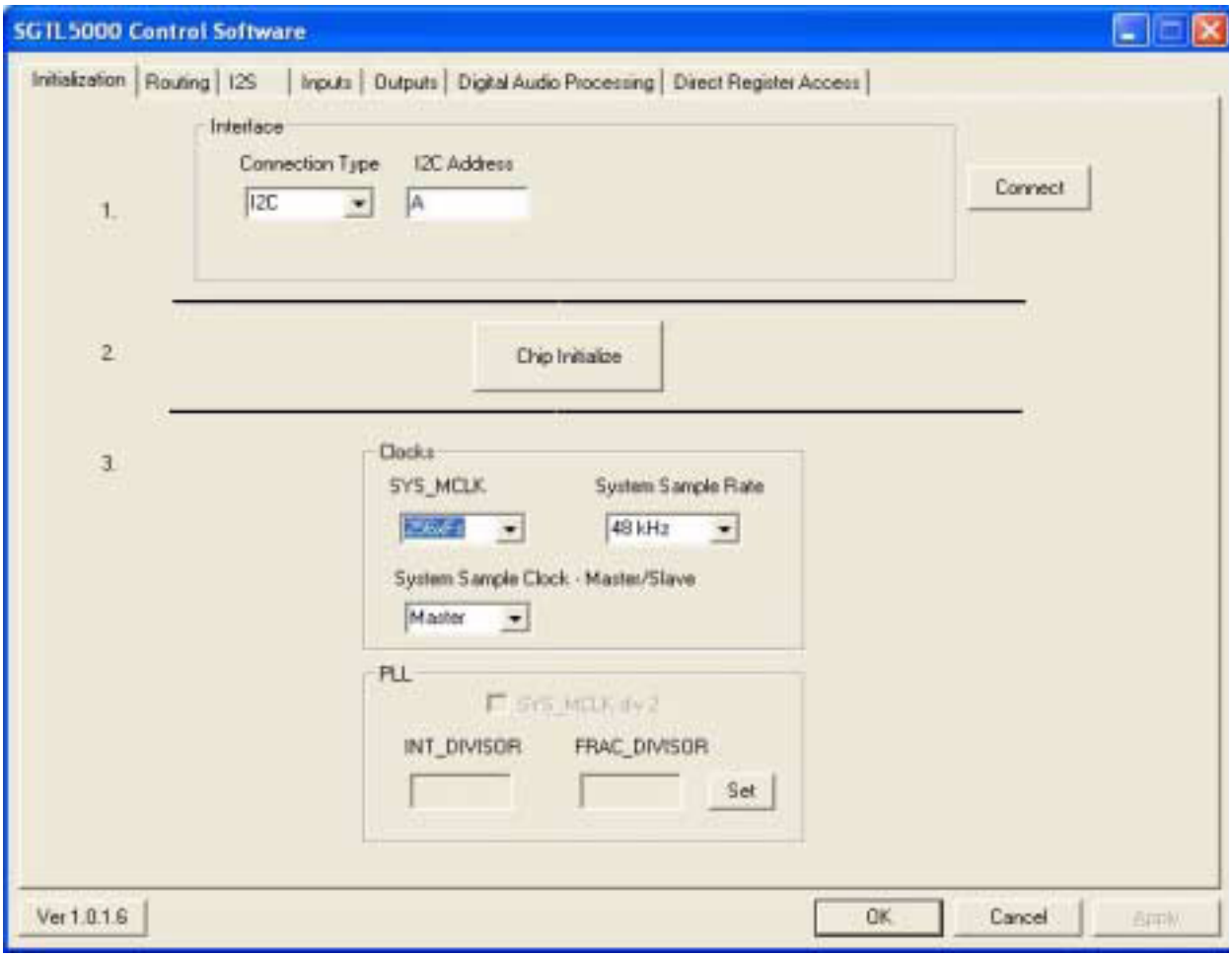
R1 is the resistor from OUT to ADJ.

R2 is the resistor from ADJ to GND.

5. SOFTWARE

The SGTL5000 Control Software allows a user access to all of the features within SGTL5000.

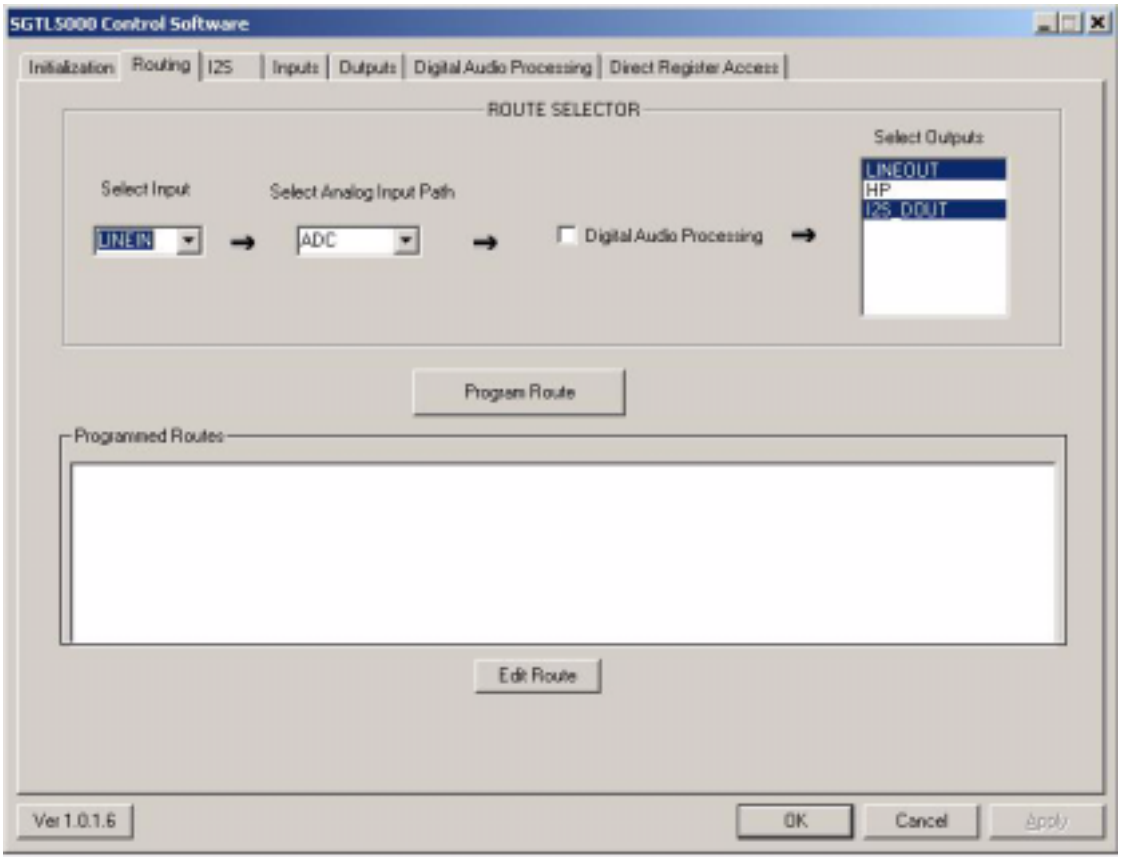
5.1. Initialization



- From the Initialization tab, the user selects the communication protocol to interface with the SGTL5000 chip - I2C or Ethernet. Click ‘Connect’ to connect to the board.
- Click on ‘Chip Initialize’. This will power up the analog and digital blocks, setup the default clocks (as shown in the clocks section of the Initialization page), and unmute the ADC and outputs.
- Clock configuration can be done on this page as well. The ‘Chip Initialize’ already sets it up in the default state. So additional configuraiton is required unless the parameters need to be changed. From the SYS_MCLK menu, PLL can be chosen if needed. If used, the PLL must be powered up by direct write under Direct Register Access page and the INT_DIVISOR/FRAC_DIVISOR divisors need to be programmed correctly. Please refer to the datasheet on how to

configure the PLL. Please note that the divisors must be calculated based on the external MCLK rate.

5.2. Routing

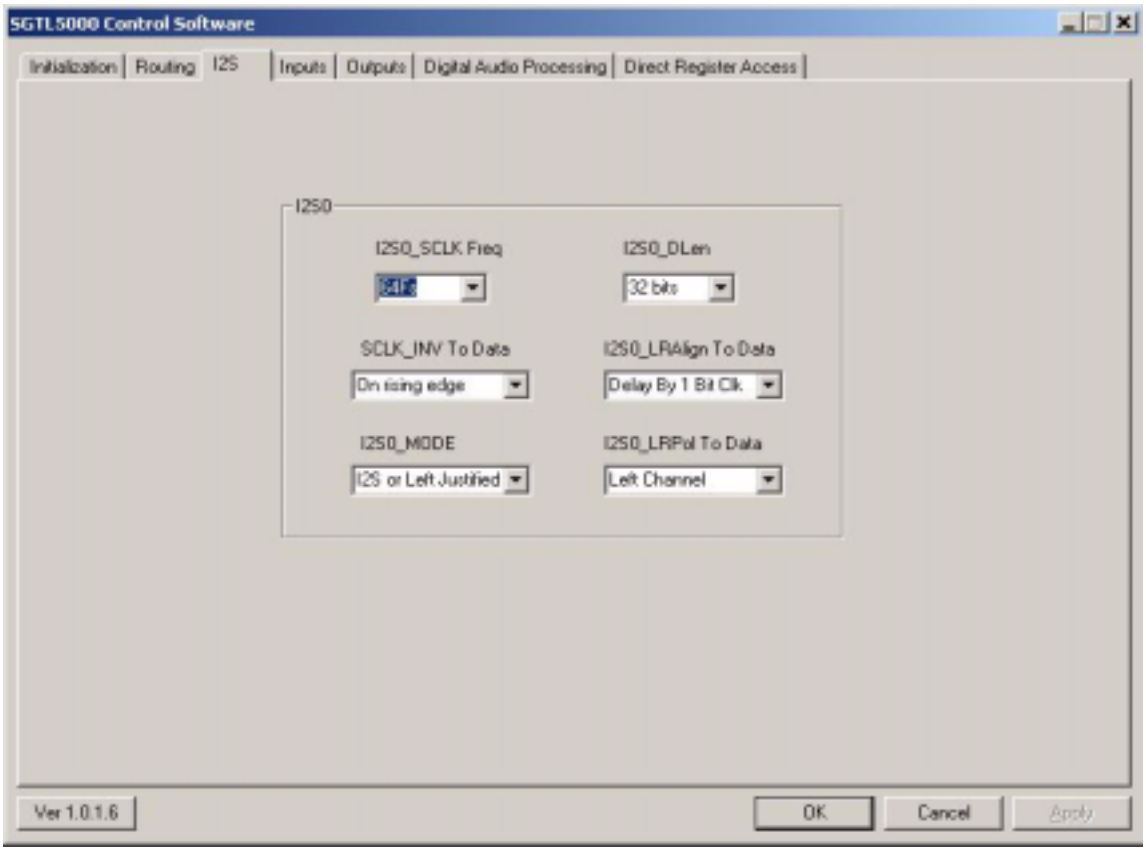


From the Routing page, various signal paths are set from input to output.

- Inputs include: LINEIN, MIC, I2S_DIN
- LINEIN or MICIN may be configured through the ADC or directly pass-through to HP_OUT.
- Outputs include: LINEOUT, Headphone (HP), I2S_DOUT
- Routes may or may not include the use of the Digital Audio Processor (DAP). Please note that when DAP is routed, it must also be enabled under the Digital Audio Processor page. Otherwise, no audio will pass through DAP.

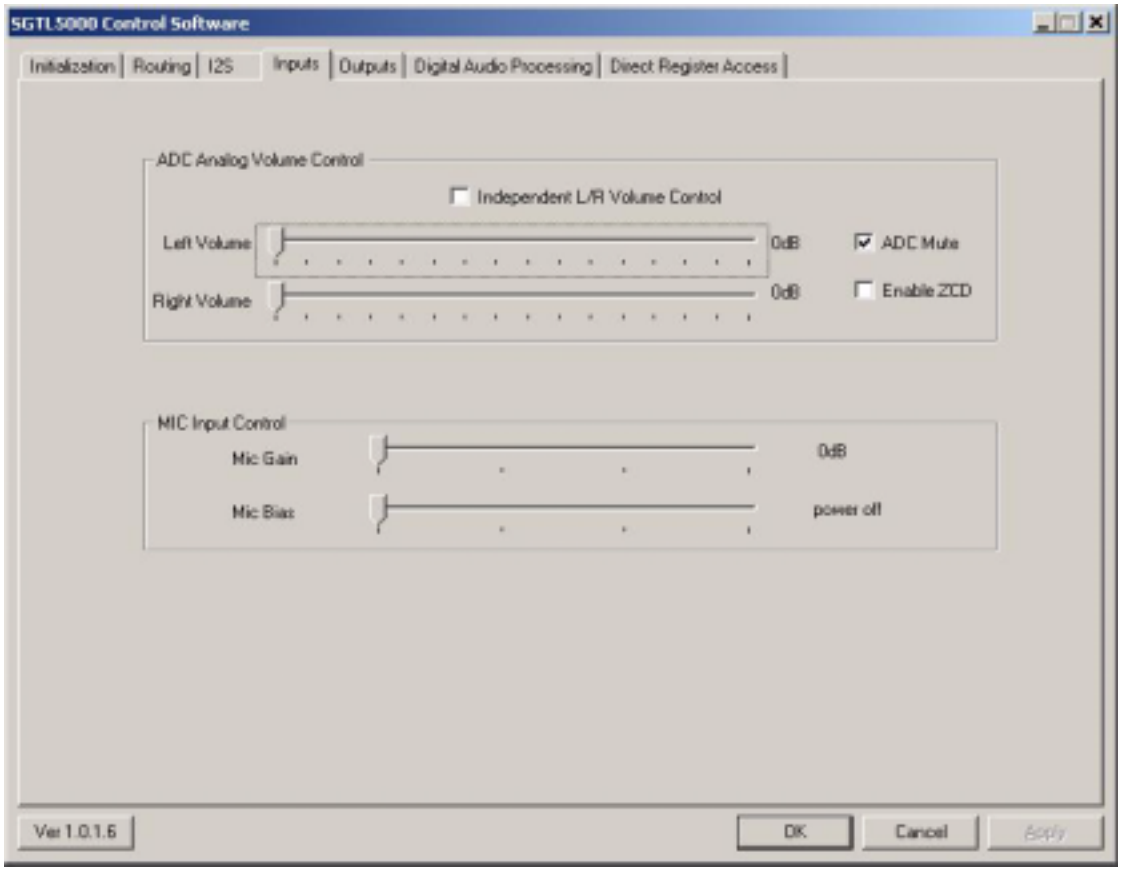
Routes may also be edited once programmed. To do so, select the route that is to be edited, press the "Edit Route" button, make the route changes, and select "Program Route."

5.3. I2S



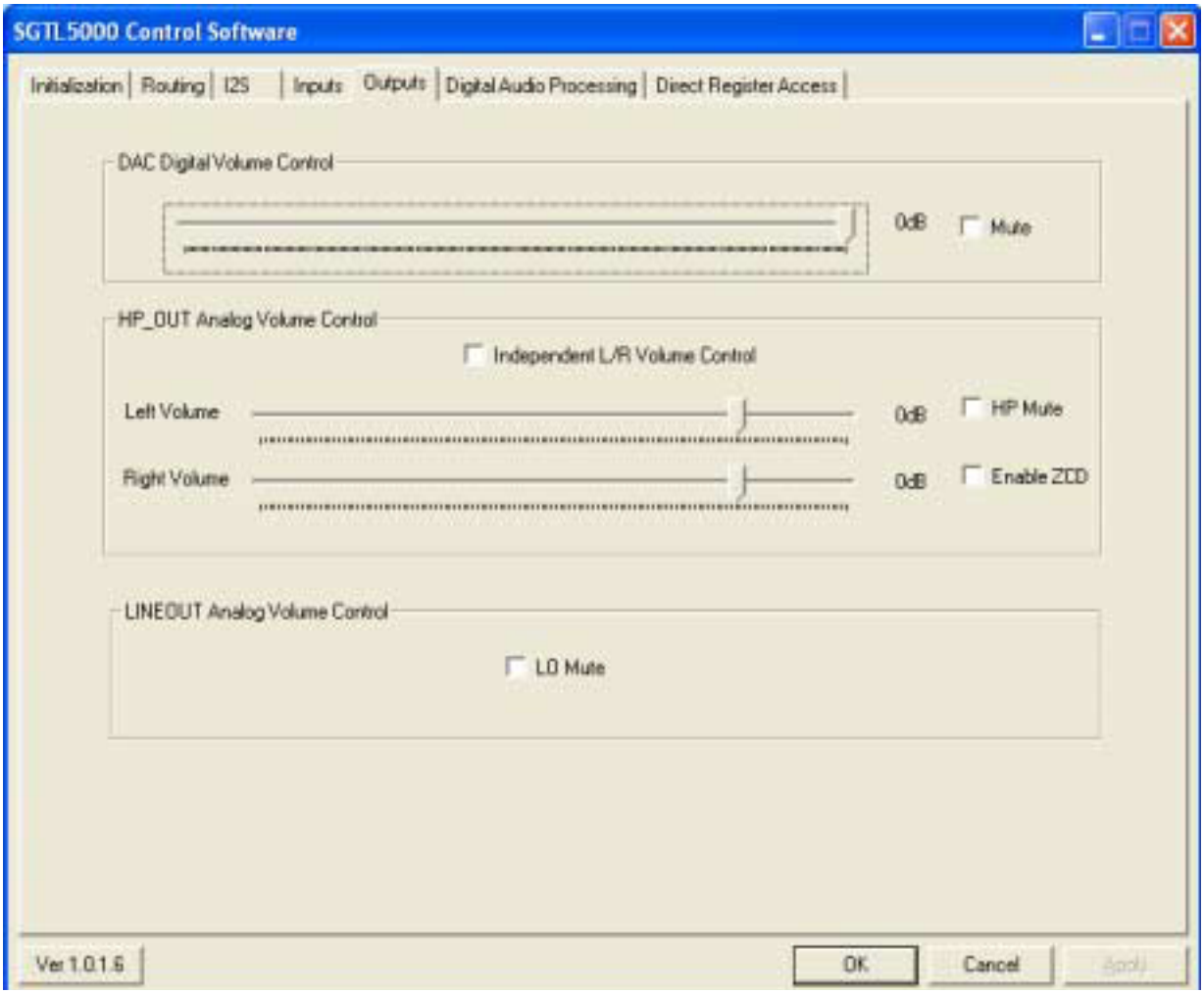
From the I2S tab, specifics to the digital I2S communication are programmed. The SCLK frequency, word length, and data alignment are options that are programmable.

5.4. Inputs



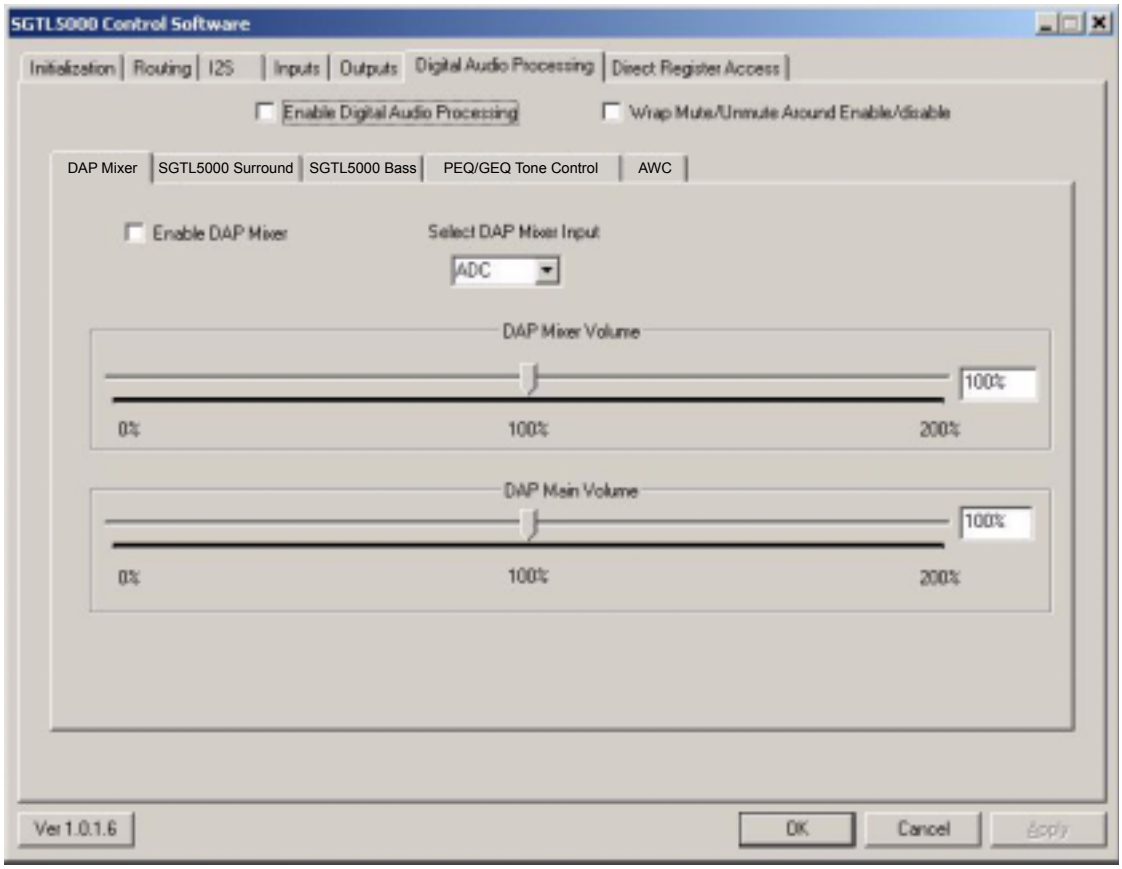
- The input screen has the volume and gain controls for the two analog inputs - Line In and Microphone.
- The software configures the left and right volume together to the same value. When ‘Independent L/R Volume Control’ is checked, left and right volumes can be controlled indepndently. The left and right channels also have independent mutes.
- The microphone has two sliders for Gain and Bias, the latter is dependent on on-board settings of the Mic Bias circuitry.

5.5. Outputs



- The output tab has controls for DAC digital volume, HP OUT analog volume/ mute and LINEOUT mute/unmute.

5.6. Digital Audio Processing (DAP)



5.6.1. DAP Mixer

The DAP Mixer allows a second audio signal to be mixed in with the main audio stream. Both can be mixed as a percentage of total signal. The Mixer can be configured to route from the ADC or I2S_DIN.

5.6.2. SGTL5000 Surround

SGTL5000 Surround widens the soundscape, and has width settings from 1-7, for varying amounts of processing.

5.6.3. SGTL5000Bass Enhance

SGTL5000 Bass Enhance boosts bass levels. Programmable settings include the low pass filter cutoff frequency, high pass filter cutoff frequency, Bass Level, Left/Right level, and a multiplier that can dramatically increase the effect.

5.6.4. PEQ/GEQ/Tone Control

SGTL5000 includes a 7-band parametric equalizer (PEQ) that can be programmed through the software's presets. Custom PEQ curves can be created, as well.

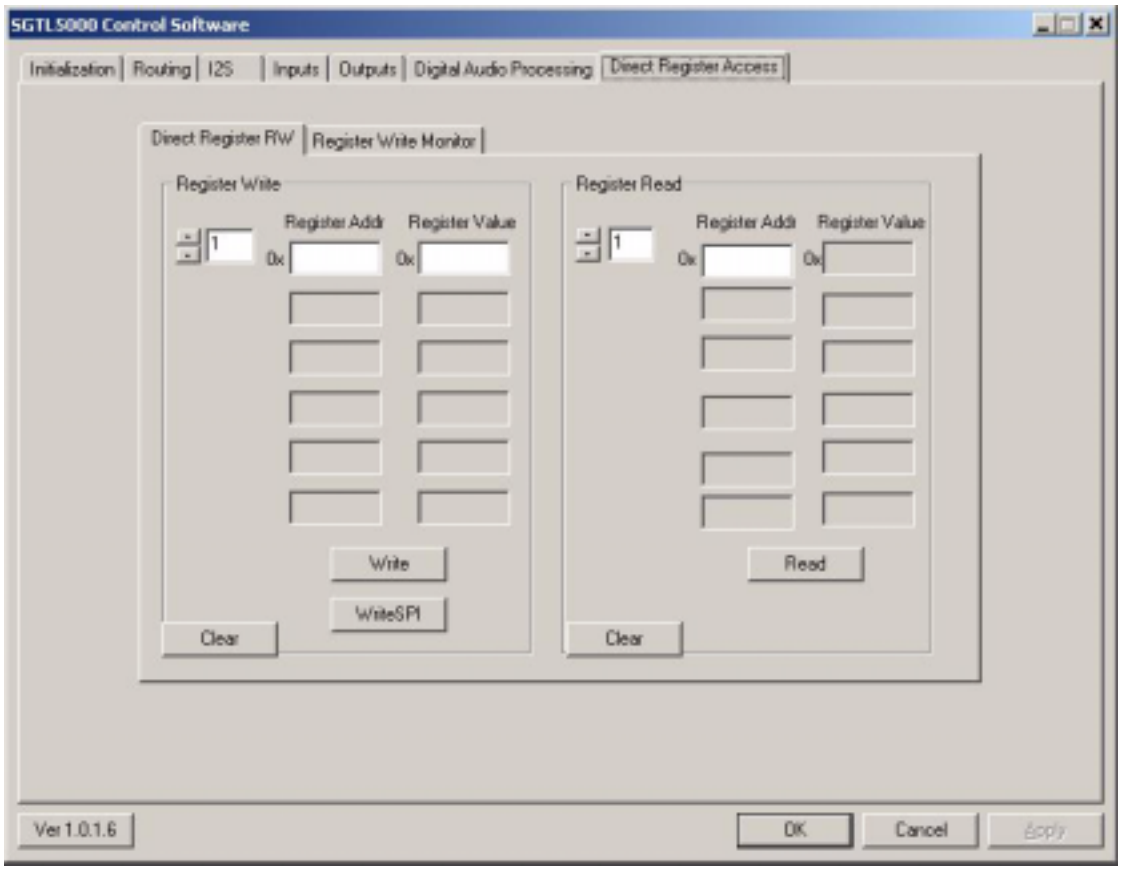
The 5-band graphic equalizer (GEQ) is fully programmable, with bands of 115Hz, 330Hz, 990Hz, 3000Hz, and 9900Hz. Each can be adjusted up to +/-12dB.

Tone Control allows the user to adjust the Bass and Treble levels, up to +/-12dB.

5.6.5. AVC

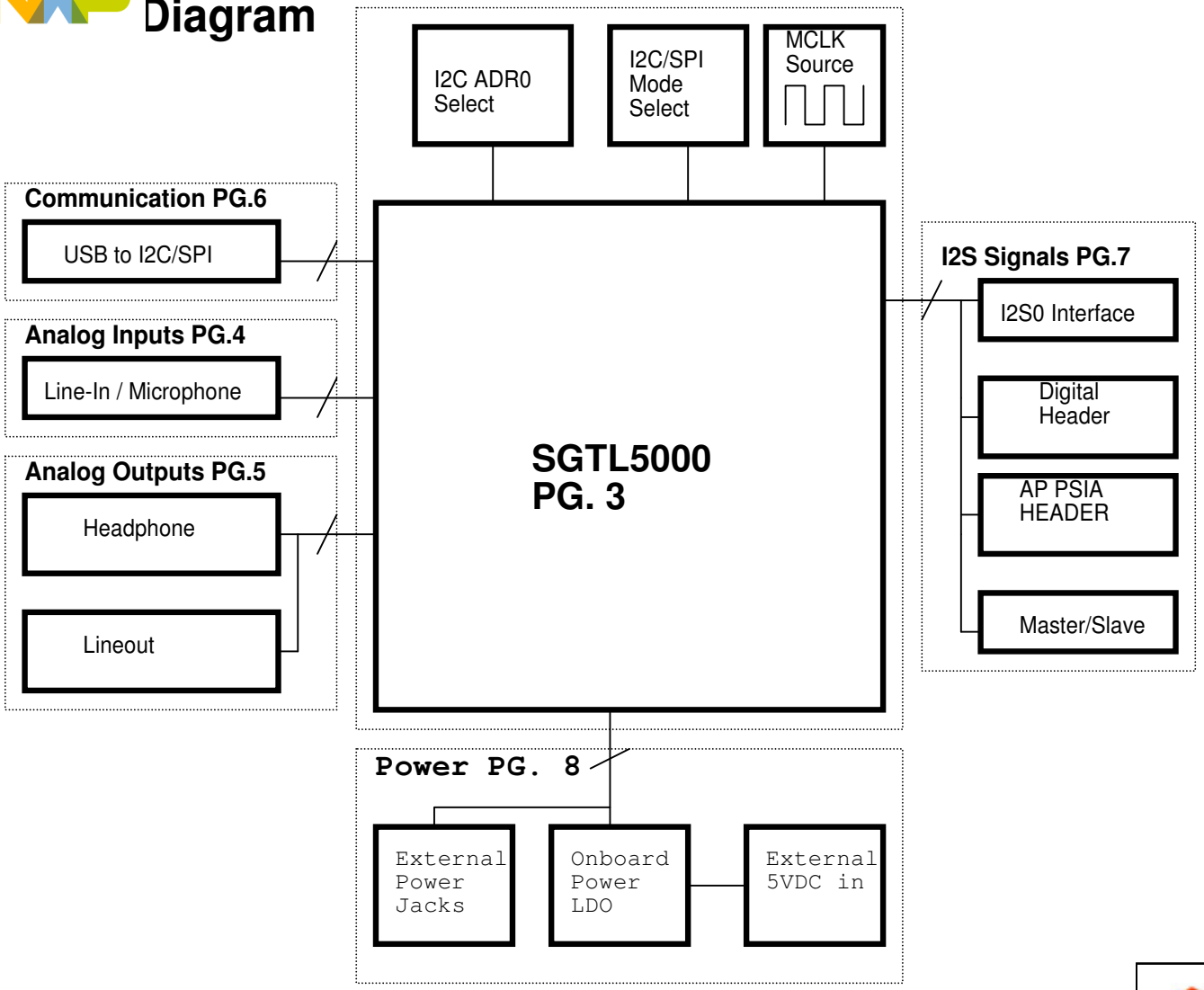
The Automatic Volume Control (AVC) helps prevent clipping or speaker damage by allowing the user to set a threshold from which SGTL5000 will attenuate or gain the signal to reach the specified value. Attack and decay rates are fully programmable.

5.7. Direct Register Access



- From the Direct Register Access tab, users can read and write directly to registers without the use of the GUI.
- The Register Write Monitor shows all read and written-to registers from the current session. Scripts can be saved and run from here as well.
- Support for SPI register writes is on this tab.

Diagram



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KITSGTL5000EVBE

Page Title:

Block Diagram - 32-Pin QFN, 5x5 Package

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Set

1. JP1 to select SYS_MCLK
2. JP2 to select on-board MIC or external MIC_IN
3. JP3~JP5 to setect between external and on-board power supply

Revision:

A) - Initial Release

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Feature Set

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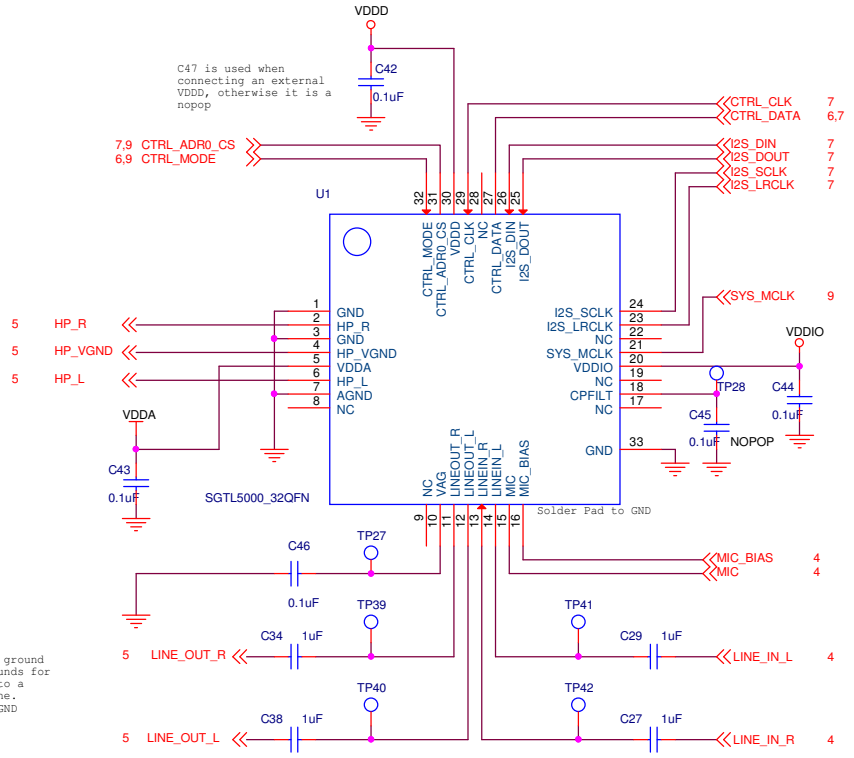

Notes:

- Star the ground pins of the chip, the ground connection for the VAG cap, and the grounds for the line-in's, line-out's, HP, and mic to a single point and then to the ground plane.
- Use short and fat traces for the HP_VGND

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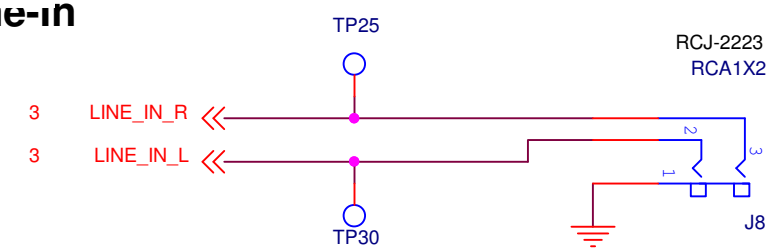
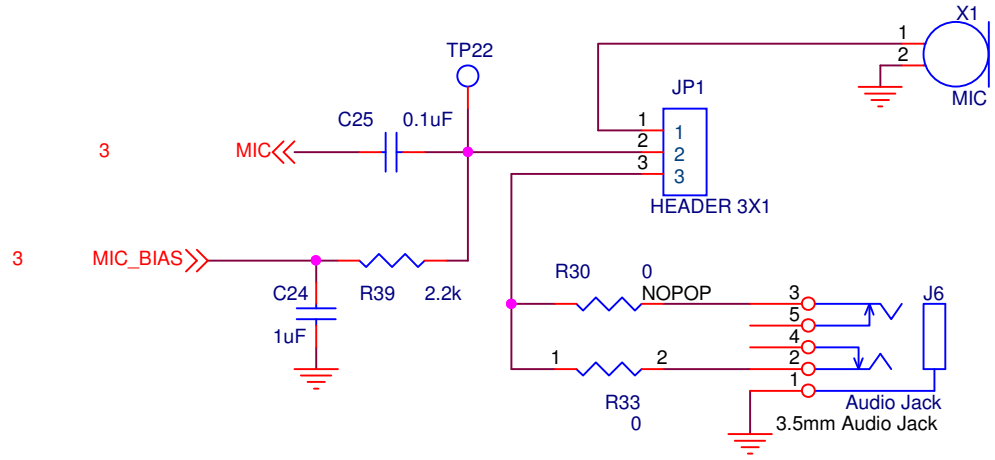
Line-In



MIC

Microphone input with MIC_BIAS derived internally.



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Analog Inputs

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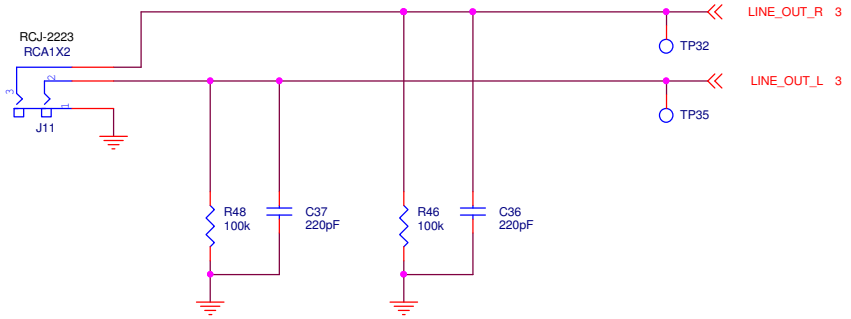
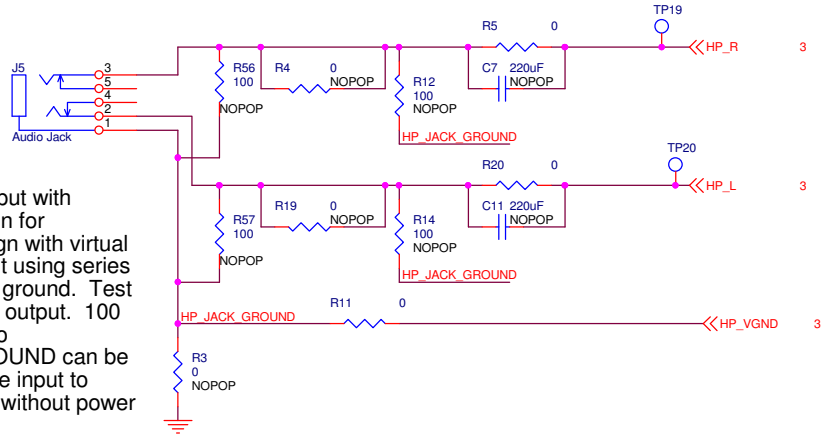


Headphone Out



Headphone output with population option for CAPLESS design with virtual ground or output using series CAP and board ground. Test filters shown on output. 100 Ohm resistors to HP_JACK_GROUND can be used to minimize input to output coupling without power applied.

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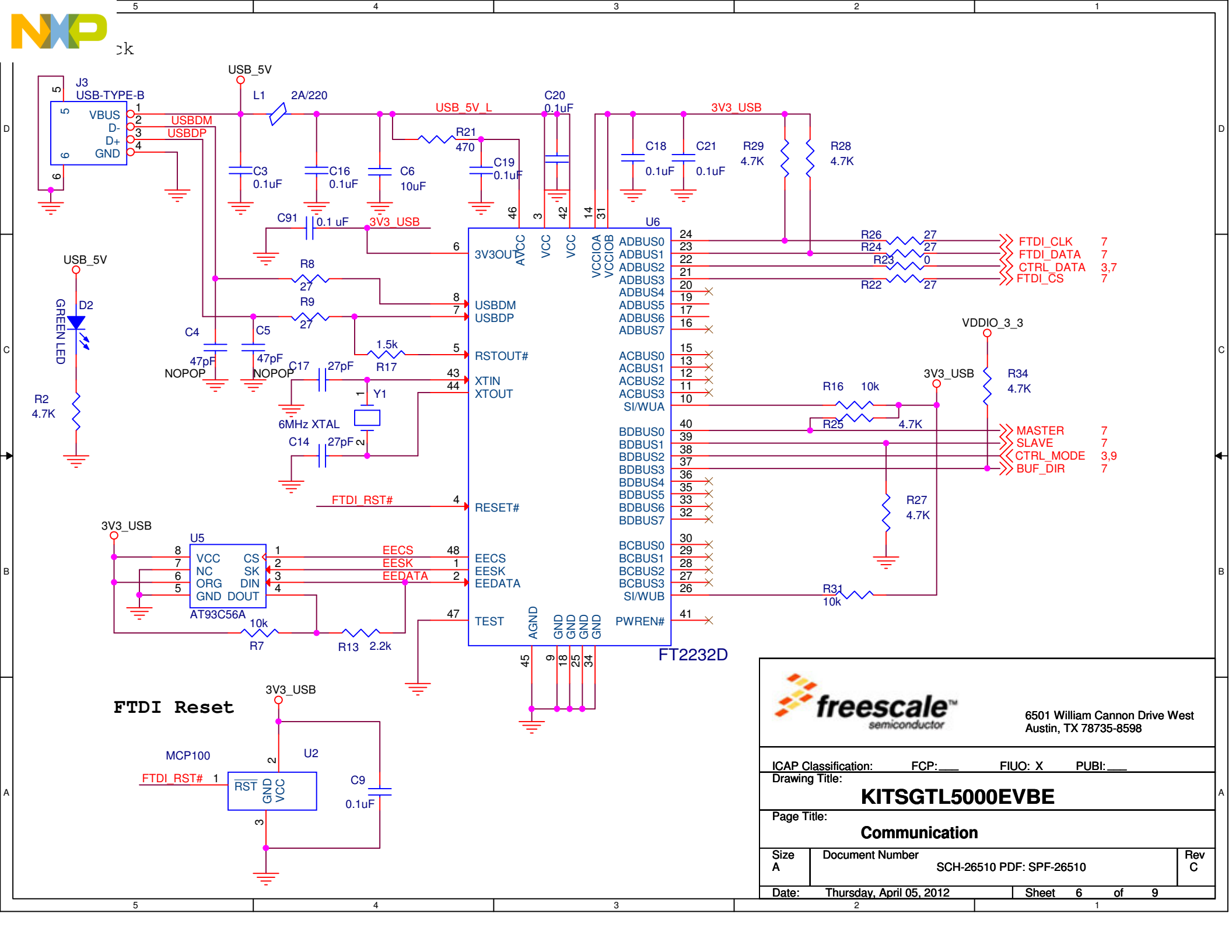
J3
USB-TYPE-B
VBUS
D-
D+
GND
USB_5V
L1
2A/220
USBDM
USBDP
USB_5V_L
C20
0.1uF
3V3_USB
R21
470
C3
0.1uF
C16
0.1uF
C6
10uF
C19
0.1uF
C18
0.1uF
C21
0.1uF
R29
4.7K
R28
4.7K
C91
0.1 uF
U6
3V3OUT
AVCC
VCC
VCCIOA
VCCIOB
ADBUS0
ADBUS1
ADBUS2
ADBUS3
ADBUS4
ADBUS5
ADBUS6
ADBUS7
R26
R24
R23
R22
FTDI_CLK
FTDI_DATA
CTRL_DATA
FTDI_CS
D2
GREEN LED
R8
27
R9
27
USBDM
USBDP
C4
47pF
NOPOP
C5
47pF
NOPOP
1.5k
R17
RSTOUT#
C17
27pF
XTIN
XTOUT
Y1
6MHz XTAL
C14
27pF
R2
4.7K
VDDIO_3_3
R34
4.7K
R16
10k
R25
4.7K
ACBUS0
ACBUS1
ACBUS2
ACBUS3
SI/WUA
BDBUS0
BDBUS1
BDBUS2
BDBUS3
BDBUS4
BDBUS5
BDBUS6
BDBUS7
MASTER
SLAVE
CTRL_MODE
BUF_DIR
R27
4.7K
FTDI_RST#
RESET#
U5
VCC
NC
ORG
GND
CS
SK
DIN
DOUT
AT93C56A
EECS
EESK
EEDATA
R7
10k
R13
2.2k
BCBUS0
BCBUS1
BCBUS2
BCBUS3
SI/WUB
R31
10k
TEST
PWREN#
AGND
GND
FT2232D
FTDI Reset
MCP100
U2
RST
GND
VCC
C9
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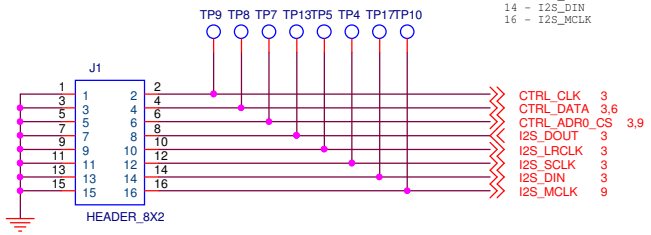
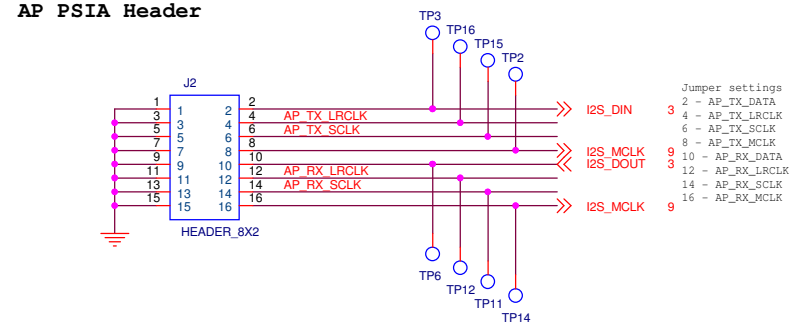
Jumper settings
2 - I2C_CLK
4 - I2C_DATA
8 - I2S_DOUT
10 - I2S_LRCLK
12 - I2S_SCLK
14 - I2S_DIN
16 - I2S_MCLK



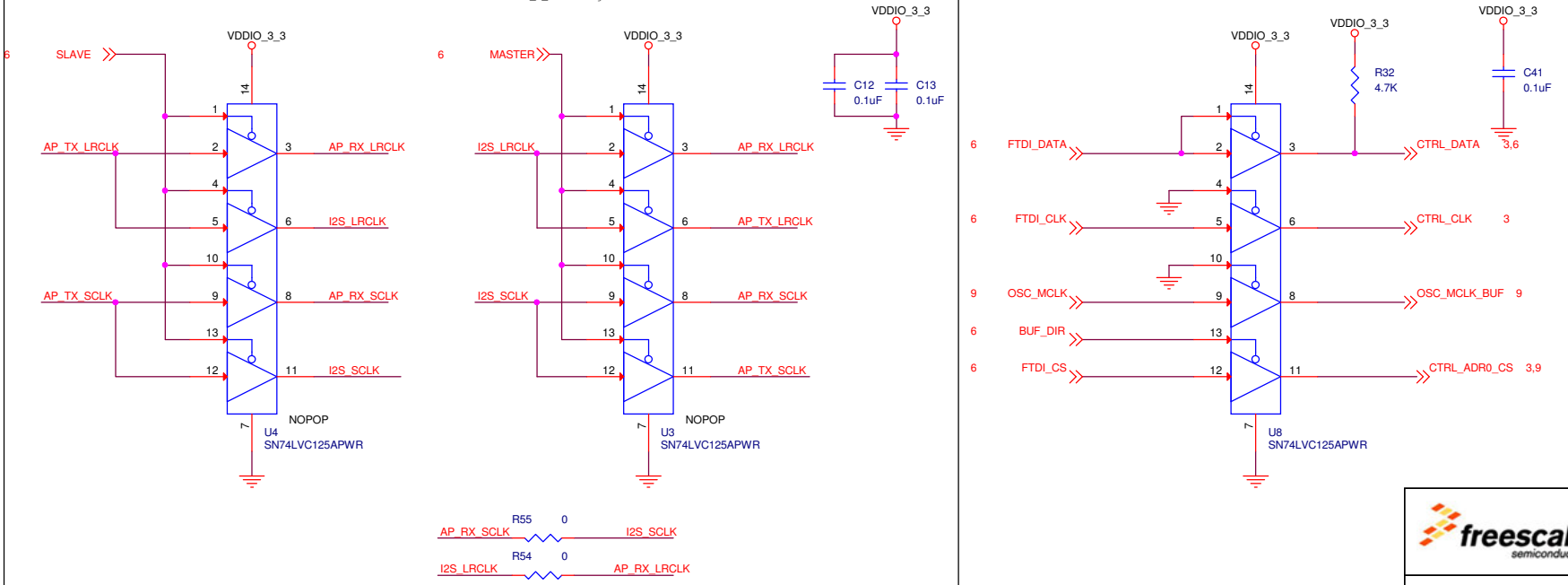
AP PSIA Header



Jumper settings
2 - AP_TX_DATA
4 - AP_TX_LRCLK
6 - AP_TX_SCLK
8 - AP_TX_MCLK
10 - AP_RX_DATA
12 - AP_RX_LRCLK
14 - AP_RX_SCLK
16 - AP_RX_MCLK

Master/Slave modes

AP PSIA level must match
VDDIO_3_3 setting



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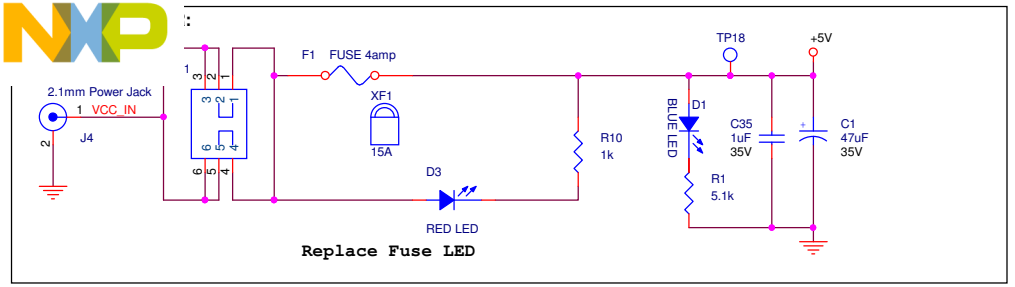
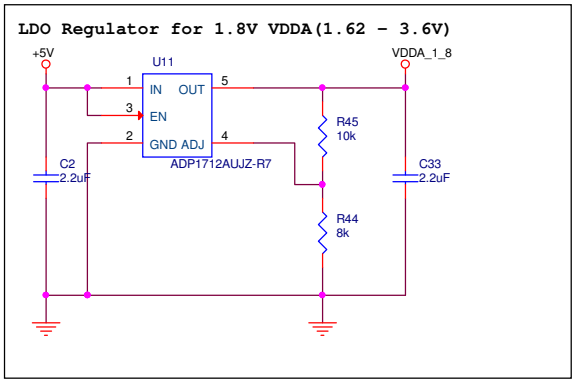
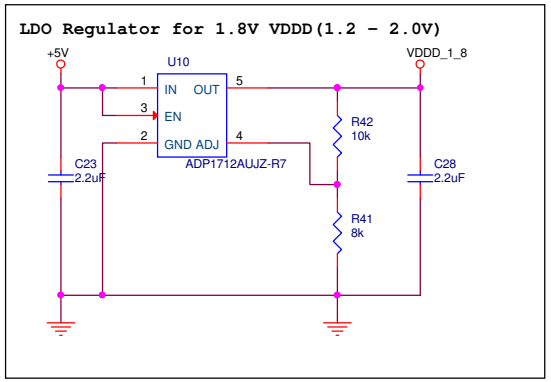
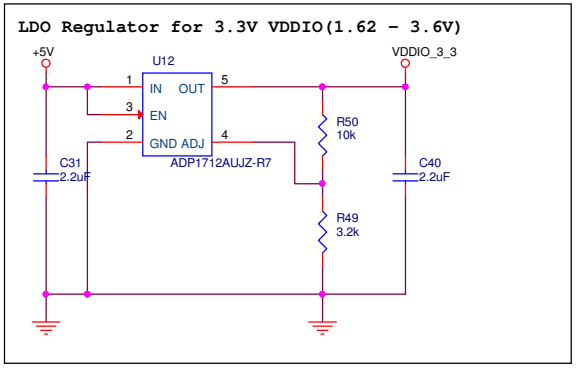
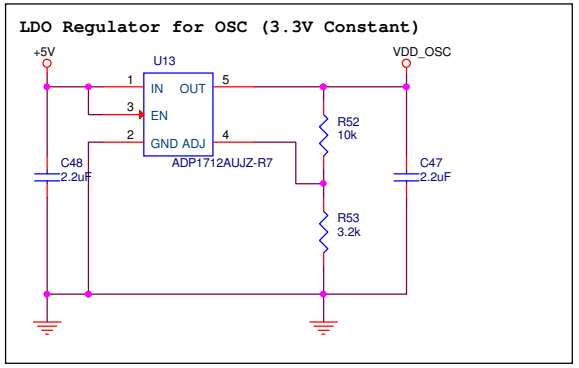


Select either External Power by tying Pins 1 and 2 together, or Internal Power by tying Pins 2 and 3 together on JP3, 4, 5.

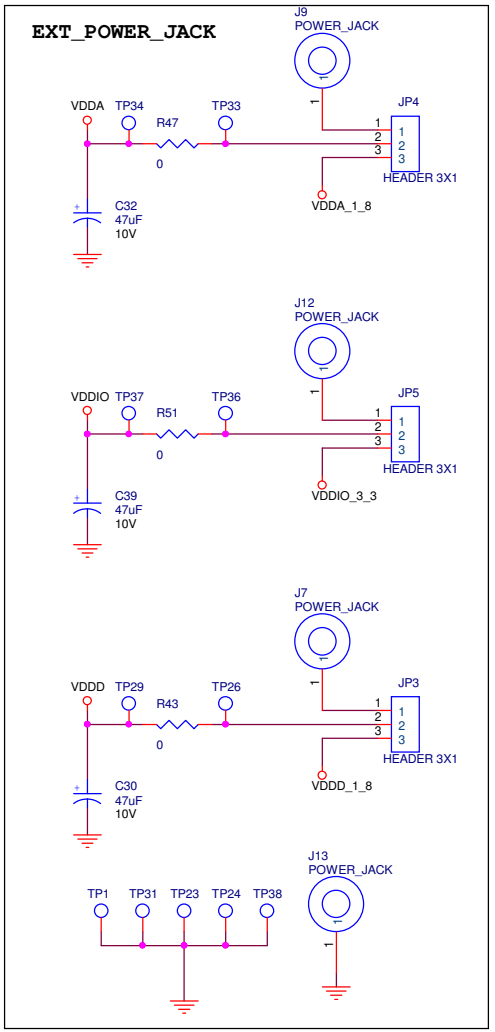


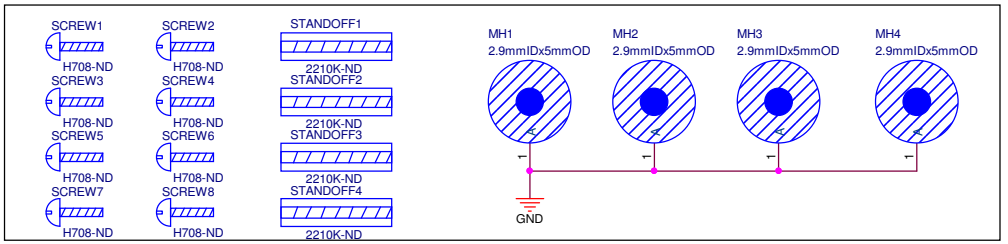






To use internal regulator, jumper pins 1, 2, and do NOT supply power to J13





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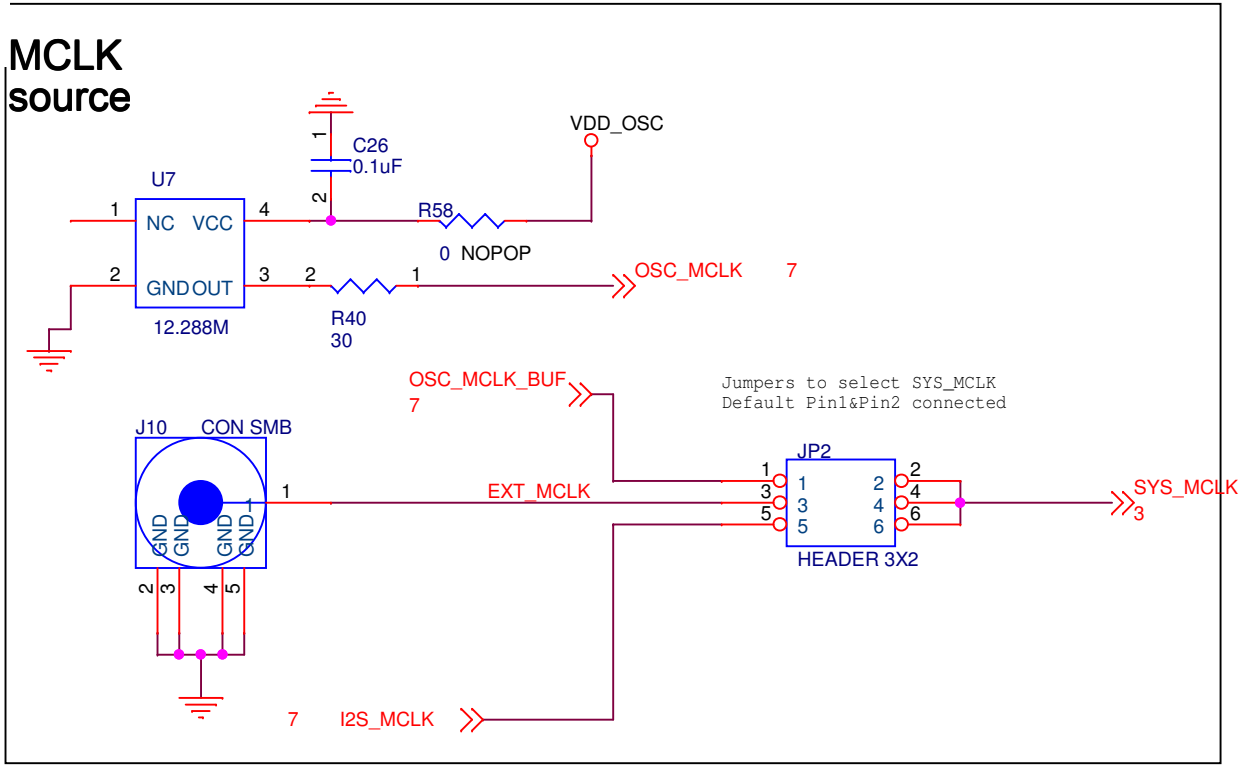
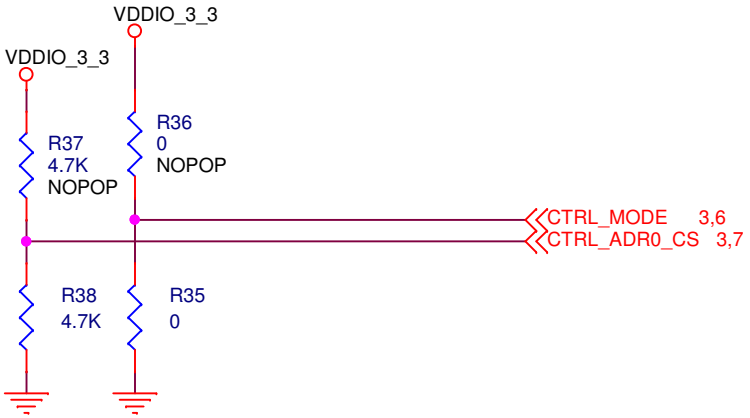
MCLK source



When CTRL_MODE = GND (I2C), CTRL_ADR0 can be pulled up or down to set the LSB of the I2C address. When CTRL_MODE = VDDIO (SPI), CTRIL_ADR0_CS is the SPI chip select.



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