MPC8560 PowerQUICC III™ Torridon User's Guide

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Chapter 1 References

This section contains references used throughout this design guide.

1.1 Glossary

Table 1-1 shows acronyms and terms used throughout this design guide.

Table 1-1. Glossary of Terms

Term	Description
ATA	AT Attachment
ATM	Asynchronous Transfer Mode
Boot Processor	MPC8560 Networking and Communications Processor
CD	Carrier Detect
COP	Common On-Board Processor
CPM	Communication Processor Module
CTS	Clear To Send
DDR SDRAM	Double Data Rate SDRAM
DIMM	Dual Inline Memory Module
DIP	Dual Inline Package
DLL	Delay Locked Loop
DMA	Direct Memory Access
DSR	Data Send Ready
DTR	Data Terminal Ready
EEPROM	Electrically Erasable Programmable Read Only Memory
FCC	Fast Communications Controller
FIFO	First In First Out
FPGA	Field Programmable Gate Array
GMII	GBit Media Independent Interface
GPCM	General Purpose Chip Select Machine
I2C	Inter-Integrated Circuit Controller
IDE	Integrated Device Electronics
I/O	Input/Output

Table 1-1. Glossary of Terms (continued)

Term	Description
LP-LVDS	Link Protocol - Low Voltage Differential Signalling
JTAG	Joint Test Access Group
MAC	Media Access Controller
MCC	Multi-Channel Communications Controller
MII	Media Independent Interface
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCMCIA	Personal Computer Memory Card International Association
PLL	Phase Locked Loop
PHY	Physical Interface
POR	Power on Reset
PowerQUICC	MPC8xx Networking and Communications Processor
PowerQUICCII	MPC82xx Networking and Communications Processor
PowerQUICCIII	MPC85xx Networking and Communications Processor
RI	Ring Indicator
RIO	RapidIO
ROM	Read Only Memory
RTS	Ready to Send
Rxd	Received Data
SCC	Serial Communications Controller
SDRAM	Synchronous Dynamic Random Access Memory
SPD	Serial Presence Detect
SSTL_2	Stub Series Terminated Logic for 2.5 Volts
TDM	Time Division Multiplex
TSEC	Triple Speed Ethernet Controller
Txd	Transmitted Data
USB	Universal Serial Bus
UTOPIA	Universal Test Operational Physical Interface for ATM
Work Processor	MPC8560 Networking and Communications Processor

1.2 References

Please refer to the following for more information.

1. MPC8560 Integrated Processor Reference Manual
2. MPC8540 Integrated Processor Reference Manual
3. TSI500 RapidIO Multi-port Switch User Manual
4. M88E1011 Data Sheet
5. Via VT82C686B “Super South” South Bridge Data Sheet
6. Torridon System Specification - Ver 1.3
7. Torridon User Manual - Ver 2.0

Chapter 2 Introduction

This section provides a brief introduction to the Torridon Platform.

2.1 Background

Torridon has been developed as a demonstration vehicle for Motorola's new generation of integrated communication processors, the PowerQUICCIII in a multi processor RapidIO environment. As well as a demonstration system, it is also a hardware and software reference platform and code development platform.

2.2 Scope

This design guide details the key design features of the platform and describes the specific implementation. This document is intended as a guide for hardware designers who are involved in the development of PowerQUICCIII based products.

It is not intended as a system specification nor a user manual for Torridon. Both these exist as separate documents.

2.3 System Overview

Although Torridon is designed such that it can plug into a larger system (e.g. through connectivity to a backplane), typically the platform will operate as a stand alone system. System configurations can change depending, for example, on the peripherals which are attached. The diagram in Figure 2-1 shows one possible system configuration.

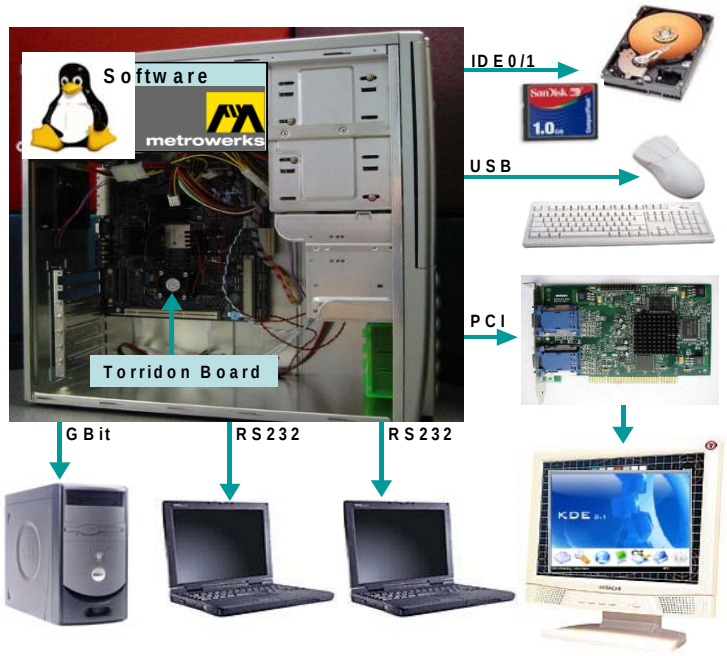


Figure 2-1. Typical Torridon Platform Configuration

The system consists of various parts

- The Torridon motherboard
- PCI expansion cards (e.g. graphics, additional peripherals)
- USB Peripherals (e.g. keyboard, mouse)
- Non-volatile storage (e.g. hard disk drive, Compact Flash)
- Communications (e.g. Gbit Ethernet, RS232)
- Linux Software Operating System
- Software Development Environment

Chapter 3 Motherboard

This section provides a brief introduction to the Torridon Motherboard.

3.1 Motherboard Overview

Figure 3-1below shows a picture of the Torridon Motherboard.

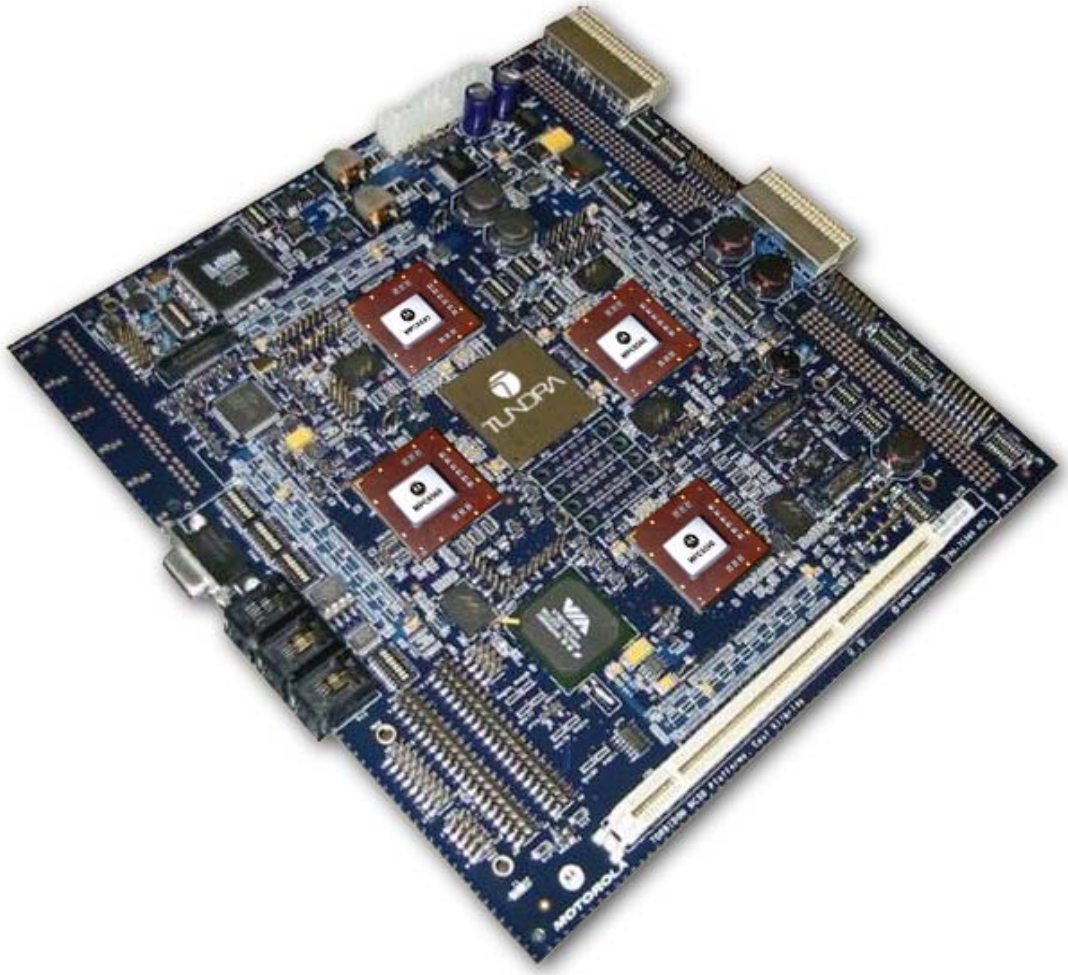


Figure 3-1. Torridon Motherboard

The board supports four MPC8560 processors. The main processor, which is responsible for booting the others and controlling the main peripherals, is referred to as the Boot Processor. The other three processors are referred to as Work Processor 1, 2 and 3.

The Boot Processor is responsible for peripheral support (e.g. USB, PS2 keyboard/mouse, hard disk, audio) via a “Southbridge chip”. It also provides support for a 64 bit PCI plug in card. It utilizes DDR memory as its local storage. Off board communications are made via a UART connection and a dual GBit ethernet connection.

In addition to the boot processor, there are the three additional PowerQUICCIII processors, Work Processor 1, 2 and 3. Each one of these processors support their own local DDR memory, UART and GBit Ethernet connections.

All of the processors communicate with each other via parallel RapidIO. A Tundra TSI500 RapidIO switch provides the switch fabric.

The board is powered from a 12V/5V/3.3V supply. All the other required voltages being generated on-board.

3.2 Motherboard Features

The motherboard consists of various subsystems

- Processor - The board has four MPC8560 processors.
- Flash - The main processor boots from its own local Flash ROM.
- DDR - Each processor has its own local bank of DDR memory.
- RapidIO - The processors communicate with each over RapidIO. This communication is via a RapidIO switch.
- GBit Ethernet - Each processor provides an interface to GBit Ethernet.
- UART - Each processor provides connectively to a UART port.
- PCI Expansion - Provided by a 64 bit PCI slot.
- Peripheral Support - Provided by a South Bridge Chip.
- Communications - Additional communications are handled via a “QUICC Application Development System” (QUADS) Compatible Header and a UTOPIA connection to the backplane
- Reset - The system reset is handled by an on-board CPLD.
- System Clocking - All the required clock signals are generated locally on board.
- Voltage Regulation - All the required voltage levels are generated locally on board.

Figure 3-2 below shows a block diagram of the system.

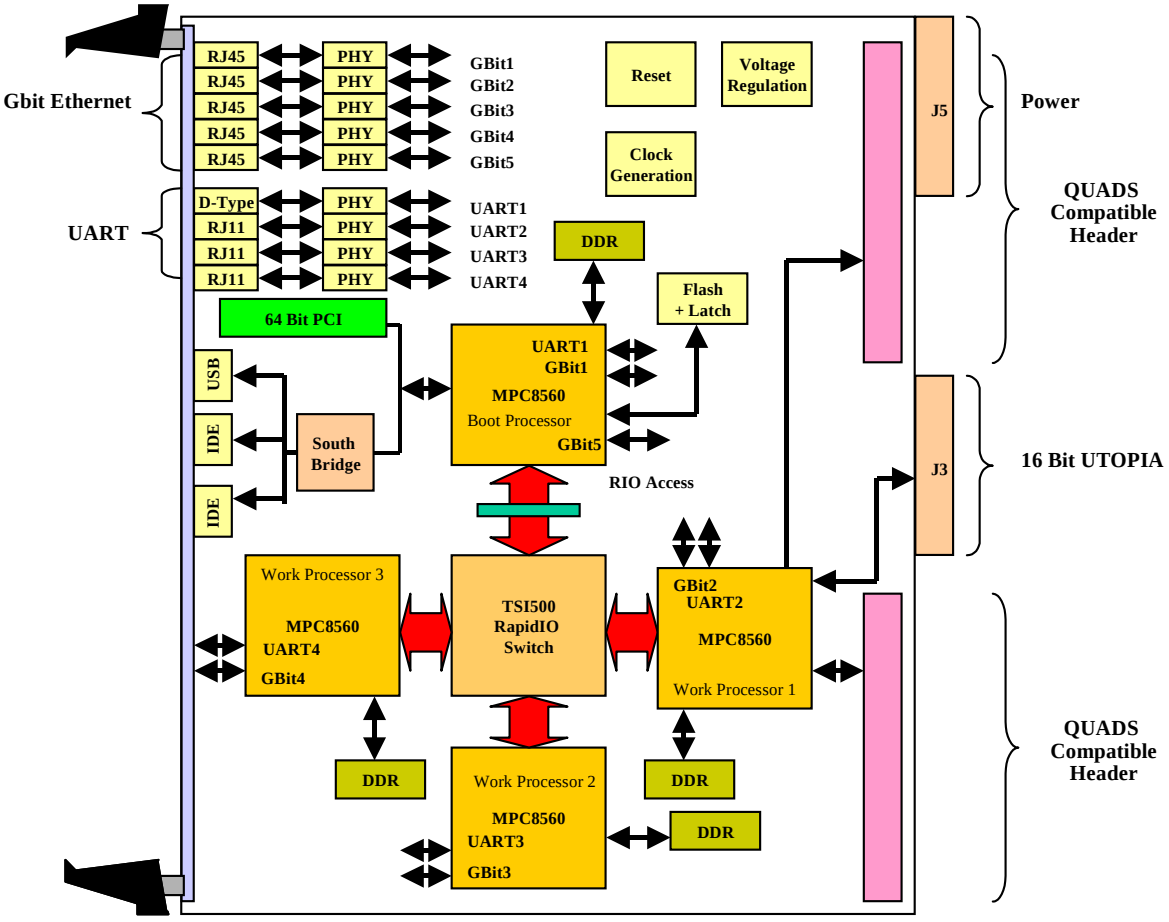


Figure 3-2. Torridon Block Diagram

Chapter 4 Processor

This section describes the processor sub-section on the Torridon Motherboard.

4.1 Overview

The processors on Torridon are all MPC8560s. The MPC8560 PowerQUICCIII is the next generation PowerQUICCII integrated communications processor. The MPC8560 provides integration of processing power for networking and communications peripherals resulting in higher device performance. The MPC8560 has four main system blocks.

The first block is a high-performance embedded e500 core processor with 256 kbyte of level-2 cache, implementing the enhanced Book E instruction set architecture.

The second block is the communications processor module (CPM). The CPM of the MPC8560 supports three high-performance fast communications channels (FCCs) for 155Mbps ATM and Fast Ethernet, and up to 256 full-duplex, time-division-multiplexed (TDM) channels using two multi-channel controllers (MCCs). Other communications (for example UART) are supported by the serial communication controllers (SCCs).

The third block is a bus controller which provides a DDR SDRAM memory controller, a local bus controller, I2C interconnect as well as an interrupt controller.

The fourth block provides additional interfaces for system integration. These include two integrated 10/100/1000 Triple Speed Ethernet controllers (TSECs), a 64-bit PCI/PCI-X controller and a RapidIO interconnect. This high level of integration simplifies board design and offers significant bandwidth and performance for high-end control-plane and data-plane applications.

Each MPC8560 provides the following main functionality on board:

- A DDR memory controller
- A Flash ROM memory controller (On the Boot Processor only)
- An RS232 interface
- Two GBit Ethernet interfaces (Only one is supported on each of the Work Processors)
- A PCI interface (provides a connection to the Southbridge) (On the Boot Processor only)
- A RapidIO interface

4.2 MPC8560 Processor Configuration

Unlike the PowerQUICCII family which uses a hard reset configuration word for initial configuration of the processor, the MPC8560 uses dedicated input pins. These pins are sampled during the assertion of reset and are used to configure variables such as the internal clock frequency, boot ROM location and so on.

These pins are sampled during the assertion of reset. This reset signal is generated locally on-board from the reset circuitry. The configuration signals are passed through a ‘244 buffer with its output enable signal controlled by the reset. This is shown in Figure 4-1 below.

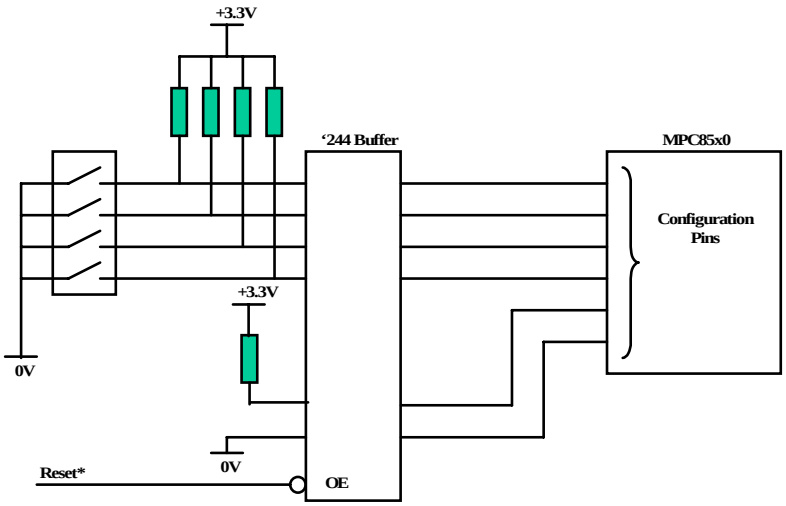


Figure 4-1. MPC8560 POR Configuration

Note: For the sake of clarity, only six configuration signals are shown in the diagram above.

Some of the signals are changeable via a set of DIP switches, whereas others are hard wired on the board.

Some of these signals have an internal pull-up which selects a default state.

Table 4-1 below summarizes these configuration pins and their specific usage on Torridon.

Table 4-1. MPC8560 Configuration

Functional Pin	Usage	Chip Default	Torridon Setting	Torridon Setup Description	Controlled By	Note
LA[28:31]	Internal PLL Ratio	None	1010	Internal clock set to 10:1 Ratio	DIP Switches	1
LALE, LGPL2	e500 Core PLL Ratio	None	01	e500 core set to 5:2 Ratio	DIP Switches	2
TSEC1_TxD[6:4]	Boot ROM Location	111	111	Processor boots from 32bit ROM	DIP Switches	3
LWE[2:3]	Host/Agent Config.	11	11	Processor acts as a host processor	DIP Switches	4
LA[27]	CPU Boot Hold off	1	1	Processor is released from reset without waiting for external configuration	DIP Switches	5
LGPL3,LGPL5	Boot Sequence Config.	11	11	Boot sequencer is disabled	Default Assumed	—
EC_MDC	Adjust TSEC Width	1	1	TSEC Port Width set to GMII	Default Assumed	—
TSEC1_TxD[7]	Configure TSEC 1 I/F	1	0	TSEC1 set to GMII mode	DIP Switches	—
TSEC2_TxD[7]	Configure TSEC 2 I/F	1	0	TSEC2 set to GMII mode	DIP Switches	6
LGPL0, LPGL1	RapidIO Clock Source	11	01	The source of the RapidIO Transmit Clock is the RapidIO Receive Clock	DIP Switches	—
TSEC2_TxD[4:2]	RapidIO Device ID	None	001	Select RapidIO Device ID	DIP Switches	7
PCI_REQ64	PCI Width (32 or 64)	1	1	PCI Bus set to 32 Bit	Default Assumed	8
PCI_GNT[1]	PCI I/O Impedance	1	0	PCI I/O Impedance set to 25 ohms	DIP Switches	8
PCI_GNT[2]	PCI Arbiter Enable	1	1	Internal PCI Arbitrator is Enabled	Default Assumed	8
PCI_GNT[3]	PCI Debug Enable	1	1	PCI Debug is Disabled	Default Assumed	8
PCI_GNT[4]	PCI/PCI-X Bus Configuration	1	1	PCI Mode is Selected	Default Assumed	8
MSRCID[0]	Memory Debug Enable	1	1	Debug Data is driven on MSrcID and MDVAL Pins	DIP Switches	—
MSRCID[1]	DDR Debug Enable	1	1	Debug Data is not Driven on ECC	Default Assumed	—
LWE[0:1]	PCI O/P Hold Config	11	11	Adjust Hold Times for PCI Drivers	DIP Switches	8
TSEC2_TxD[6:5]	Local Bus Hold Config	11	11	Adjust Hold Times for Local Bus Drivers	DIP Switches	9

1 Based on a 33.3MHz input clock, the platform clock will run at 333MHz.

[2] Based on a 33.3MHz input clock, the core clock will run at 833Mhz

[3] For the Work Processors, this is set to 011 meaning the boot ROM location is RapidIO

[4] For the Work Processors, this is set to 01 meaning the processor is configured as a RapidIO agent

[5] For the Work Processors, this is set to 0 meaning the processor is prevented from booting until released by the Boot Processor

[6] Not used on the Work Processors; they only use TSEC1

[7] The RapidIO device IDs are as follows

Boot Processor ID = 1
Work Processor 1 ID = 2
Work Processor 2 ID = 3
Work Processor 3 ID = 4

[8] Not used on the Work Processors; they do not use PCI.

[9] Not used on Work Processors 2 & 3; they do not use their local bus

4.3 COP Interface

The COP - Common On-Chip Processor, is part of the MPC8560's JTAG machine, implemented as a set of additional instructions and logic within the JTAG permissions. This port may be connected to a dedicated debug station for extensive system debug.

There are several third party debug solutions on the market. These debug-stations may be connected to the host computer via either Ethernet, Parallel-Port, RS232 or any other media.

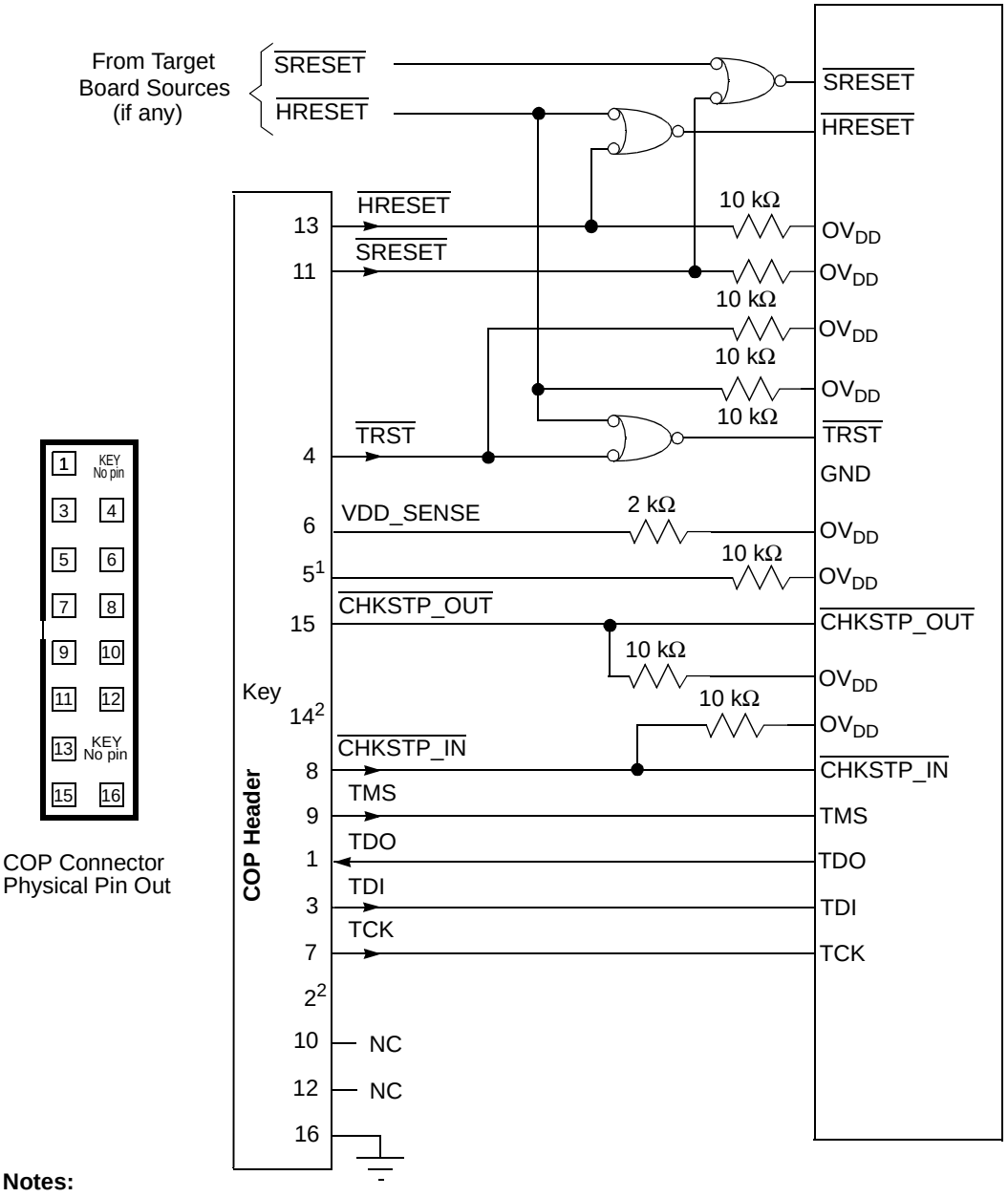
To support debug station connection to the COP/JTAG port of each processor, five 16 pin headers are provided on Torridon, carrying the COP/JTAG signals as well as additional signals aiding in system debug.

The pinout for each of the COP/JTAG connectors is shown in Table 4-2 below.

Table 4-2. COP/JTAG Connector

Pin#	Signal	Description
1	TDO	Transmit Data Output. The MPC8560's JTAG serial data output pin.
2	NC	Not Connected
3	TDI	Transmit Data Input. The MPC8560's JTAG serial data input pin.
4	TRST*	Test port Reset. Used to resets the JTAG logic on the MPC8560.
5	+3.3V	+3.3 Volt Power.
6	+3.3V	+3.3 Volt Power
7	TCLK	Test port Clock. This clock shifts in / out data to / from the MPC8560's JTAG logic.
8	CHK_STP_IN*	Check Stop In.This pin is pulled up to 3.3V via a 10K resistor.
9	TMS	Test Mode Select. This signal changes the state of the JTAG machines.
10	NC	Not Connected
11	SRESET*	Soft Reset. The MPC8560's Soft Reset Signal.
12	NC	Not Connected
13	HRESET*	Hard Reset. The MPC8560's Hard Reset Signal.
14	NC	Not Connected
15	CHK_STP_OUT*	Check Stop Out.This pin is pulled up to 3.3V via a 10K resistor.
16	GND	Digital Ground

The diagram in Figure 4-2 shows the COP/JTAG connections.



Notes:

1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the part. Connect pin 5 of the COP header to OV_{DD} with a 10 KΩ pull-up resistor.
2. Key location; Pins 2 and 14 are not physically present on the COP header

Figure 4-2. COP/JTAG Connections

Chapter 5 Flash

This section describes the flash sub-section on the Torridon Motherboard.

5.1 Overview

Although Torridon supports four processors, only one of these, the boot processor, uses local Flash ROM directly as its boot device. The other processors, the work processors, boot over RapidIO. Hence, Torridon only requires one bank of Flash memory.

The MPC8560 boots from a Flash ROM which is accessed using the MPC8560's General Purpose Chip Select Machine (GPCM). The address and data on the local bus of the MPC8560 is multiplexed. An external demultiplexor, controlled by the local buses address latch enable (LALE) signal is used to separate the address and data bus.

5.2 Flash

The Flash is arranged as 32 bit wide Flash ROM and is physically implemented in two AMD 29LV641D Flash devices providing a total of 16Mbytes of Flash. This Flash is soldered directly onto the Torridon motherboard.

The diagram in Figure 5-1 shows the Flash ROM on the Boot processor.

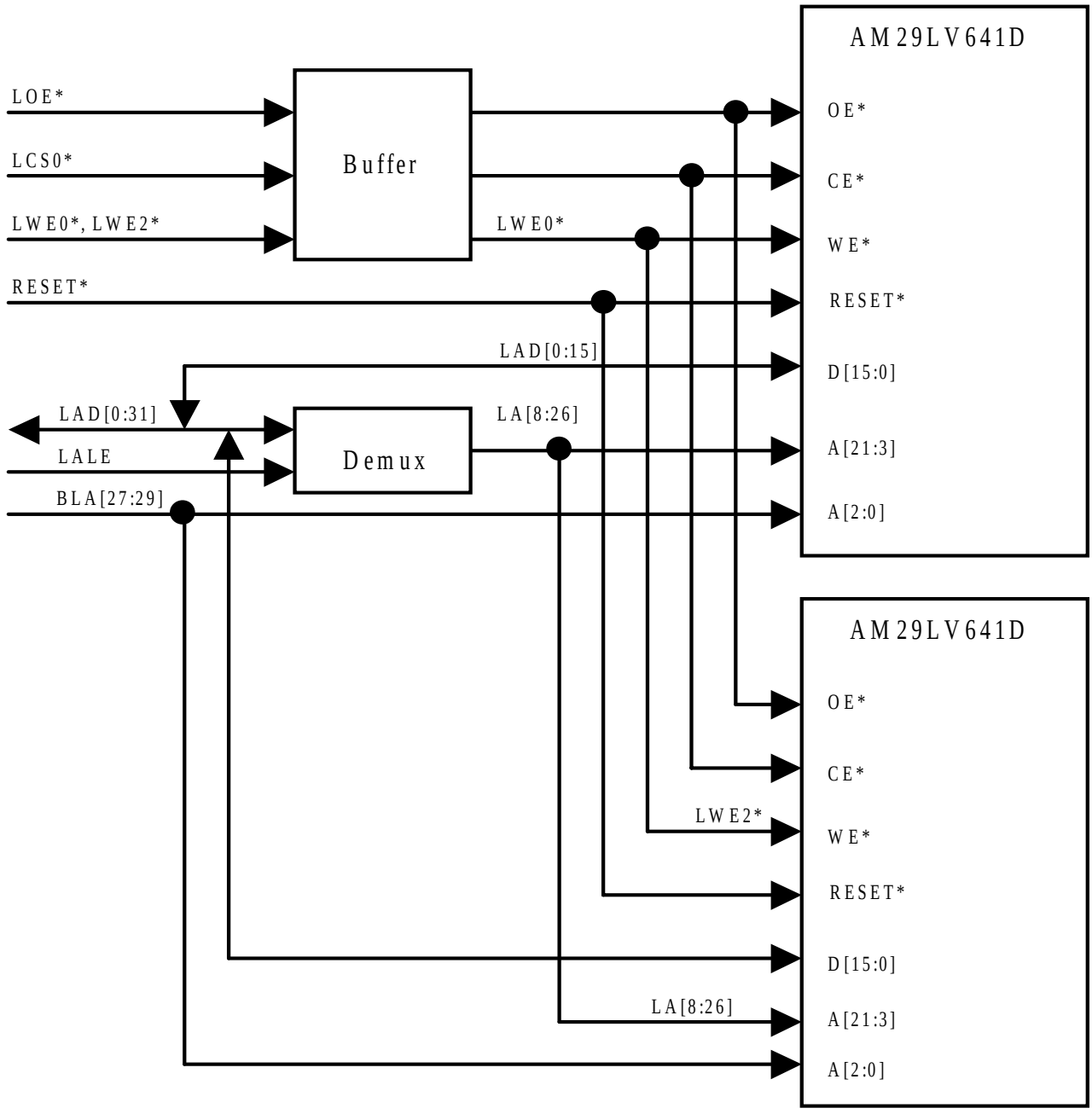


Figure 5-1. Flash ROM

The schematics for the Flash interface are shown in Figure 5-2, Figure 5-3, and Figure 5-4.

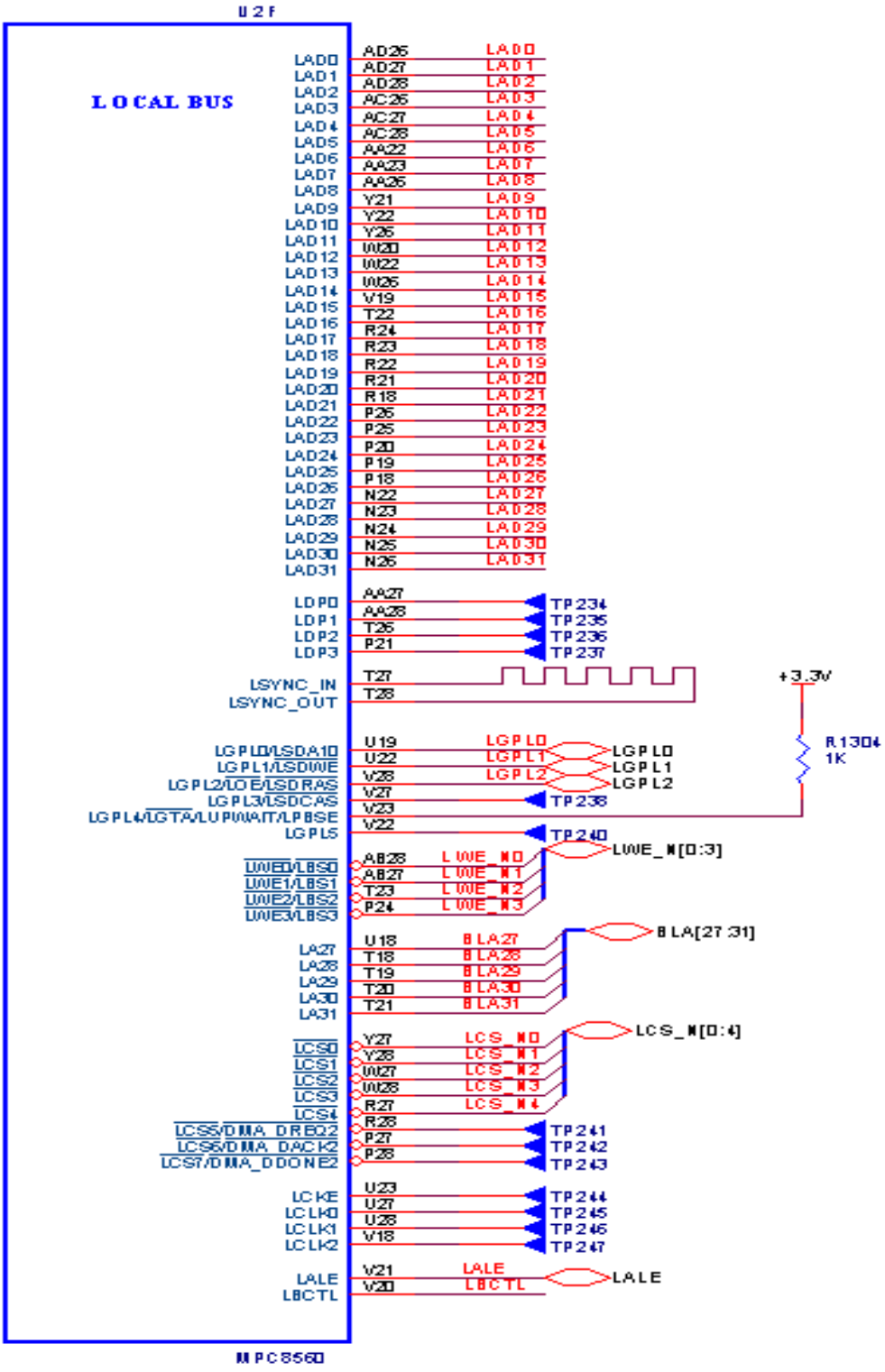


Figure 5-2. Flash ROM Schematics - Local Bus Controller

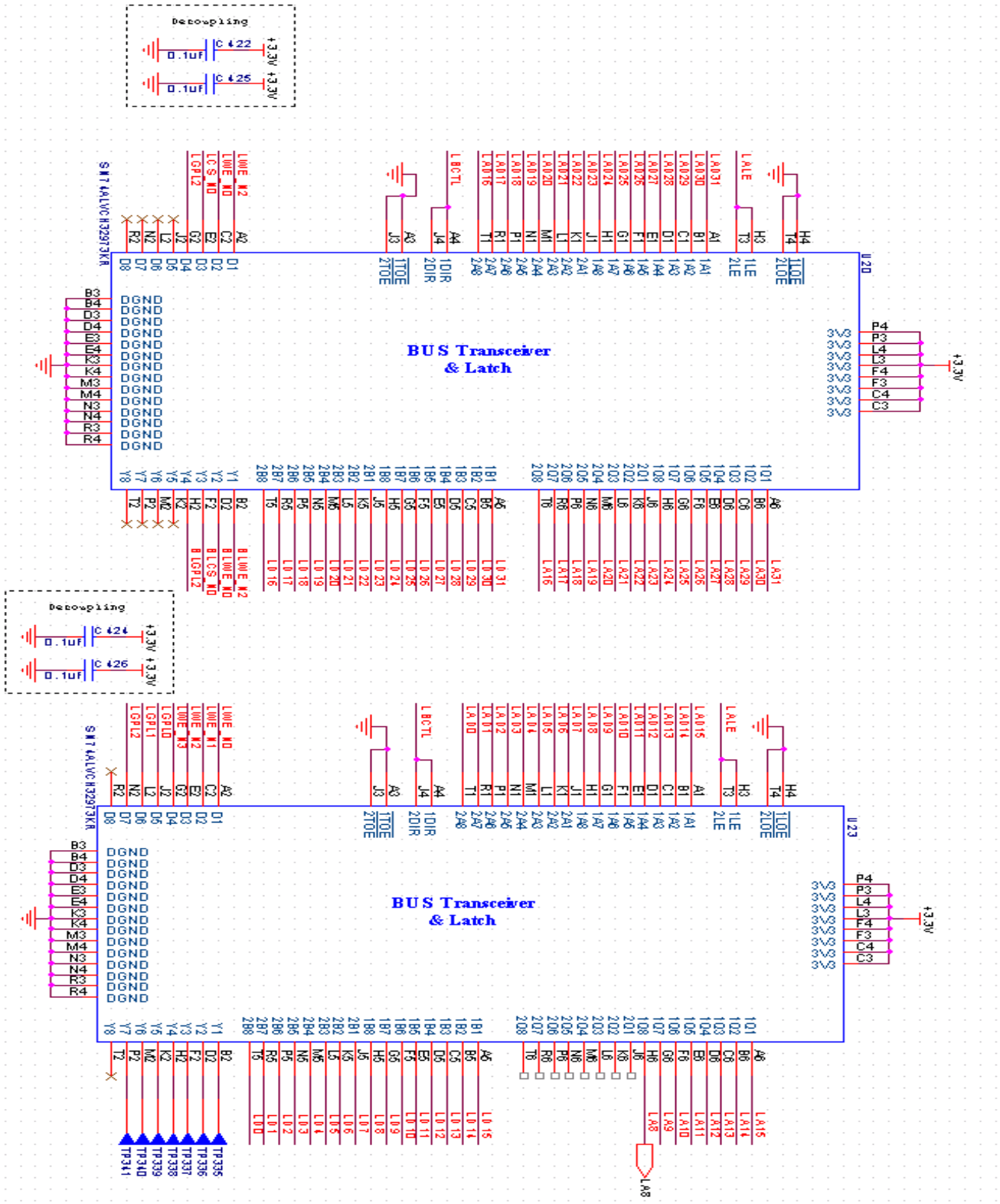


Figure 5-3. Flash ROM Schematics - Address/Data Demuxing

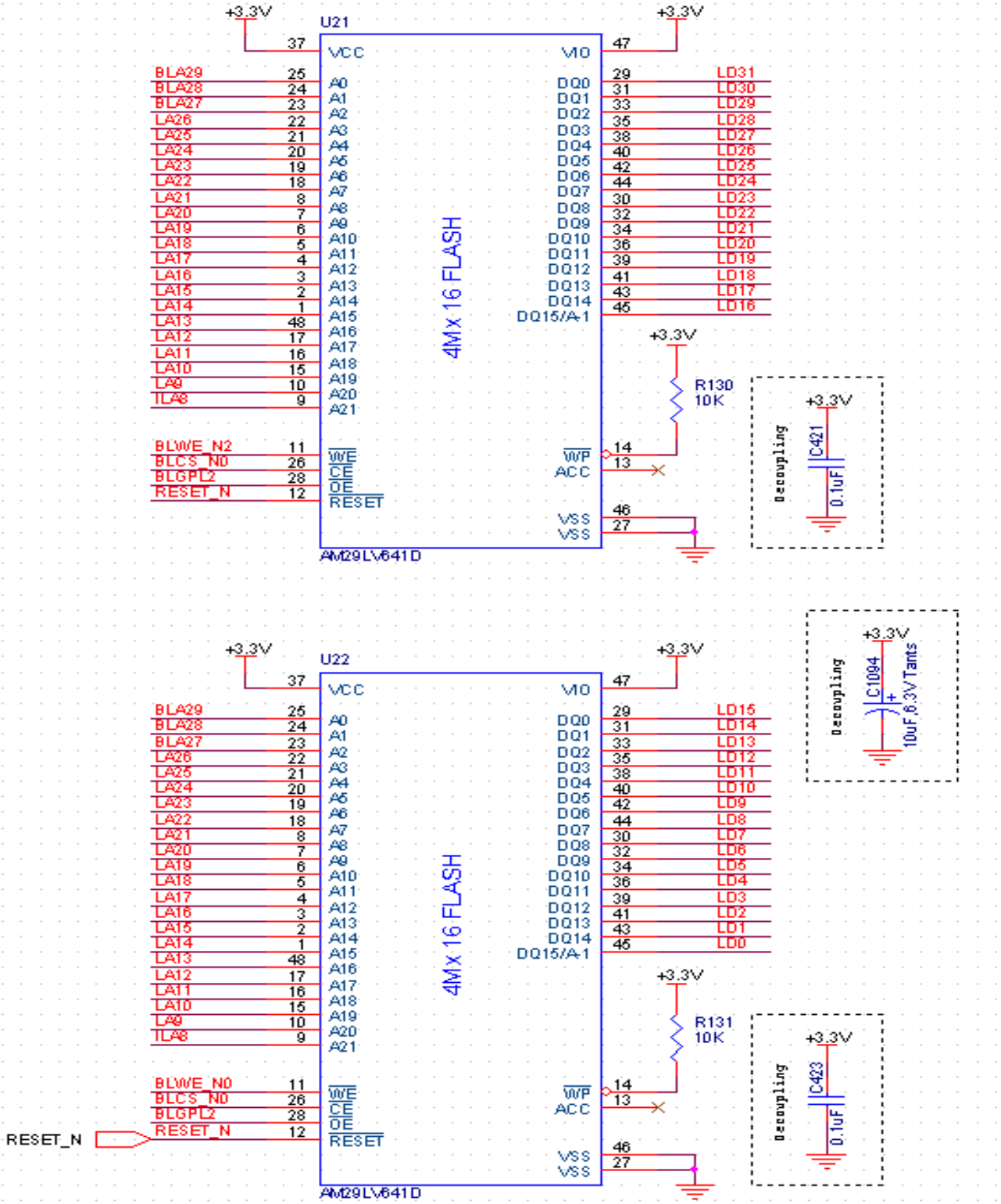


Figure 5-4. Flash ROM Schematics - Flash

The following should be noted about the circuitry.

- Although the local bus's DLL is connected (LSYNC_IN, LSYNC_OUT), no synchronous devices are connected to the local bus.
- The external Transfer Acknowledge (/LGTA) signal is pulled up to ensure the cycle is not terminated by a false transfer acknowledge cycle.
- The '74ALVCH32973 devices provide both buffering and de multiplexing.
- As the '74ALVCH32973 is 16 bits wide, two devices are required to de-multiplex the 32 bit bus.
- Some of the control signals (e.g. LWE_N0, LGPL2 etc.) are used elsewhere in the design. These are buffered to provide additional drive to cope with the additional loading.
- As the processor is big endian, the least significant bit on the address and data bus is bit 31.
- The flash devices are arranged as 32 bit wide devices, hence the two least significant address bits are don't cares.
- The burst address pins (BLA(27:29]) allow burst accesses to be supported.
- Note the write enable signals are different for each Flash device.

Chapter 6 DDR

This section describes the DDR sub-section on the Torridon Motherboard.

6.1 Overview

6.1.1 DDR Memory

DDR (Double Data Rate) memory is the next generation SDRAM. Like SDRAM, DDR is synchronous with the system clock however, DDR reads data on both the rising and falling edges of the clock signal. SDRAM only carries information on the rising edge of a signal. This enables the DDR module to transfer data twice as fast as traditional SDRAM. For example, using a clock rate of 133MHz on a SDRAM would yield a data rate of 133MHz. The same clock rate on DDR memory would transfer data at 266MHz.

6.1.2 The MPC8560's DDR Memory Controller

The MPC8560 has an integrated memory controller which supports JEDEC standard DDR Type 1 SDRAMs. The DDR memory controller is intended for use with x8 or x16 DDR SDRAMs. In addition, the memory controller will either be connected to all unbuffered DIMMs or all registered DIMMs. The memory controller does not support a mix of unbuffered and registered DIMMs in the same system.

The memory controller includes these distinctive features:

- Support for DDR Type 1 SDRAM
- 64/72-bit DRAM data bus
- Programmable settings for meeting all DRAM timing parameters
- Many different DRAM configurations supported
- Support for up to four banks, each bank independently addressable
- Support for 64 Mbit to 1 Gbit devices with x8/x16 data ports

6.1.2.1 Available Signals

The DDR SDRAM memory is controlled directly by the processor's memory controller. The memory controller provides all the signals necessary for this control.

The signals used by DDR can be split into three different groups.

Table 6-1 details the signals provided by the MPC8560's memory controller.

Table 6-1. DDR SDRAM Interface Signals

Signal Group	Signal Name	Description	I/O (w.r.t. Processor)
Address & Control	BA[0:1]	Bank Address Bus	Output
	A[0:14]	Address Bus	Output
	RAS*	Row Address Strobe	Output
	CAS*	Column Address Strobe	Output
	WE*	Write Enable	Output
	CS[0:3]*	Chip Selects	Output
Data	DQ[0:63]	Data Bus	Input/Output
	DQS[0:8]	Data Strobes	Input/Output
	DM[0:8]	Data Masks	Outputs
	ECC[0:7]	Error Correction Codes	Input/Output
Clock	CLK[0:5]	Clocks	Output
	CLK[0:5]*	Complement Clocks	Output
	CKE[0:1]	Clock Enable	Output
	MSYNC_IN	Delay Locked Loop Synchronization In	Input
	MSYNC_OUT	Delay Locked Loop Synchronization Out	Output

6.2 Design Considerations

The following section details design considerations.

6.2.1 Signal Termination

The DDR SDRAM memory controller uses Stub Series Terminated Logic for 2.5 Volts, SSTL_2. To guard against unwanted signal reflections on the signal paths, these lines must be impedance matched. Typically this is achieved by the use of a series termination and a pull up resistor, connected to the termination voltage, V_{TT}. The V_{TT} voltage is implemented on the PCB as a split plane on the top layer. This is referred to as the "V_{TT} Island".

The diagram in Figure 6-1 shows a single ended termination scheme.

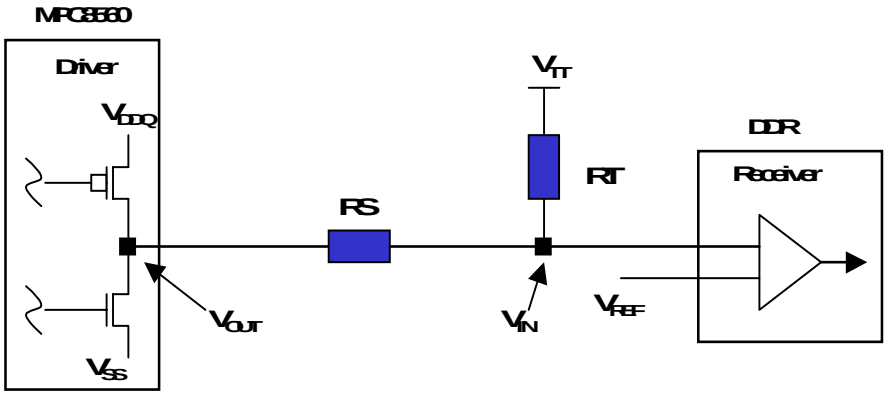


Figure 6-1. DDR Termination

Where R_S = Series Resistance, R_T = Termination Resistance.

On Torridon; R_T = 27 Ohms, R_S = 22Ohms.

6.2.2 Signal Connections

6.2.2.1 Address and Control Signals

As well as fifteen address bits, A[0:14], the MPC8560's memory controller provides two bank address bits, BA[0:1]. This allows a maximum address range of 1GBit. Four chip selects (CS[0:3]) provide connection to four separate physical banks. (As opposed to the Bank Address pins which select logical banks).

As with "normal" SDRAM, the row and column addresses are latched using a Row Address Strobe (RAS*) and a Column Address Strobe (CAS*) respectively. A Write Enable signal (WE*) indicates a write cycle is in progress.

6.2.2.2 Data

The data signal group is made up of four different types of signals; data bits, mask bits, strobe bits and parity bits. The data bus is 64 bits wide. Each byte of data has its own mask bit (used to mask specific data byte lanes during a write cycle) and its own strobe bit (used to latch the data).

As well as this, the entire data bus is protected by parity. As with the data bits, the parity bits have their own dedicated mask and strobe bits.

6.2.2.3 Clock

The MPC8560's memory controller provides 6 clock / complement clock pairs. The number of clock pairs actually used will depend on the physical implementation. For example, a single 64 bit DDR DIMM would require 3 clock pairs.

6.2.2.4 Serial Presence Detect

Most DDR SDRAM DIMMs support Serial Presence Detect (SPD). The DDR SDRAM configuration is contained in a non-volatile ROM on the DDR SDRAM DIMM. This ROM is accessed by the processor's I^2C bus. Using the interface, the processor may interrogate the memory to check for its presence, size, speed etc.

Note: The I^2C signals are open drain and require pull ups.

6.2.2.5 DDR SDRAM Power

The diagram in Figure 6-2 shows the voltage levels associated with the DDR SDRAM interface.

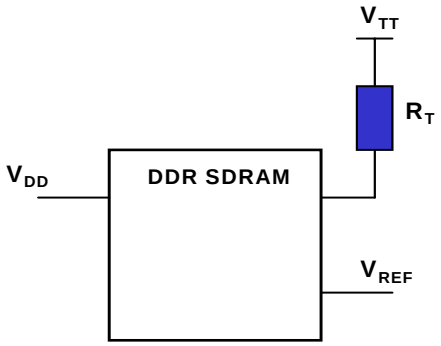


Figure 6-2. DDR SDRAM Voltage Levels

The SSTL_2 interface uses a reference voltage and differential input to determine the logic levels.

$V_{REF} = V_{DD} / 2$

$V_{TT} = V_{REF}$

Where: V_{DD} is the supply voltage

V_{REF} is the reference voltage

V_{TT} is the termination voltage

Therefore,

V_{DD} = 2.5 Volts

$V_{TT} = V_{REF} = V_{DD} / 2$ = 1.25 Volts.

6.2.2.6 Voltage Generation

The required termination voltage for each DDR SDRAM DIMM is generated locally. i.e. each DDR DIMM will have its own dedicated power supply.

The reference voltage, V_{REF}, and the termination voltage, V_{TT}, are generated from the input voltage, V_{DD}, using a National Semiconductor LP2995 voltage regulator.

The diagram in Figure 6-3 shows the generation of these voltage levels.

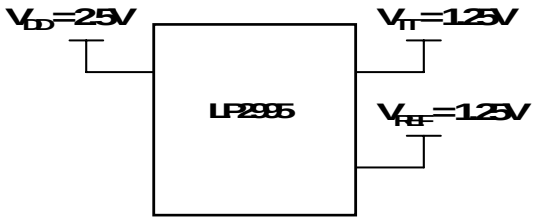


Figure 6-3. DDR SDRAM Voltage Generation

6.3 Physical Implementation

The diagram in Figure 6-4 shows the connection between the MPC8560 and the DDR SDRAM. On Torridon, the DDR is physically implemented as a SODIMM (Small Outline DRAM In Line Memory Module) however the connections shown will be very similar for a full sized DIMM or if using discrete devices.

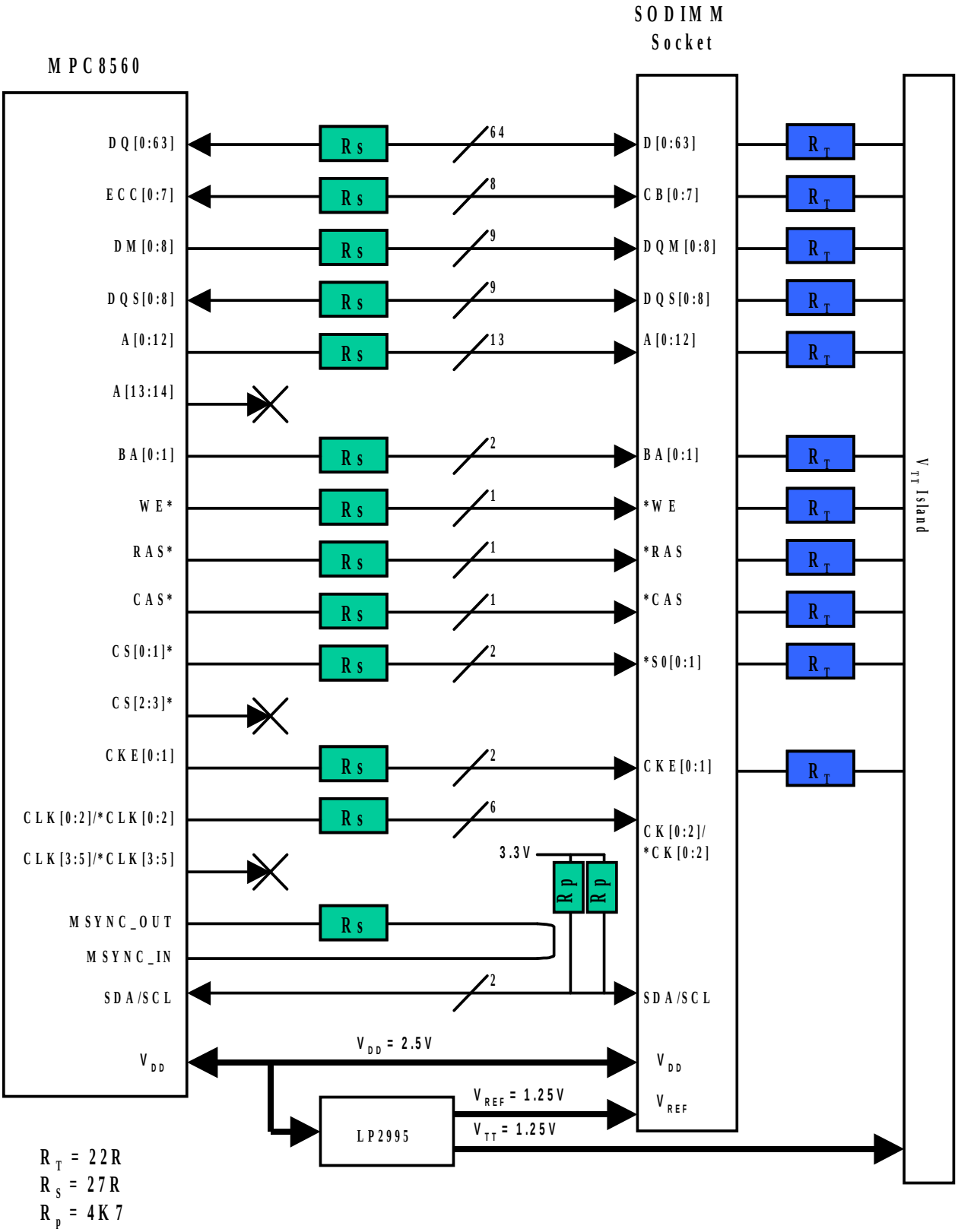


Figure 6-4. 64 Bit DDR SDRAM

The diagram in Figure 6-4 above shows the connection between the MPC8560 and the SODIMM on Torridon.

Each processor can support an SODIMM up to 1Gbit. Thirteen address signals, A[0:12], and the two bank address signals, BA[0:1], are used to support this address range. The other two address signals, A[13:14], are not used and are left unconnected.

Each processor support one SODIMM. As each SODIMM may have up to two banks, two chip selects, CS[0:1], are used. The other two chip selects, CS[2:3], which would be used if another DIMM were present on the design, are left unconnected.

Again, due to the fact that only one SODIMM is used, only three of the clock pairs are required.

Although not part of the DDR controller, the I2C interface is shown which supports the serial presence detect mechanism.

6.3.1 Schematics

The schematics in Figure 6-5 show the MPC8560 - DDR SODIMM connection on Torridon.

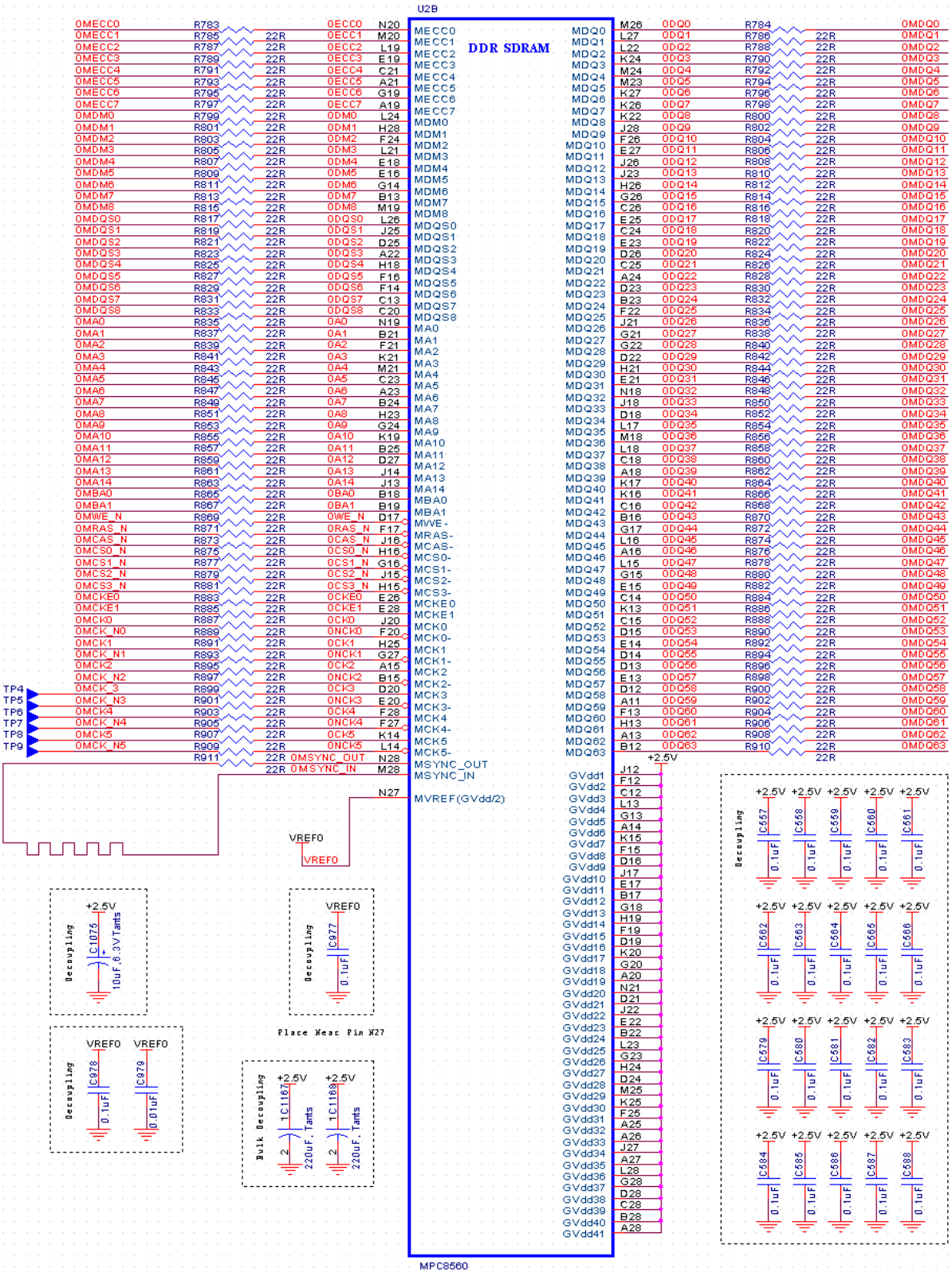


Figure 6-5. MPC8560 DDR Controller

The schematics in Figure 6-5 above show the breakout from the MPC8560's DDR controller

The following points should be noted.

- Torridon supports four MPC8560 processors, each with its own dedicated DDR memory. To differentiate the signals, the net names are preceded with a number: 0, 1, 2 or 3.
- The undulating line connecting MSYNC_OUT and MSYNC_IN indicates that this signal length must be of a certain length. The length of this signal will be determined during the layout process.
- Specific net names are given to the nets between the processor and the series resistor and the nets between the series resistor and the SODIMM. These specific net names are used when matching signal lengths during the layout.
- The use of discrete resistors, as opposed to resistor networks, makes the layout easier with respect to matching signal lengths. Using resistor networks would force several signals to converge to a single package. This makes line length matching more difficult as it limits flexibility.

The schematics in Figure 6-6 below show the connection to the SODIMM. The following points should be noted.

- In this case, resistor networks can be used as opposed to individual ones. The constraints on these signals (i.e. the distance to the V_{TT} island) are not as stringent as on the previous signal, hence more variations on signal lengths can be tolerated.
- As a rule of thumb, two decoupling capacitors should be used for each resistor network.
- In addition, two bulk capacitors (10uF) are also used.
- A voltage tap is taken from the mid point of the V_{TT} rail. This monitors the actual voltage on this rail. This data is fed back to the voltage generator.

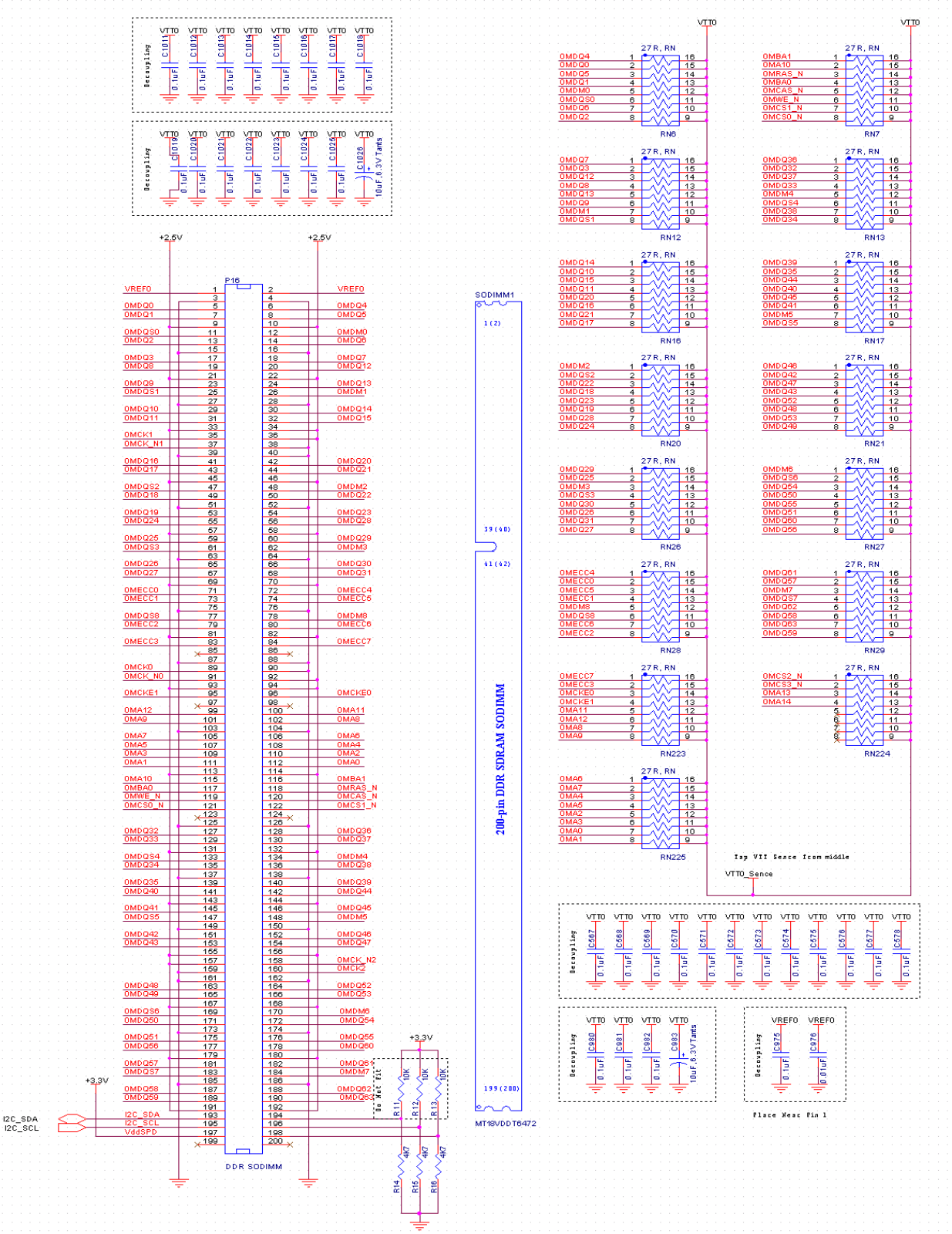


Figure 6-6. SODIMM Connection

The schematic in Figure 6-7 below shows the V_{TT} voltage generation.

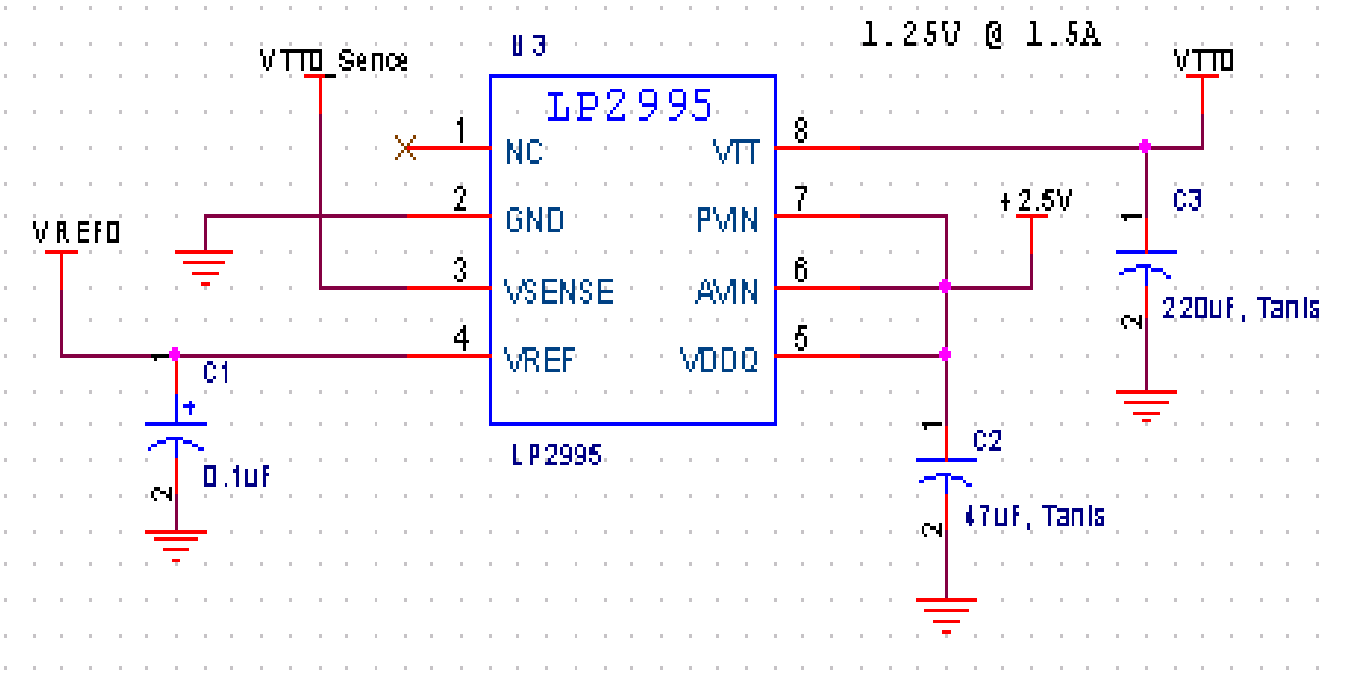


Figure 6-7. V_{TT} Voltage Generation

6.4 Layout

The following section details layout considerations.

6.4.1 Address and Control

The diagram in Figure 6-8 below shows the usage of the address and control signals on Torridon.

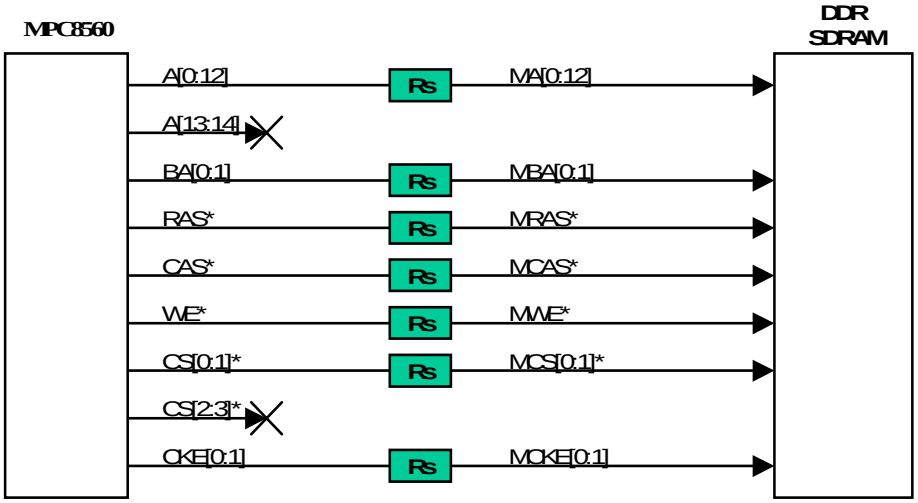


Figure 6-8. Address and Control

The length of each signal is the length of the etch from the processor to the series resistor plus the length of the etch between the series resistor and the DDR SODIMM.

For example, the total length of the row address strobe is [RAS*] + [MRAS*].

To ensure correct operation, all the signals should be equal in length to each other to within 50mils.

The diagram in Figure 6-9 shows the layout of the address and control group.

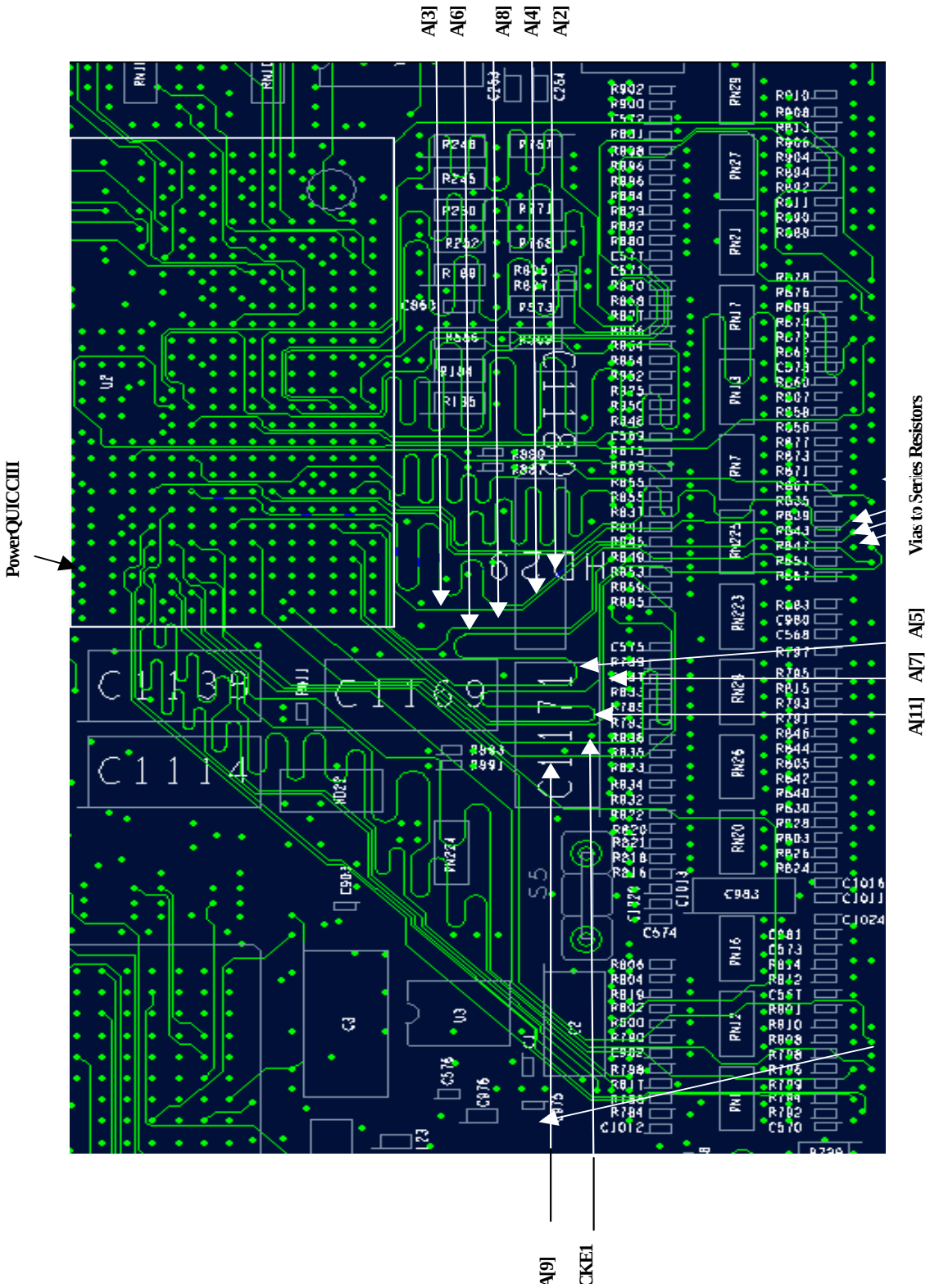


Figure 6-9. Address and Control Layout

6.4.2 Data

The data group is made up of nine data lanes. Each data lane contains the byte of data, the strobe signal and the mask signal. The data signal group should be considered as nine separate byte lanes as detailed below in Table 6-2.

Although during normal operation, the designation of these signal groups is all but transparent to the user, the grouping of these signal lanes is important during the layout of the data signal group.

Table 6-2. Data Byte Lanes

Byte Lane	Signal Name
0	DQ[0:7], DQS[0],DM[0]
1	DQ[8:15], DQS[1],DM[1]
2	DQ[16:23], DQS[2],DM[2]
3	DQ[24:31], DQS[3],DM[3]
3	DQ[32:39], DQS[4],DM[4]
3	DQ[40:47], DQS[5],DM[5]
6	DQ[48:55], DQS[6],DM[6]
7	DQ[56:63], DQS[7],DM[7]
8	ECC[0:7], DQS[8],DM[8]

The diagram below in Figure 6-10 shows the data lanes.

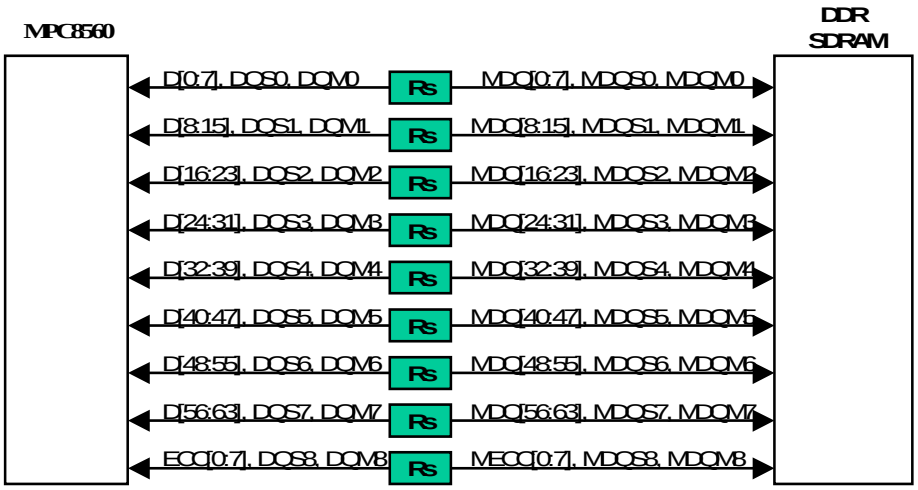


Figure 6-10. Data

The following rules should be applied when laying out the data signals.

- Route each data byte lane on a single layer.
- Each data byte lane consists of 10 signals.
- Each signal has two sections - between the processor and the series resistor and between the series resistor and the DIMM.
- The 9 data byte lanes are as follows:

(xDQ + xMDQ)[7:0], (xDM+xMDM)[0], (xDQS+xMDQS)[0]

(xDQ + xMDQ)[15:8], (xDM+xMDM)[1], (xDQS+xMDQS)[1]

(xDQ + xMDQ)[23:16], (xDM+xMDM)[2], (xDQS+xMDQS)[2]

(xDQ + xMDQ)[31:24], (xDM+xMDM)[3], (xDQS+xMDQS)[3]

(xDQ + xMDQ)[39:32], (xDM+xMDM)[4], (xDQS+xMDQS)[4]

(xDQ + xMDQ)[47:40], (xDM+xMDM)[5], (xDQS+xMDQS)[5]

(xDQ + xMDQ)[55:48], (xDM+xMDM)[6], (xDQS+xMDQS)[6]

(xDQ + xMDQ)[63:56], (xDM+xMDM)[7], (xDQS+xMDQS)[7]

(xECC + xMECC[7:0], (xDM+xMDM)[8], (xDQS+xMDQS)[8]

Note: x = 0, 1, 2 or 3

- All signals on a single byte lane should be equal +/- 25mils
- All byte lanes should be equal +/- 250mils

The diagram in Figure 6-11 below shows the layout of one of the data lanes.

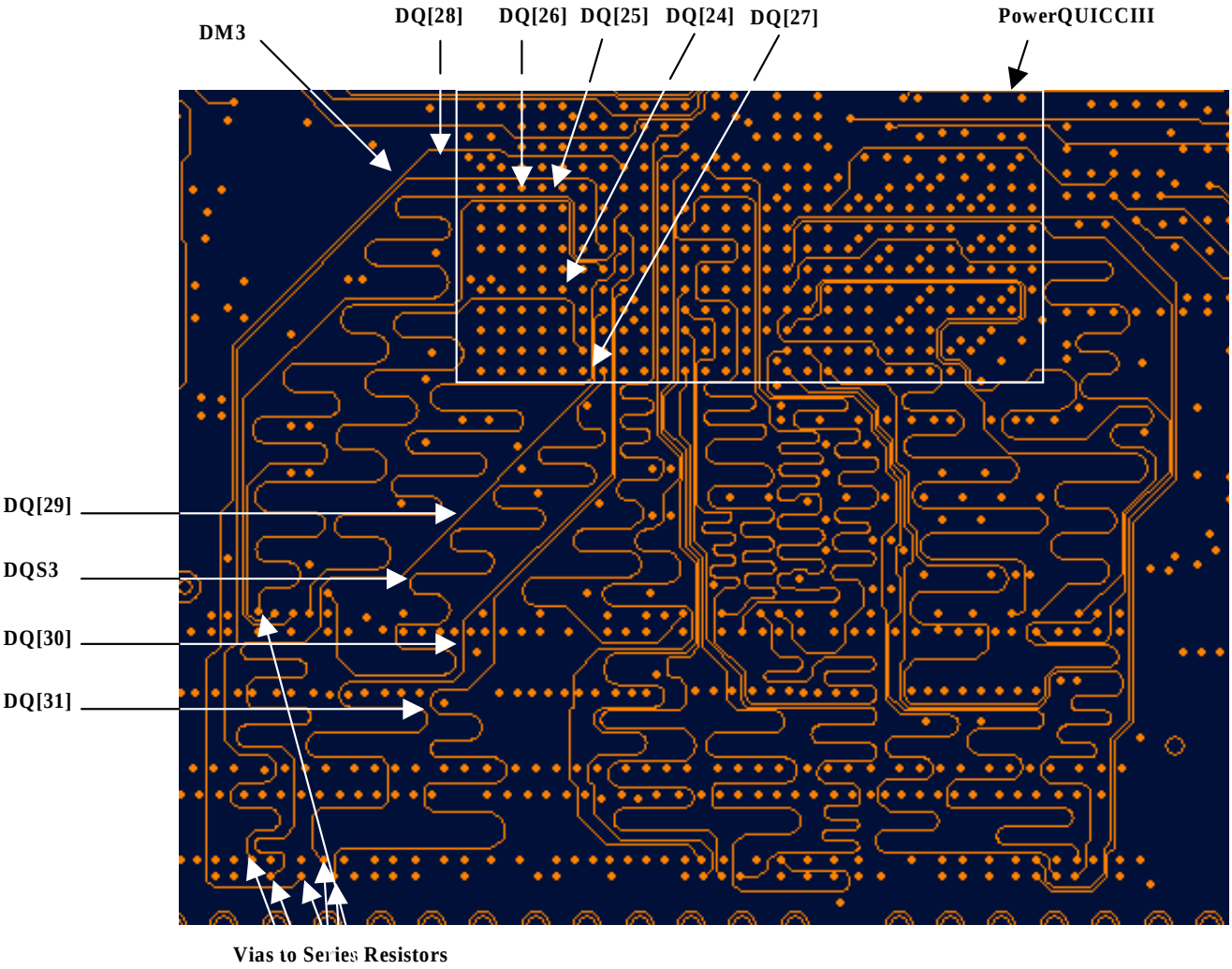


Figure 6-11. Data Layout

The diagram above shows the routing of the signals from the PowerQUICCIII to the series resistors, Rs.

6.4.3 Clocks

The processor's on chip DLLs (Delay Locked Loop) uses a PCB trace to measure how much delay is needed, so that the timing can be optimised. PCB traces allow extremely precise and predictable delays. The diagram in Figure 6-12 below shows this.

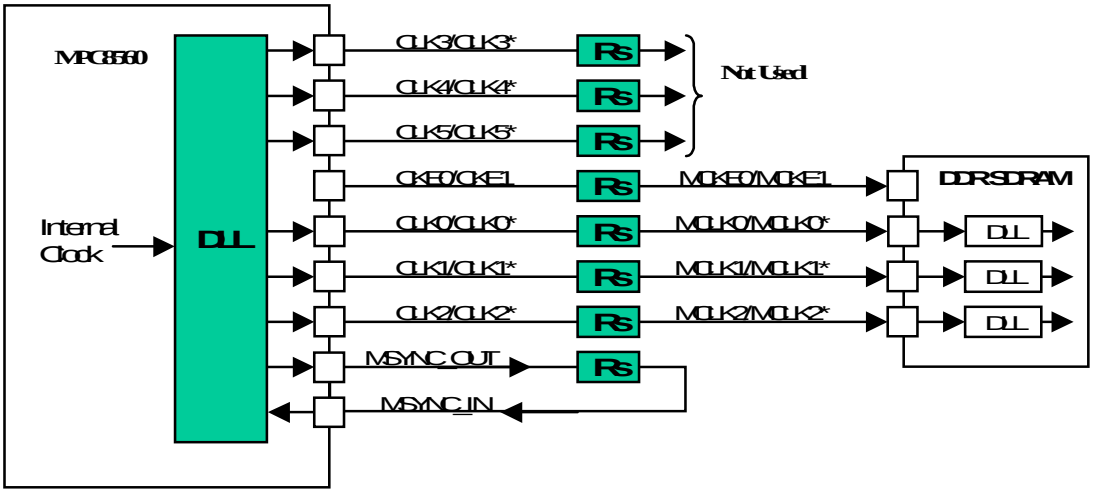


Figure 6-12. DLL Configuration

The DLL loop should exactly match the signal length of the clock path. i.e.

[MSYNC_OUT] + [MSYNC_IN] = [CLK0] + [MCLK0]

[MSYNC_OUT] + [MSYNC_IN] = [CLK0*] + [MCLK0*]

Where: CLK0 / CLK0* is the differential pair.

[x] denotes the length of signal x.

Rs is the series resistor.

Note: The same is true for any other clock pairs.

Torridon uses one SODIMM per processor to implement its DDR. This required 3 pairs of clock signals. The diagram in Figure 6-13 below shows the signals used in the clocking scheme.

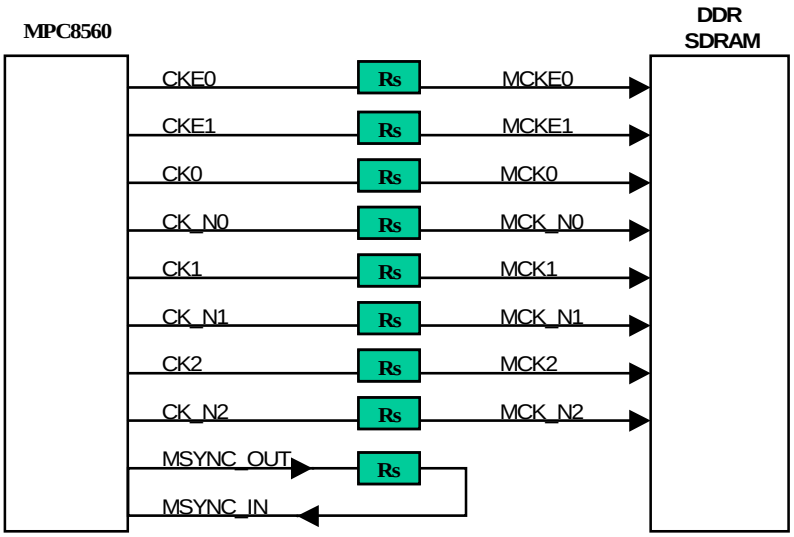


Figure 6-13. DDR Clock Signals

The following rules should be applied when laying out the clock signals.

- Clock traces should be as short as possible
- All the DDR clocks should be on the same PCB layer
- The clocks must be treated as differential pairs.
- Each clock signal must equal its differential partner +/- 10 mils.
- They must be tightly coupled and remain (as far as possible) the same distance apart.
- The clock pairs should not cross. If need be, the clock pairs can be swapped. i.e. clock pair 0 from the MPC8560 may be connected to clock pair 1 on the SODIMM. This is because all the clock pairs from the processor have identical timing.
- The clock pairs should all be equal +/- 25mils.
- The length of the clock should be equal to the length of the longest address signal.
- [MSYNC_IN] + [MSYNC_OUT] = longest clock signal +/- 10mils.

The diagram in Figure 6-14 below shows the clock routing between the processor and an SODIMM.

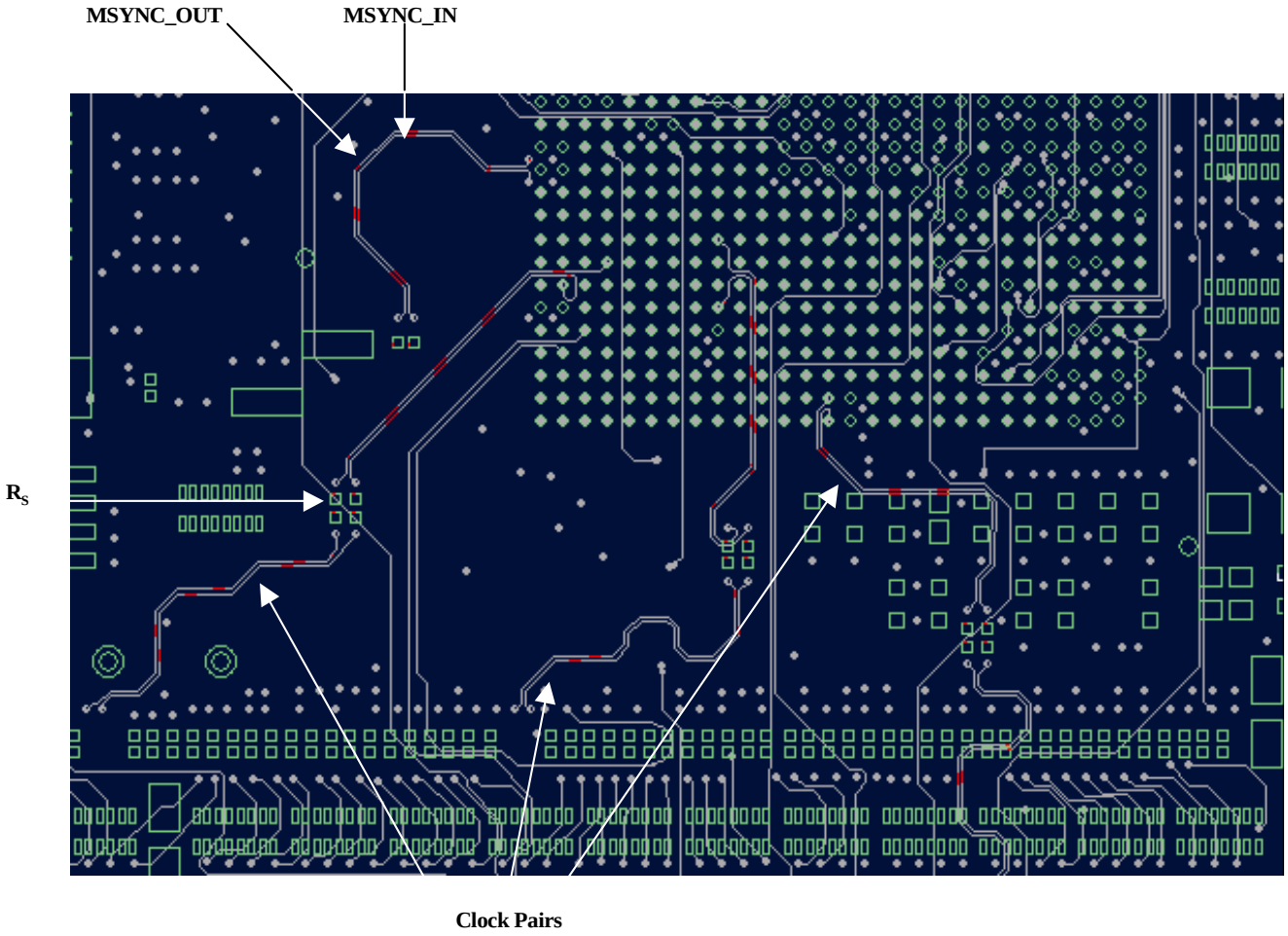


Figure 6-14. Clock Layout

6.4.4 DDR Power

The following points should be noted about the LP2995.

- AVIN and PVIN should be tied together for optimal performance. A local bypass capacitor should be placed as close as possible to the PVIN pin.
- GND should be connected to a ground plane with multiple vias for improved thermal performance.
- VSENCE, (used by the voltage regulator to monitor the voltage produced), should be connected to the V_{TT} termination bus at the point where regulation is required. For mother-board applications an ideal location would be at the centre of the termination bus.

- VDDQ can be connected remotely to the VDDQ rail input at either the DIMM or the memory controller. This provides the most accurate point for creating the reference voltage.
- V_{REF} should be bypassed with a 0.01 uF or 0.1uF ceramic capacitor for improved performance. This capacitor should be located as close as possible to the pin.

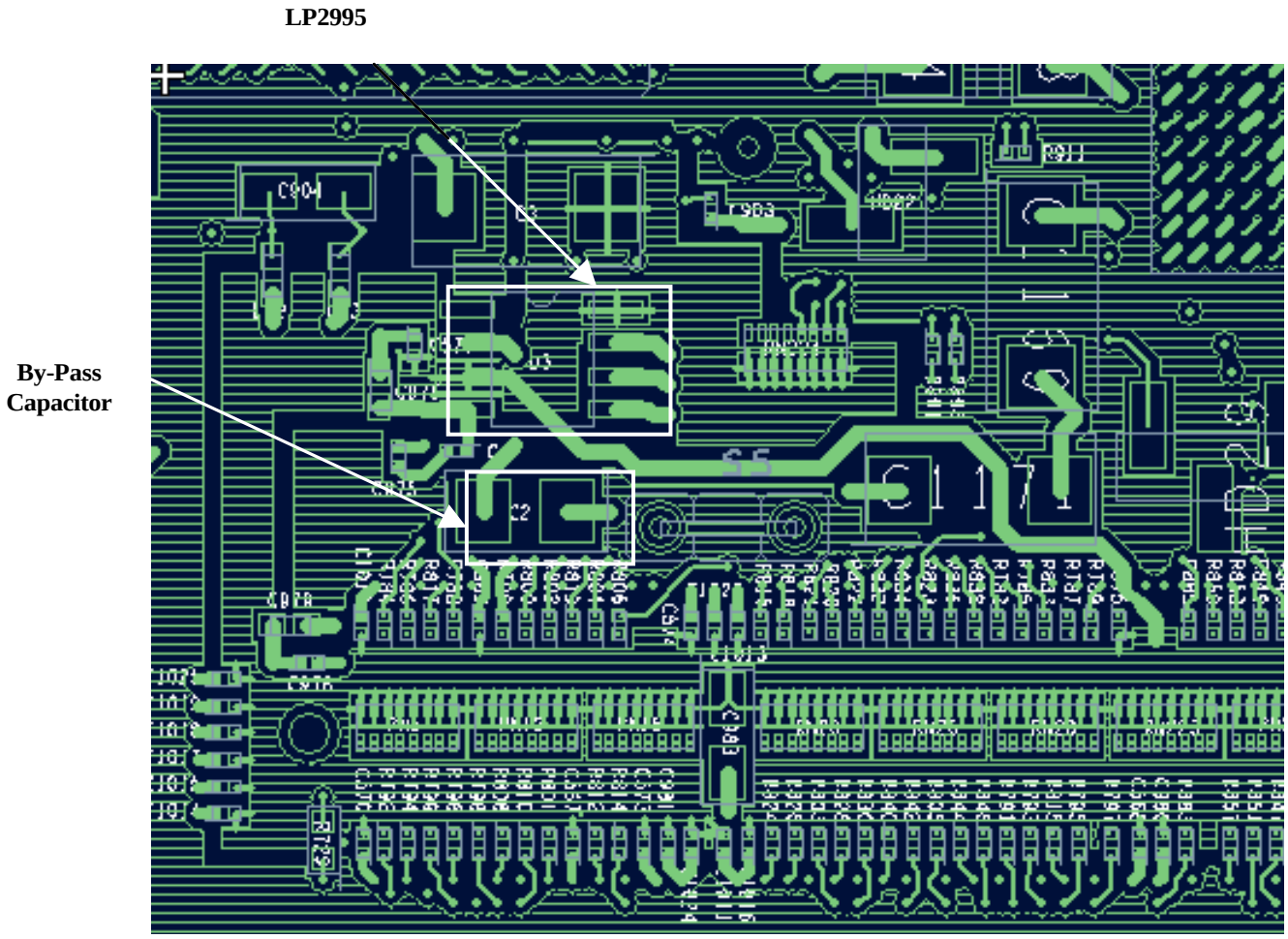


Figure 6-15. LP2995 Layout

The following points should be noted about the V_{REF} voltage reference plane.

- Use 30 mils trace between de coupling cap and destination
- Maintain a 25 mils clearance from other nets.
- Isolate VREF and/or shield with Ground.
- Decouple using distributed 0.01uf and 0.1uf capacitors by the regulator, controller, and SODIMM slot.
- Place one 0.01uf and 0.1uf near pin one of the SODIMM.
- Place one 0.1uf near the source of V_{REF}, one near the V_{REF} pin on the controller and two between the controller and the SODIMM.

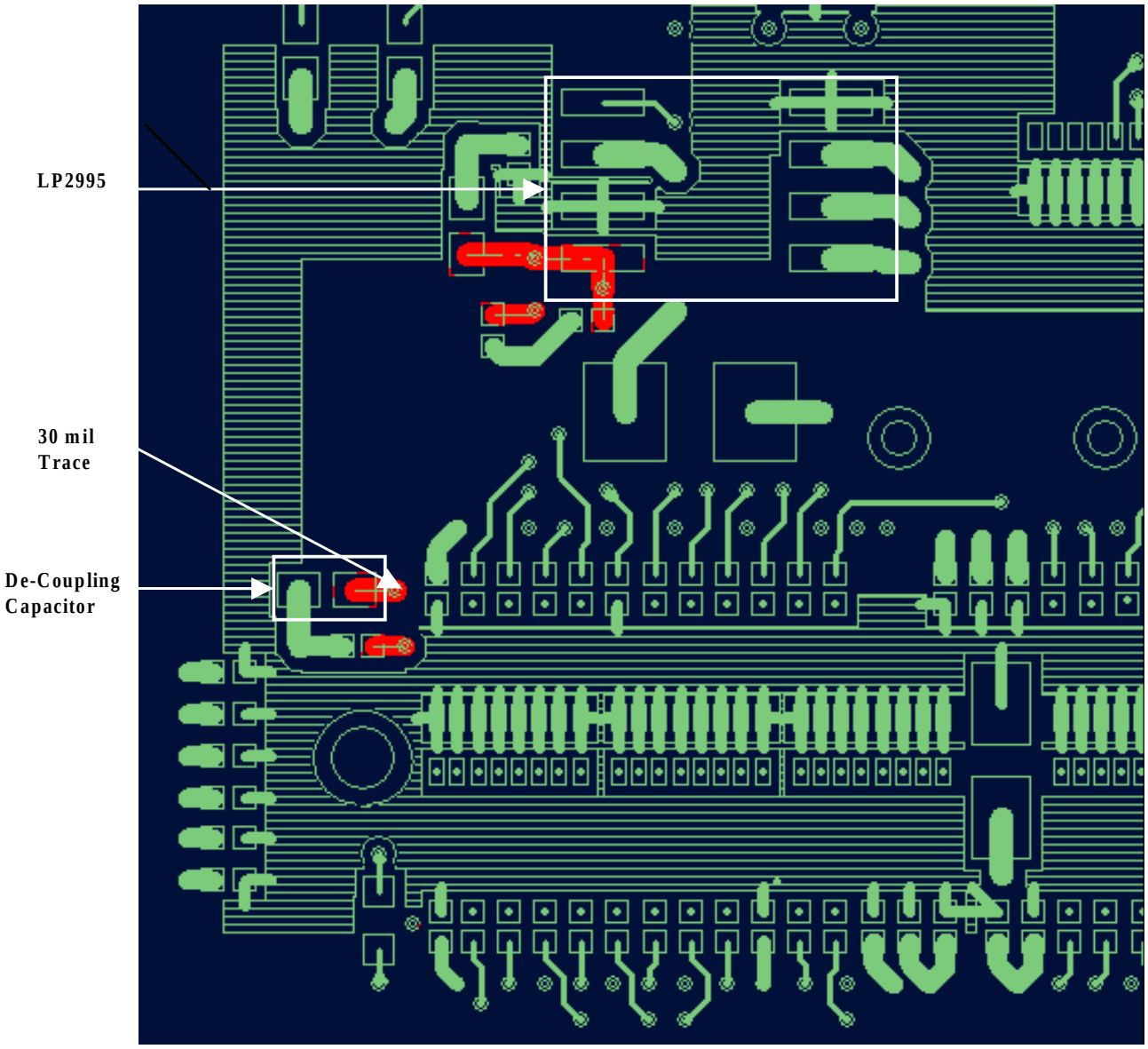


Figure 6-16. V_{REF} Layout

The following points should be noted about the V_{TT} voltage reference plane.

- Place the V_{TT} island on the component side signals layer at the end of the bus behind the DIMM slot.
- Use a wide-island trace for current capacity
- Place V_{TT} generator as close to termination resistors as possible to minimize impedance (inductance).
- Place one or two 0.1uf de coupling capacitor by each termination RPACK on the V_{TT} island to minimize the noise on V_{TT}. Other bulk (10-22uf) de coupling is also recommended to be placed on the V_{TT} island.

The diagram in Figure 6-17 below shows an example of DDR layout.

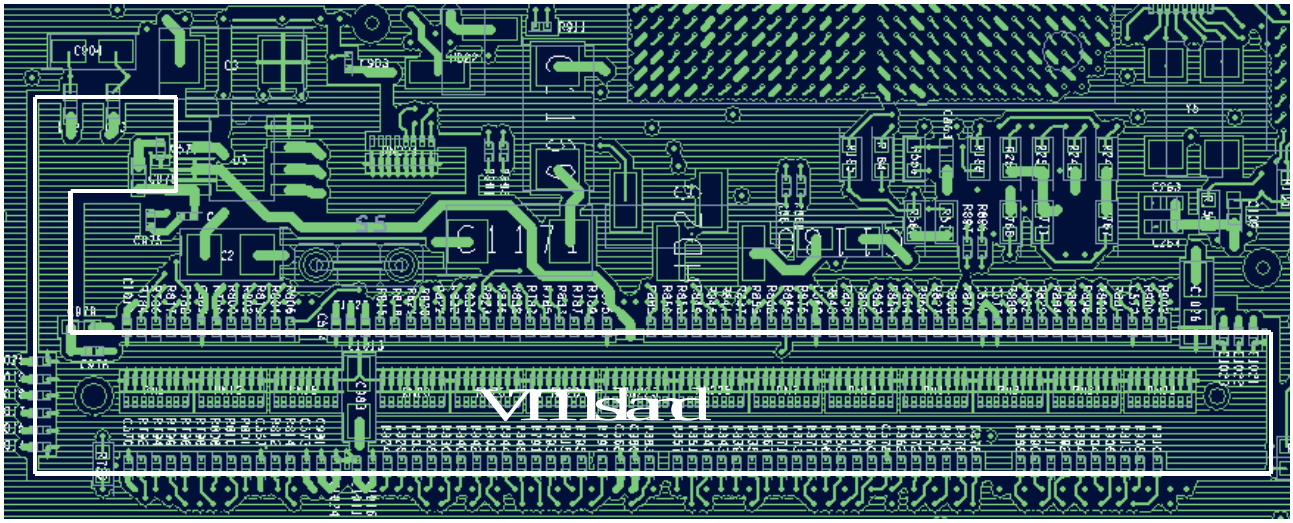


Figure 6-17. VTT Island

To ensure the voltage on the Vtt island remains constant, it is monitored by the voltage regulator. The feedback from the island should be provided by tapping off the voltage at the mid point of the island. This is shown in Figure 6-18 below.

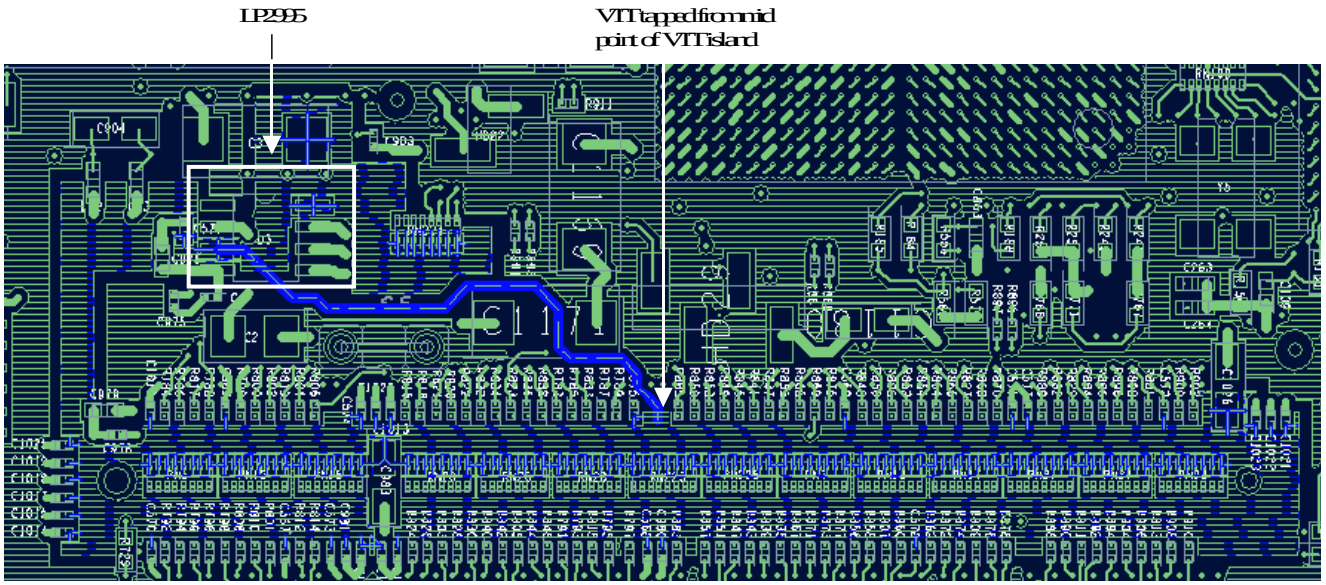


Figure 6-18. VTT Voltage Monitoring

Chapter 7 RapidIO

This section describes the RapidIO sub-section on the Torridon Motherboard.

7.1 Overview

7.1.1 RapidIO Interconnect

RapidIO is a point to point, packet switched interconnect. Developed as an open standard, the RapidIO architecture addresses the needs of present and future systems. RapidIO is focused as a processor, memory, and memory mapped I/O interface optimised for use inside a chassis.

7.1.2 The MPC8560's RapidIO Controller

The MPC8560 provides an integrated 8 bit parallel RapidIO interface which is based on the Rev 1.1 RapidIO Interconnect Specification. The port physically connects to other RapidIO devices via an 8/16 LP-LVDS (Link Protocol - Low Voltage Differential Signalling) physical layer.

The physical layer of the RapidIO unit can operate at up to 500 MHz. As the interface is defined as a source synchronous, double data rate, LVDS signaling interconnect, the theoretical unidirectional peak bandwidth is 1 Gbyte/s for an 8-bit port.

7.1.3 Signals Descriptions

RapidIO uses two distinct, uni-directional data paths; one for transmit and one for receive. Each data path is made up of the following components.

- Data Signals - The actual data being transmitted
- Clock - Used to clock the data
- Frame - Indicates the start of a frame

As RapidIO uses an LVDS interface, each signal is made up of two individual parts - the signal plus its differential compliment. Table 7-1 details the signals used for each point to point connection.

Table 7-1. RapidIO Interface Signals

Data Path	Signal Name	Description	I/O (w.r.t. Processor)
Receive	RD[7:0]/RD[7:0]*	8 Bit Wide Data	Input
	RCLK/RCLK*	Clock	Input
	RFRAME/RFRAME*	Frame	Input
Transmit	TD[7:0]/TD[7:0]*	8 Bit Wide Data	Output
	TCLK/TCLK*	Clock	Output
	TFRAME/TFRAME*	Frame	Output

7.2 Design Considerations

The following sections detail design considerations for RapidIO.

7.2.1 Signal Termination

Due to the high speed of LVDS, impedance matching is very important. Any discontinuities in the trace will cause reflections which can degrade the signal quality. The LVDS outputs need a termination resistor to close the loop. Without termination resistors, the interface will not work. The value of the termination resistor, (R_T), should match the differential impedance of the transmission line to reduce the reflections. Typically this will range from 90 ohms to 100 ohms. See Figure 7-1

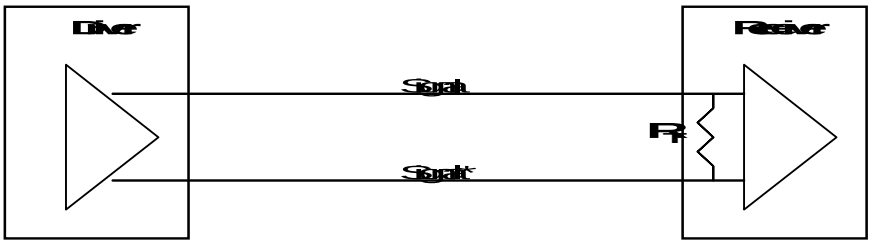


Figure 7-1. RapidIO Termination

As far as all Torridon is concerned, all of the RapidIO connections are between the MPC8560 processors and the Tundra TSI500 switch. Both the processors and the switch have the termination built in.

7.2.2 Signal Connections

The connection between each processor and the switch is very straight forward. It is simply a point to point connection. No additional components are required.

The diagram in Figure 7-2 shows the connections of the RapidIO buses on Torridon.

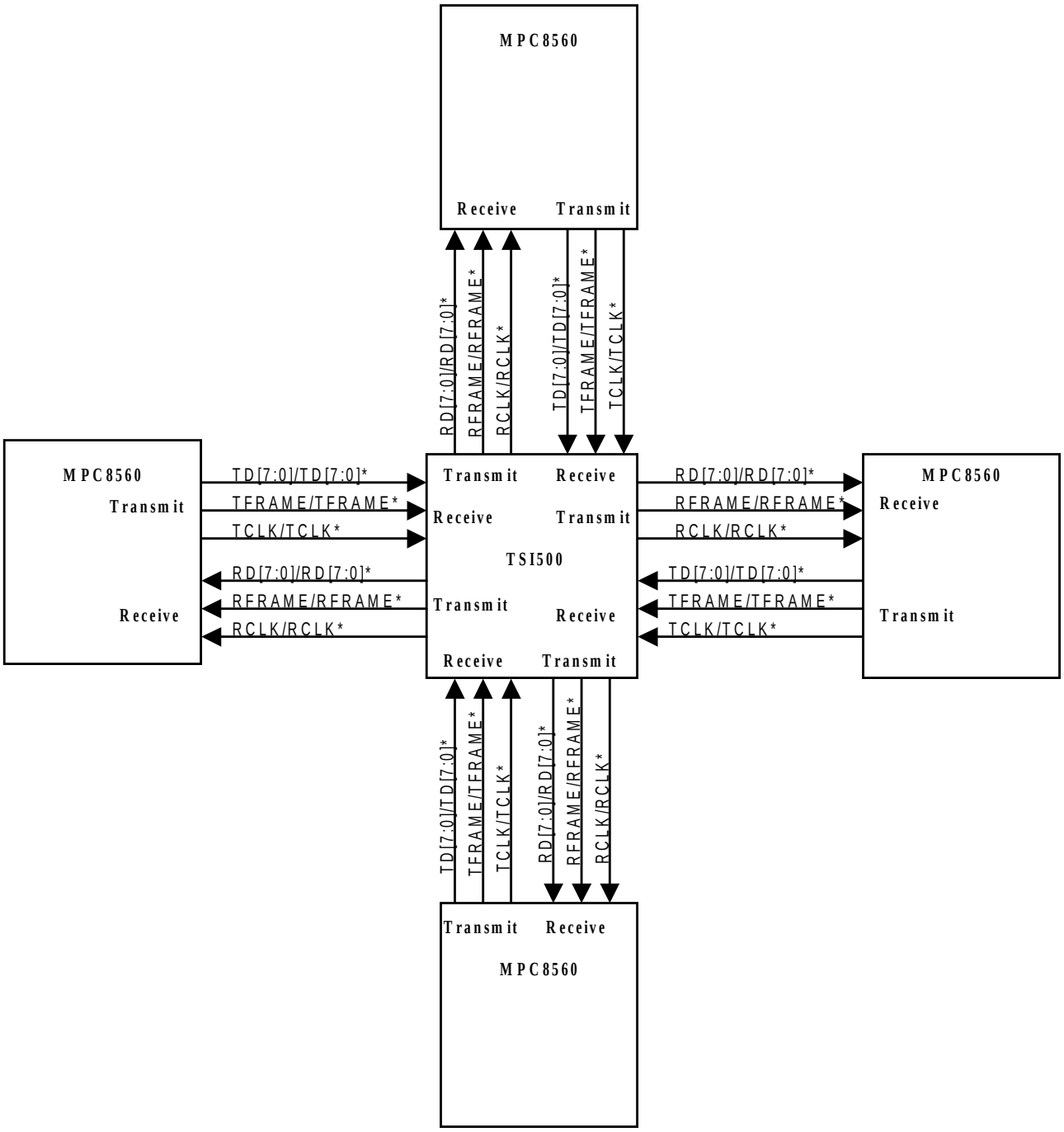


Figure 7-2. RapidIO Signal Connections

Note: The receive port on the processor connects to the transmit port of the switch and vice-versa.

Torridon uses a 4 port, parallel RapidIO switch from Tundra Semiconductor, the TSI500.

7.3 Logic Analyser Connection

To aid in the debug of RapidIO driver code and to allow the bus to be monitored, logic analyser connectors have been added to one of the RapidIO buses. Due to space constraints, it was only possible to add these connections onto one of the RapidIO buses, the one between the Boot Processor and the switch.

Torridon has been designed to support the Tektronix analyser. The TLA700 logic analyser with the TMS805 RapidIO Support Package directly supports RapidIO. See Figure 7-3.

Figure 7-3. Tektronix TLA700 System

The logic analyser connects to the motherboard using compression fit probes, the P6880. The P6880 is a 34-channel high-density compression probe with differential clock and differential data. This probe utilises a connector less probe attach mechanism for quick and reliable connection to the motherboard. See Figure 7-4.

Figure 7-4. P6880 Probes

The probes connect to the motherboard using compression fittings as shown in Figure 7-5.

Figure 7-5. Mother Board Connection

Each probe connects to a series of pads on the motherboard. As well as the 27 pads, the probe requires two holes. These holes are used to attach a back plate which ensures sufficient pressure can be applied to make a solid electrical connection. The diagram in Figure 7-6 shows the layout required for each probe.

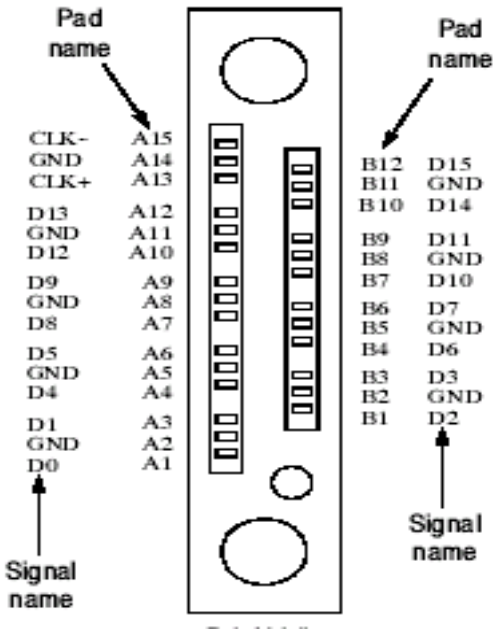


Figure 7-6. Probe Layout

7.4 Physical Connections

Four probes are required to allow access to bus, two for receive and two for transmit. On Torridon, these four probes are labelled as P30, P31, P32 & P33. Table 7-2, Table 7-3, Table 7-4, and Table 7-5 below detail the connections to these four probes.

Table 7-2. RapidIO Probe - P30

Pin#	Signal	Description
A1	RIO0_TXD0	RapidIO Transmit Data[0]
A2	GND	0 Volts
A3	RIO0_TXD0*	RapidIO Transmit Data[0]*
A4	RIO0_TXD2	RapidIO Transmit Data[2]
A5	GND	0 Volts
A6	RIO0_TXD2*	RapidIO Transmit Data[2]*
A7	RIO0_TXD4	RapidIO Transmit Data[4]
A8	GND	0 Volts
A9	RIO0_TXD4*	RapidIO Transmit Data[4]*
A10	RIO0_TXD6	RapidIO Transmit Data[6]
A11	GND	0 Volts
A12	RIO0_TXD6*	RapidIO Transmit Data[6]*
A13	RIO0_TFRAME	RapidIO Transmit Frame
A14	GND	0 Volts
A15	RIO0_TFRAME*	RapidIO Transmit Frame*
B1	RIO0_TXD1	RapidIO Transmit Data[1]
B2	GND	0 Volts
B3	RIO0_TXD1*	RapidIO Transmit Data[1]*
B4	RIO0_TXD3	RapidIO Transmit Data[3]
B5	GND	0 Volts
B6	RIO0_TXD3*	RapidIO Transmit Data[3]*
B7	RIO0_TXD5	RapidIO Transmit Data[5]
B8	GND	0 Volts
B9	RIO0_TXD5*	RapidIO Transmit Data[5]*
B10	RIO0_TXD7	RapidIO Transmit Data[7]
B11	GND	0 Volts
B12	RIO0_TXD7*	RapidIO Transmit Data[7]*

Table 7-3. RapidIO Probe - P31

Pin#	Signal	Description
A1	NC	Not Connected
A2	GND	0 Volts
A3	NC	Not Connected
A4	NC	Not Connected
A5	GND	0 Volts
A6	NC	Not Connected
A7	NC	Not Connected
A8	GND	0 Volts
A9	NC	Not Connected
A10	NC	Not Connected
A11	GND	0 Volts
A12	NC	Not Connected
A13	RIO0_TCLK	RapidIO Transmit Clock
A14	GND	0 Volts
A15	RIO0_TCLK*	RapidIO Transmit Clock*
B1	NC	Not Connected
B2	GND	0 Volts
B3	NC	Not Connected
B4	NC	Not Connected
B5	GND	0 Volts
B6	NC	Not Connected
B7	NC	Not Connected
B8	GND	0 Volts
B9	NC	Not Connected
B10	NC	Not Connected
B11	GND	0 Volts
B12	NC	Not Connected

Table 7-4. RapidIO Probe - P32

Pin#	Signal	Description
A1	RIO0_RXD0	RapidIO Receive Data[0]
A2	GND	0 Volts
A3	RIO0_RXD0*	RapidIO Receive Data[0]*
A4	RIO0_RXD2	RapidIO Receive Data[2]
A5	GND	0 Volts
A6	RIO0_RXD2*	RapidIO Receive Data[2]*
A7	RIO0_RXD4	RapidIO Receive Data[4]
A8	GND	0 Volts
A9	RIO0_RXD4*	RapidIO Receive Data[4]*
A10	RIO0_RXD6	RapidIO Receive Data[6]
A11	GND	0 Volts
A12	RIO0_RXD6*	RapidIO Receive Data[6]*
A13	RIO0_RFRAME	RapidIO Receive Frame
A14	GND	0 Volts
A15	RIO0_RFRAME*	RapidIO Receive Frame*
B1	RIO0_RXD1	RapidIO Receive Data[1]
B2	GND	0 Volts
B3	RIO0_RXD1*	RapidIO Receive Data[1]*
B4	RIO0_RXD3	RapidIO Receive Data[3]
B5	GND	0 Volts
B6	RIO0_RXD3*	RapidIO Receive Data[3]*
B7	RIO0_RXD5	RapidIO Receive Data[5]
B8	GND	0 Volts
B9	RIO0_RXD5*	RapidIO Receive Data[5]*
B10	RIO0_RXD7	RapidIO Receive Data[7]
B11	GND	0 Volts
B12	RIO0_RXD7*	RapidIO Receive Data[7]*

Table 7-5. RapidIO Probe - P33

Pin#	Signal	Description
A1	NC	Not Connected
A2	GND	0 Volts
A3	NC	Not Connected
A4	NC	Not Connected
A5	GND	0 Volts
A6	NC	Not Connected
A7	NC	Not Connected
A8	GND	0 Volts
A9	NC	Not Connected
A10	NC	Not Connected
A11	GND	0 Volts
A12	NC	Not Connected
A13	RIO0_RCLK	RapidIO Receive Clock
A14	GND	0 Volts
A15	RIO0_RCLK*	RapidIO Receive Clock*
B1	NC	Not Connected
B2	GND	0 Volts
B3	NC	Not Connected
B4	NC	Not Connected
B5	GND	0 Volts
B6	NC	Not Connected
B7	NC	Not Connected
B8	GND	0 Volts
B9	NC	Not Connected
B10	NC	Not Connected
B11	GND	0 Volts
B12	NC	Not Connected

Note: There are four distinct RapidIO busses on Torridon. Each bus is labelled RIOx_yyy where x is the bus number (0, 1, 2, or 3) and yyy is the signal name. (e.g. RCLK, TFRAME etc.)

RIO0 is the bus between the Boot Processor and the switch; RIO1 is the bus between Work Processor 1and the switch etc.

7.5 Layout Considerations

RapidIO uses differential signalling. This means that each individual signal is actually two separate wires. Care must be taken when routing these signals.

- The signals should be tightly coupled together.
- Each signal should be equal to its complimentary signal to within a tolerance of +/- 10mils (0.02mm)
- Within a particular receive or transmit path, all signals should be equal to within a tolerance of +/- 50mils (0.1mm)
- The number of vias on any differential pair must be less than or equal to 4
- The transmit signal path should routed on a separate layer to the receive signal path
- RapidIO signals should be routed on a different plane than single ended signals
- Each of the four RapidIO busses on Torridon (RIO0_yyy, RIO1_yyy, RIO2_yyy and RIO3_yyy) are totally independent. There is no requirement to match signals between busses
- Within each RapidIO bus, the transmit and receive paths can be treated as independent. There is no requirement to match signals between receive and transmit paths
- The length of the bus should not exceed 3 inches.

The board shots in Figure 7-7 show some examples of RapidIO routing on Torridon.

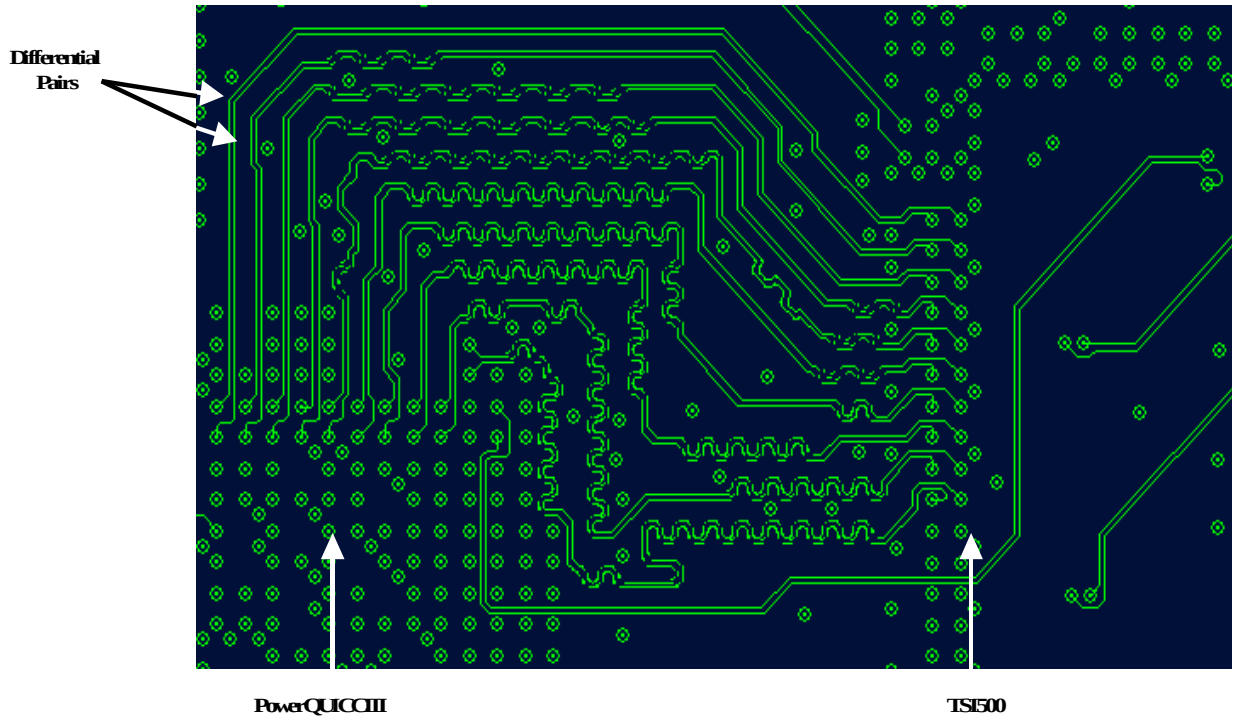


Figure 7-7. RapidIO Receive Path Layout

The diagram above shows a receive path between one of the MPC8560's and the TSI500 switch. Note that each signal pair has been tightly coupled and effectively routed as a single signal. Also note that the shortest signal has been lengthened to match the longest signal length.

The board shot above shows layer 8 of the PCB. The transmit path for this connection is routed separately on layer 11.

The diagram in Figure 7-8 shows the routing between the Boot Processor and the switch. This path incorporates the probes for the logic analyser.

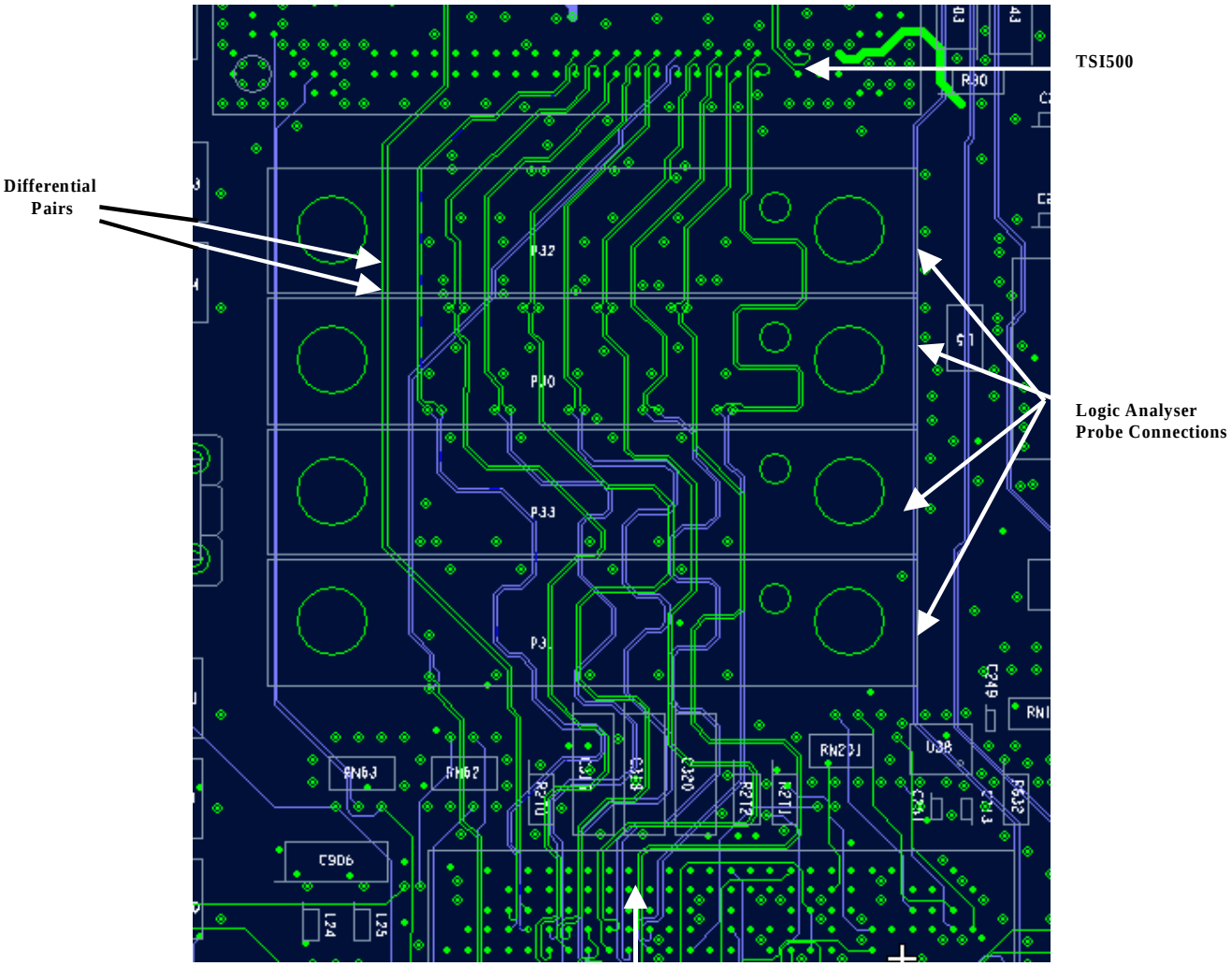


Figure 7-8. RapidIO Receive Path Layout (With Logic Probes)

Chapter 8 GBit Ethernet

This section describes the GBit Ethernet sub-section on the Torridon Motherboard.

8.1 Overview

Torridon provides five GBit Ethernet ports. The Boot Processor provides two of these ports, the other three are provided by each of the Work Processors. Connection to the outside world is made via IEEE 802.3 compliant twisted pair (T.P.) ports (10/100/1000-BaseT). Each port is controlled by the MPC8560's triple speed Ethernet controller (TSEC). The TSEC incorporates a MAC that supports 10, 100,and 1000 Mbps Ethernet/802.3 networks. The TSEC includes address/data filtering, data insertion and extraction, 2-kbyte FIFOs, and DMA functions.The TSEC network interface supports multiple options. One is the Media Independent Interface (MII) option which uses 18 I/O pins and supports both data and a management interface to the PHY. The MII supports both 10 and 100 Mbps. The GBit Media Independent Interface (GMII) option is a super-set of the MII signals and supports data rates up to 1000Mbps.

8.2 GBit Ethernet Connection

The diagram in Figure 8-1 shows the basic parts to allow the MPC8560 to interface to the outside world via GBit Ethernet.

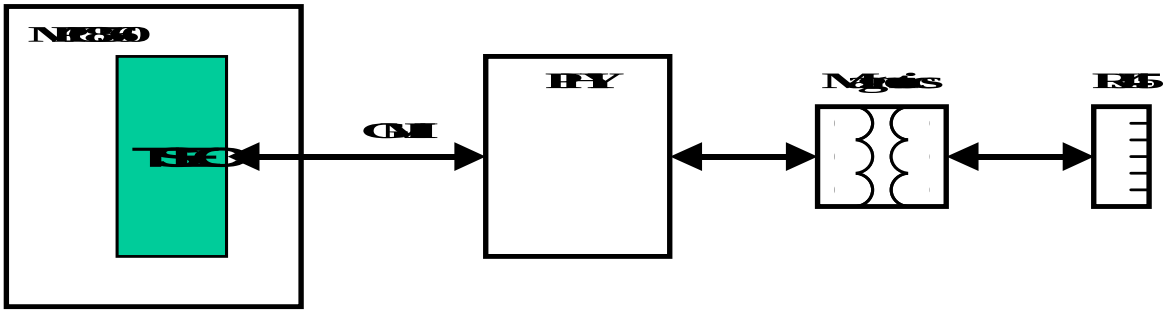


Figure 8-1. GBit Ethernet Connection

The MPC8560's Triple Speed Ethernet Controller (TSEC) connects to the Ethernet physical device (PHY) via a GBit Media Independent Interface (GMII). Electrical isolation is provided between the PHY and the external connector, (RJ45), via a magnetic circuit. Each of these blocks will be discussed in more detail below.

8.3 GMII Interface

As 1000Mbps data rates are supported on Torridon, the GMII interface is used to interface the processor's TSEC to its respective PHY device. Table 8-1 and Figure 8-2 detail the signals used in the GMII interface.

Table 8-1. TSEC GMII Interface Signals

Signal	Description	I/O (w.r.t. Processor)
COL	Collision	Input
CRS	Carrier Sense	Input
GTX_CLK	GBit Transmit Clock	Output
GTX_CLK125	GBit Transmit 125MHz Source	Input
MDC	Management Data Clock	Output
MDIO	Management Data Input/Output	Input/Output
RX_CLK	Receive Clock	Input
RX_DV	Receive Data Valid	Input
RXD[7:0]	Receive Data	Input
RX_ER	Receive Error	Input
TX_CLK	Transmit Clock	Input
TXD[7:0]	Transmit Data	Output
TX_EN	Transmit Enable	Output
TX_ER	Transmit Error	Output

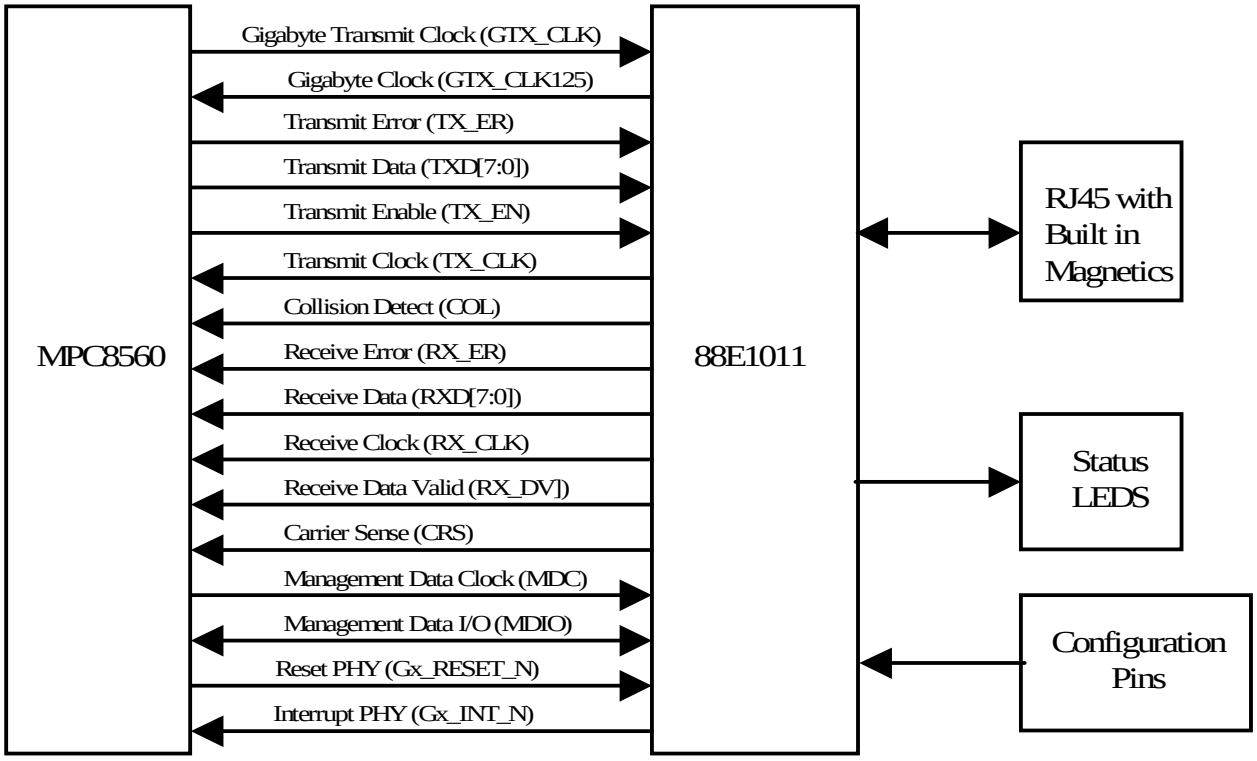


Figure 8-2. GMII Interface

8.4 PHY Device

The Marvell 88E1011 device provides the physical interface for the Ethernet connection on Torridon. The 88E1011 connects to the TSEC via the GBit Media Independent Interface, GMII, which is used for both the device's control and data path.

The PHY may be reset independently by a general purpose pin on the MPC8560. It may also be reset by setting the most significant bit in the 88E1011's control register via the MII management interface.

Each PHY has the ability to interrupt the MPC8560 by the assertion of its respective interrupt (*INT) pin. The polarity of this interrupt is programmable.

The initial power on status of the PHY is determined by seven configuration pins, CONFIG[6:0]. These pins determine various initial setting such as the PHY address, connection speed etc. Table 8-2 details the possible settings.

Table 8-2. PHY Configuration Pins

Pin	Bit[2]	Bit[1]	Bit[0]
Config0	PHYADR[2]	PHYADR[1]	PHYADR[0]
Config1	ENA_PAUSE	PHYADR[4]	PHYADR[3]
Config2	ANEG[3]	ANEG[2]	ANEG[1]
Config3	ANEG[0]	ENA_XC	DIS_125
Config4	HWCFG_MODE[2]	HWCFG_MODE[1]	HWCFG_MODE[0]
Config5	DIS_FC	DIS_SLEEP	HWCFG_MODE[3]
Config6	SEL_BDT	INT_POL	75/50 Ohm

Note: Refer to the 88E1011 Data Sheet for full details of the settings available

Each configuration pin defines three configuration bits. The three bit value is determined by tying the configuration pin to one of the other pins on the device.

Table 8-3 details the pins used to set the values of the configuration pins.

Table 8-3. Setting PHY Configuration Pins

Pin	Bit[2:0]
VDD0	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

For example to set Config0 to 101, it must be connected to the LED_LINK100 pin.

Each one of the configuration pins must be tied to the appropriate pin. On Torridon each one of the PHY are configured as shown in Table 8-4.

Table 8-4. PHY Configuration Pins on Torridon

Pin	Connected to	Bit[2:0]
Config0	VSS	000
Config1	VSS	000
Config2	LED_LINK10	110
Config3	VSS	000
Config4	VDD0	111
Config5	VDD0	111
Config6	VSS	000

This sets the PHYs up in the following initial state.

- PHY address set to 0 [1]
- MAC Pause is not implemented
- Auto negotiate - advertise all capabilities, force master operation
- Disable MDI crossover
- Enable generation of the 125MHz clock
- Configure device to run in GMII to copper mode
- Disable energy detect
- Disable fibre/copper selection
- Select the MDC/MDIO interface
- Select the interrupt to be active high
- Select 50 ohm termination to fibre. (Note: This is irrelevant as there is no support for fibre on Torridon)

[1] Note: The second PHY on the Boot Processor is set to address 1 by connecting Config0 pin to LED_TX instead of VSS. All the other PHYs have an address of 0.

8.5 Magnetics & RJ45

The PHY device provides an eight pin media dependent interface (MDI[3:0]+/-). This interface is made up of four differential pairs of signals which, via the magnetics, provide the connection to the RJ45 connector.

On Torridon, the magnetics and the RJ45 connector are integrated on a single device. As well as simplifying the design, this is a more space efficient solution. The device also includes two built in LEDs. See Figure 8-3 and Table 8-5.

Figure 8-3. RJ45 with Integrated Magnetics

Table 8-5. Ethernet Connections

Pin#	Signal	Description
1	Tx+	Transmit Data +ve
2	Tx-	Transmit Data -ve
3	Rx+	Receive Data +ve
4	GND	0 Volts
5	GND	0 Volts
6	Rx-	Receive Data -ve
7	GND	0 Volts
8	GND	0 Volts

8.6 Layout Considerations

As far as layout was concerned, the routing of the signals on the GMII bus (between the MPC8560 and the PHY), was not overly critical.

Due to the fact that the PHY is situated close to the processor and the interface is digital, apart for following sound layout guidelines, no additional constraints were imposed on this interface.

However, the MDI bus between the PHY and the magnetics was more critical due to the relatively long signal lengths involved. The following constraints were imposed on the layout of the MDI bus.

- Each pair (e.g. Tx+ and TX-) should be routed so they are tightly coupled in the same layer and the separation between the two traces of the pair should remain constant over the entire length
- The signals in a pair should be equal in length to within a tolerance of +/- 10 mils (0.02mm)

- The signals across the bus should be equal in length to within a tolerance of +/- 50 mils (0.1mm)
- The number of vias on any signal should be less than or equal to 4. See Figure 8-4 below.

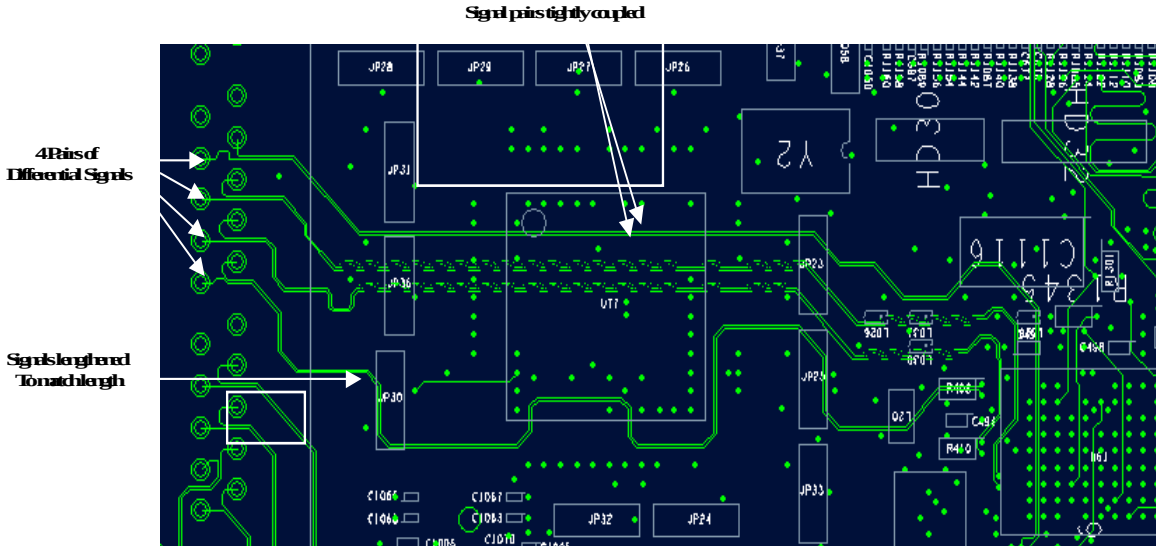


Figure 8-4. MDI Bus Layout

Chapter 9 UART

This section describes the UART sub-section on the Torridon Motherboard.

9.1 Overview

Each of the processors support a single RS232 port. The MPC8560's SCC1 controller with a MAX3229 level translator, implements the standard RS232 serial I/O protocol. A DB9 connector is attached to the front of the board provides access to the boot processor's serial port. The serial ports for the three work processors are accessible on three separate headers. See Figure 9-1.

Note the additional SCC control signals, Request to Send (RTS), Carrier Detect (CD) and Clear to Send (CTS) are not connected hence hardware flow control is not supported on this interface.

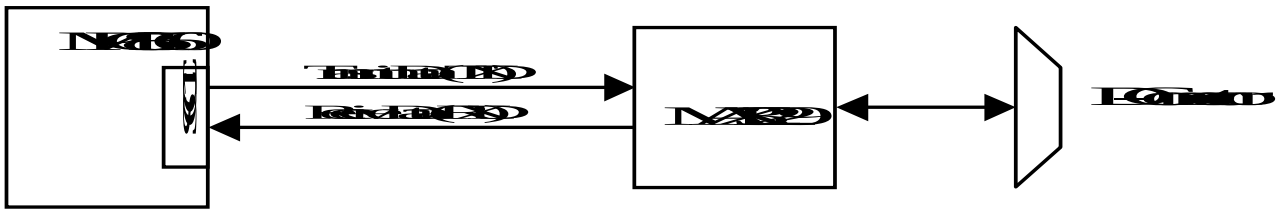


Figure 9-1. RS232 Interface

Table 9-1 shows the port usage on the MPC8560 for the serial ports.

Table 9-1. Specific MPC8560 - UART Signals

Signal	MPC8560 Pin	Description	I/O (w.r.t. Processor)
SCC1_RXD	PD[31]	RS232 Receive Data	Input
SCC1_TXD	PD[30]	RS232 Transmit Data	Output

Note: These signals are pin compatible with the MPC8540's DUART controller. This means that the MPC8560 may be replaced with an MPC8540 and the RS232 interface will still function.

Connection to the debug port is made via a standard 9 pin d-type connector. The pin out is shown in Table 9-2.

Table 9-2. RS232 Connector

Pin#	Signal	Connection
1	CD	Not connected
2	RXD	To SCC1 TXD
3	TXD	To SCC1 RXD
4	DTR	Not connected
5	GND	0 Volts
6	DSR	Not connected
7	RTS	Not connected
8	CTS	Not connected
9	RI	Not connected

The schematics are shown in Figure 9-2 and Figure 9-3.

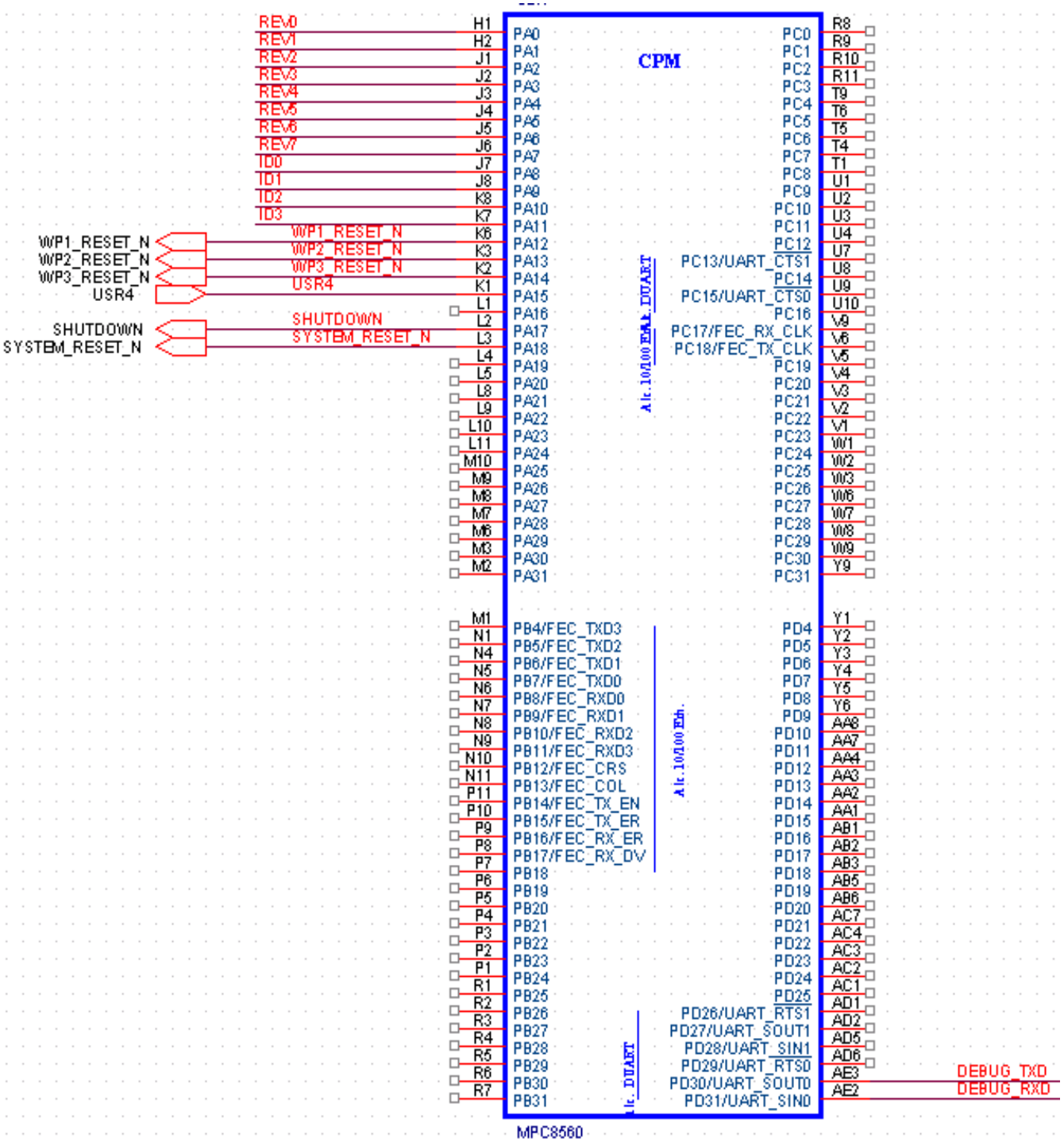


Figure 9-2. MPC8560 CPM

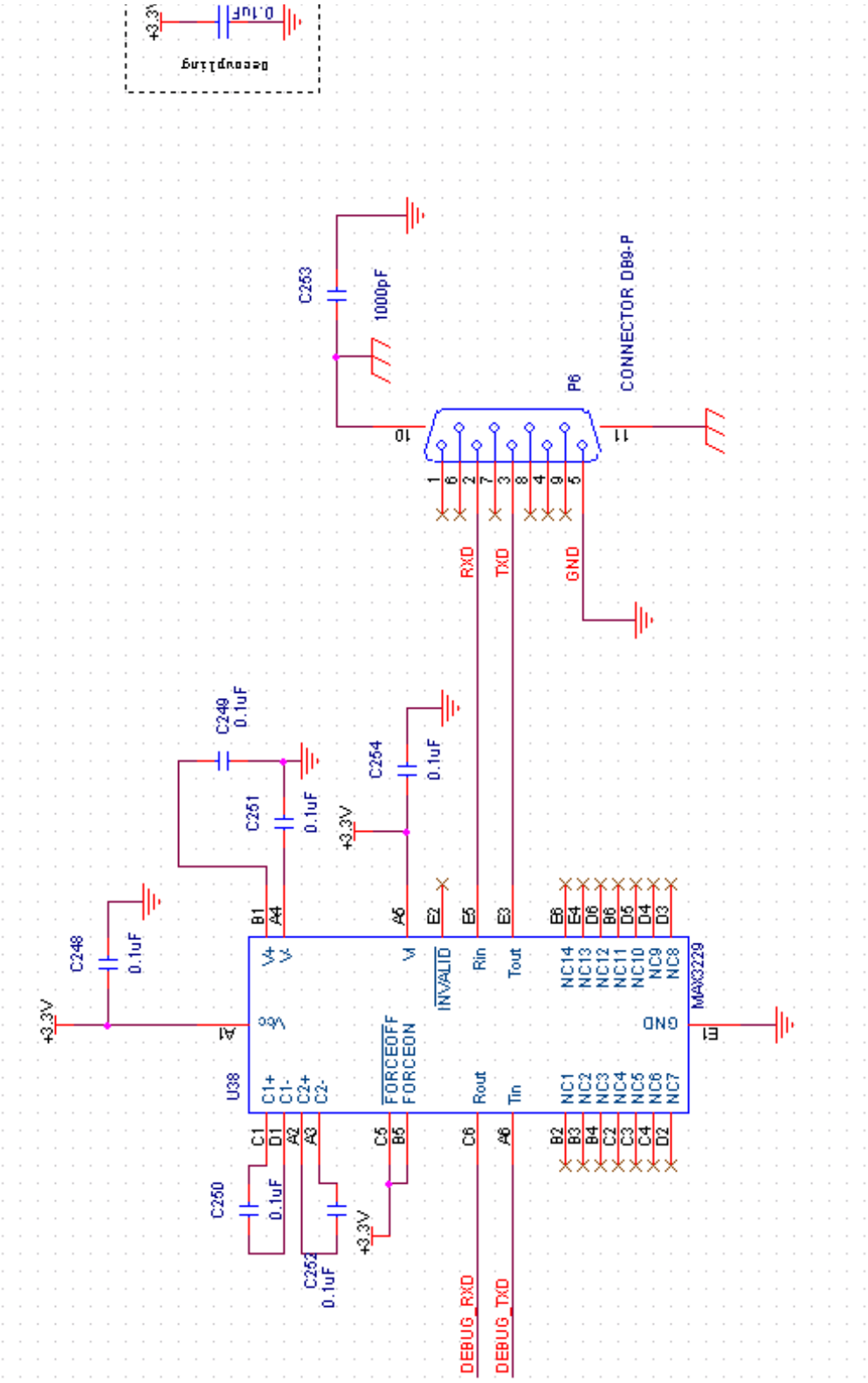


Figure 9-3. RS232 Transceiver

The following should be noted about the schematics:

- Only the DEBUG_RXD and DEBUG_TXD signals from the CPM are used to drive the RS232 interface. The other signals shown in the schematics are to control/monitor other devices on Torridon.
- The small package size of the MAX3229 helps limit board space

Chapter 10 PCI

This section describes the PCI sub-section on the Torridon Motherboard.

10.1 Overview

Although Torridon supports four processors, only one of the PCI busses available is utilised. The boot processor provides a single 64 bit PCI slot. The PCI busses on the three Work Processors are not used, these busses are simply left as no connects on the motherboard.

As well as providing a 64 bit PCI slot, the Boot Processor also provides an interface to the Via Southbridge chip. This interface is further discussed in Chapter 11, “Peripheral Support”. The diagram in Figure 10-1 details the connection to the Boot Processor’s PCI bus.

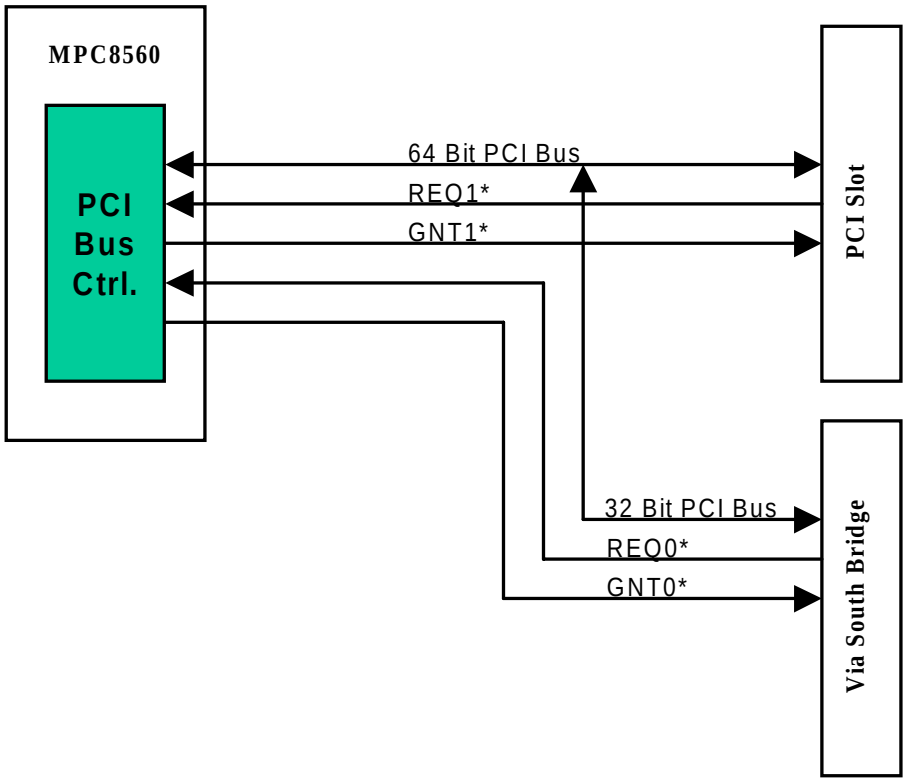


Figure 10-1. Boot Processor’s PCI Bus

The PCI connection to the PCI slot and the Via chip are very similar with a few notable differences.

- Each “peripheral” uses a separate request/grant pair. The Via chip uses REQ0#/GNT0#, the PCI slot uses REQ1#/GNT1#
- The Via chip only uses 32 bits of the 64 bit bus.

10.2 PCI Clocks

In terms of clocks, the PCI bus sees three separate devices.

- The MPC8560
- The PCI slot
- The Via chip

All three devices are driven from a single 33MHz clock oscillator. The oscillator is passed through a fan out buffer to provide sufficient drive capability.

Refer to Section 14.2, “System Clocks” for details.

10.3 Bus Connectivity

For the majority of the PCI signals, a straight point to point connection is made between the Boot processor, the interface connector and the Via chip.

10.4 PCI Configuration

The PCI interface on the Torridon board can be configured via switch settings. These switches are used to configure the following.

- The impedance of the interface
- Switch between 32 and 64 bit mode
- Enable/disable the internal arbitration unit
- Enable/disable the PCI debug feature

Refer to Section 4.2, “MPC8560 Processor Configuration” for details.

10.5 Schematics

The diagrams in Figure 10-2 and Figure 10-3 show the schematics pertaining to the PCI bus.

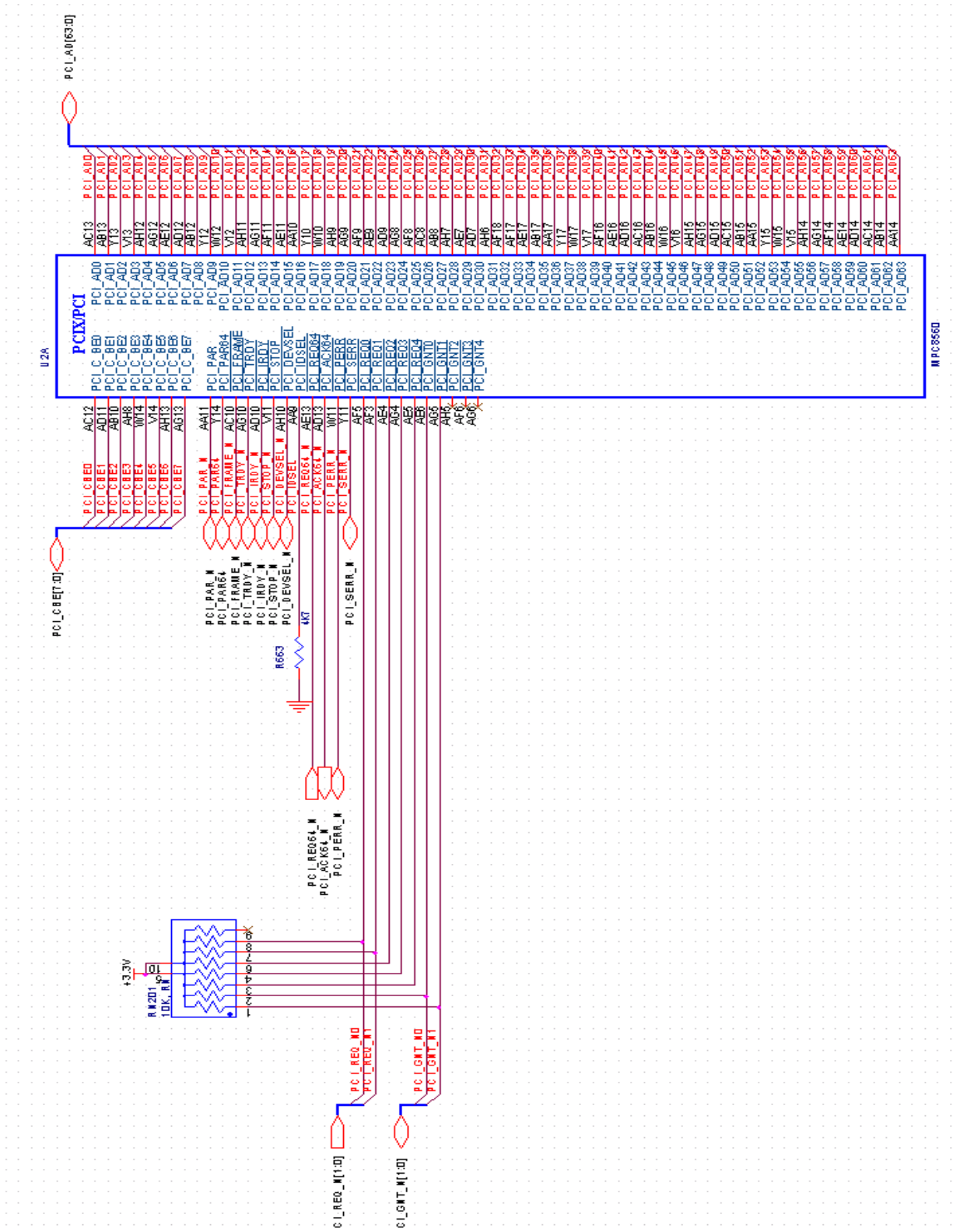


Figure 10-2. MPC8560's PCI Interface - Schematics

The following should be noted about the circuitry.

- To guard against spurious requests/acknowledges, pull-ups are added to the request/acknowledge lines
- Pull-ups are added to the unused request inputs.
- As the processor is the host, which initiates the PCI transactions, the IDSEL pin is pulled low. This will guard against it replying to one of its own bus transactions.

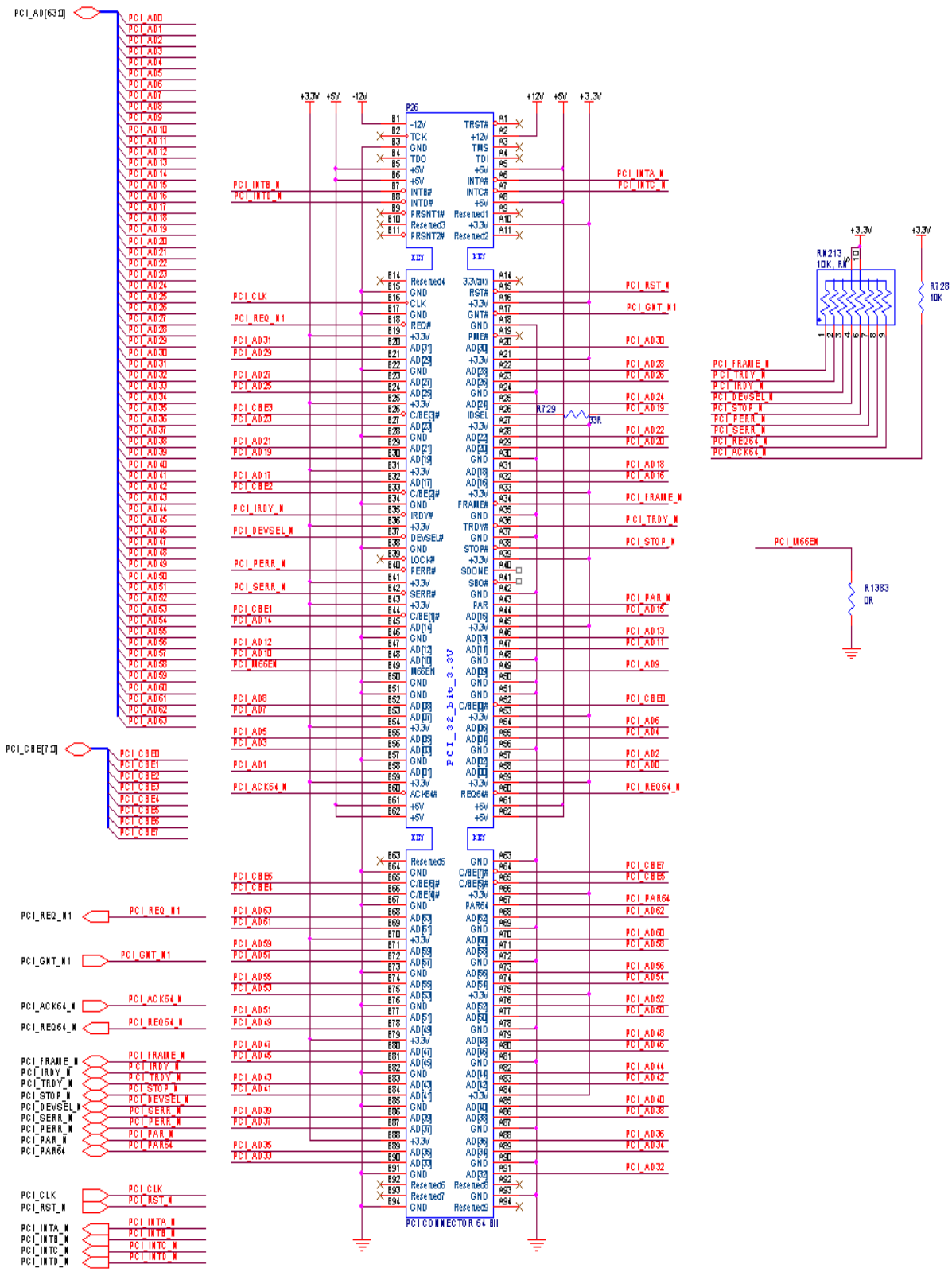


Figure 10-3. PCI Slot - Schematics

The following should be noted about the circuitry.

- Control signals are pulled up
- As the PCI bus on the MPC8560 is 3.3V only, the I/O voltage is set to 3.3V
- As the PCI bus is limited to 33MHz (This is the maximum speed of the Via chip), the M66EN signal, which advertises bus speed capability, is tied to 33MHz.
- The IDSEL pin, which sets the address range for this PCI slot, is tied to address pin 19. (This must be a unique address space on the bus)

Chapter 11 Peripheral Support

This section describes the Peripheral sub-section on the Torridon Motherboard.

11.1 Overview

The “Super South” South Bridge (VT82C686) from Via Technologies provides additional IO on Torridon; namely IDE, USB and PS2 interfaces.

The South Bridge is connected directly to the PCI bus on the boot processor. Please refer to Chapter 10, “PCI” for details of the interface.

11.2 IDE Interface

Two IDE interfaces, the Primary and the Secondary, are provided on Torridon. These are available at two separate 40 pin connectors, P23 and P24.

The IDE interfaces are driven directly from the Via Southbridge device. The schematics are shown in Figure 11-1 and Figure 11-2.

The following should be noted about the schematics

- Series resistors are used to smooth out over/under shoots
- A 2 pin header (HD23) allows a front panel LED to be added which will indicate when the IDE interface is active.
- An inverter is added on the reset drive signal (RSTDRV) to switch the polarity. (The RSTDRV signal from the Via is active high, the IDE interface expects and active low signal)

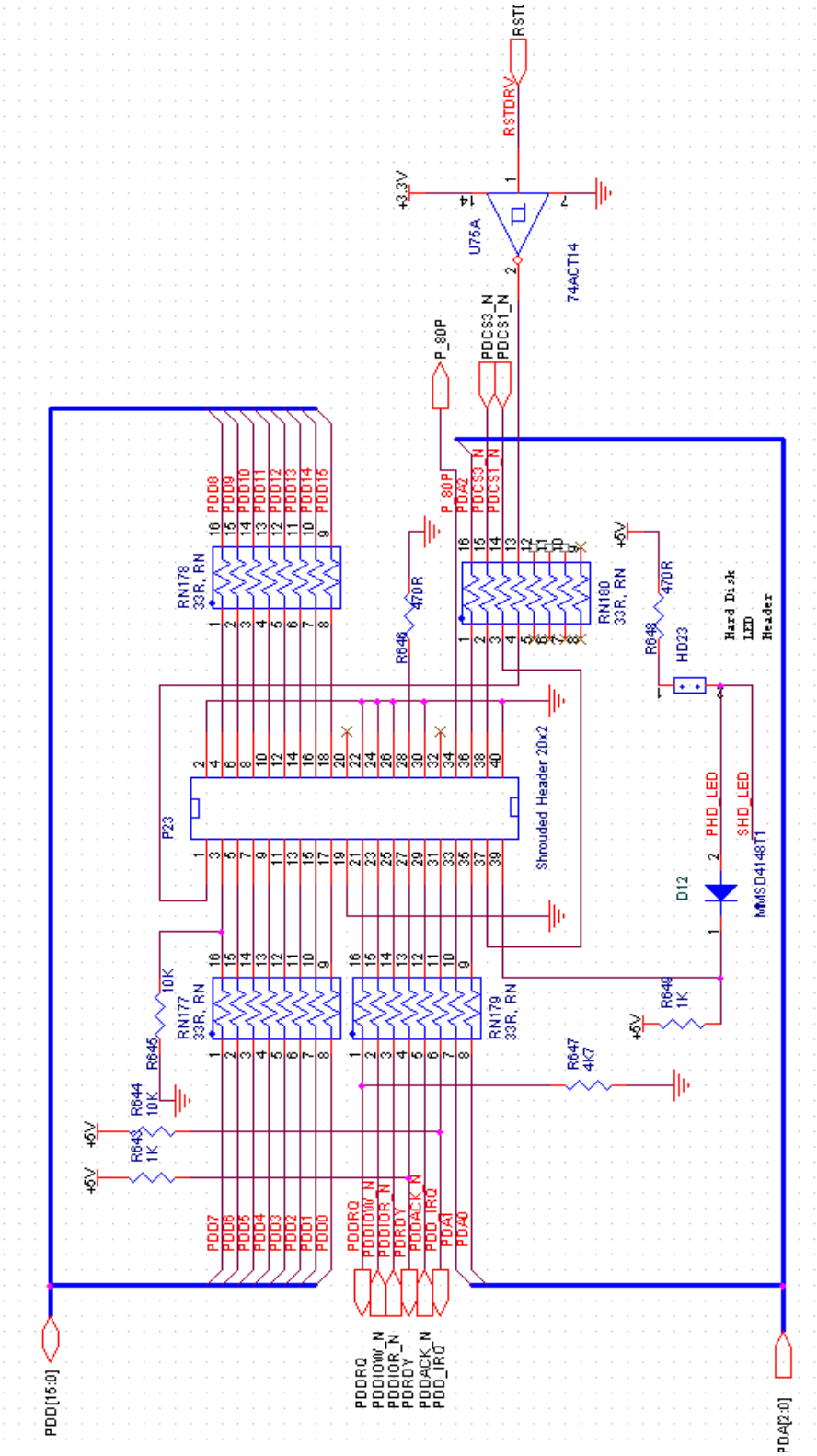


Figure 11-1. Primary IDE Interface - Schematics

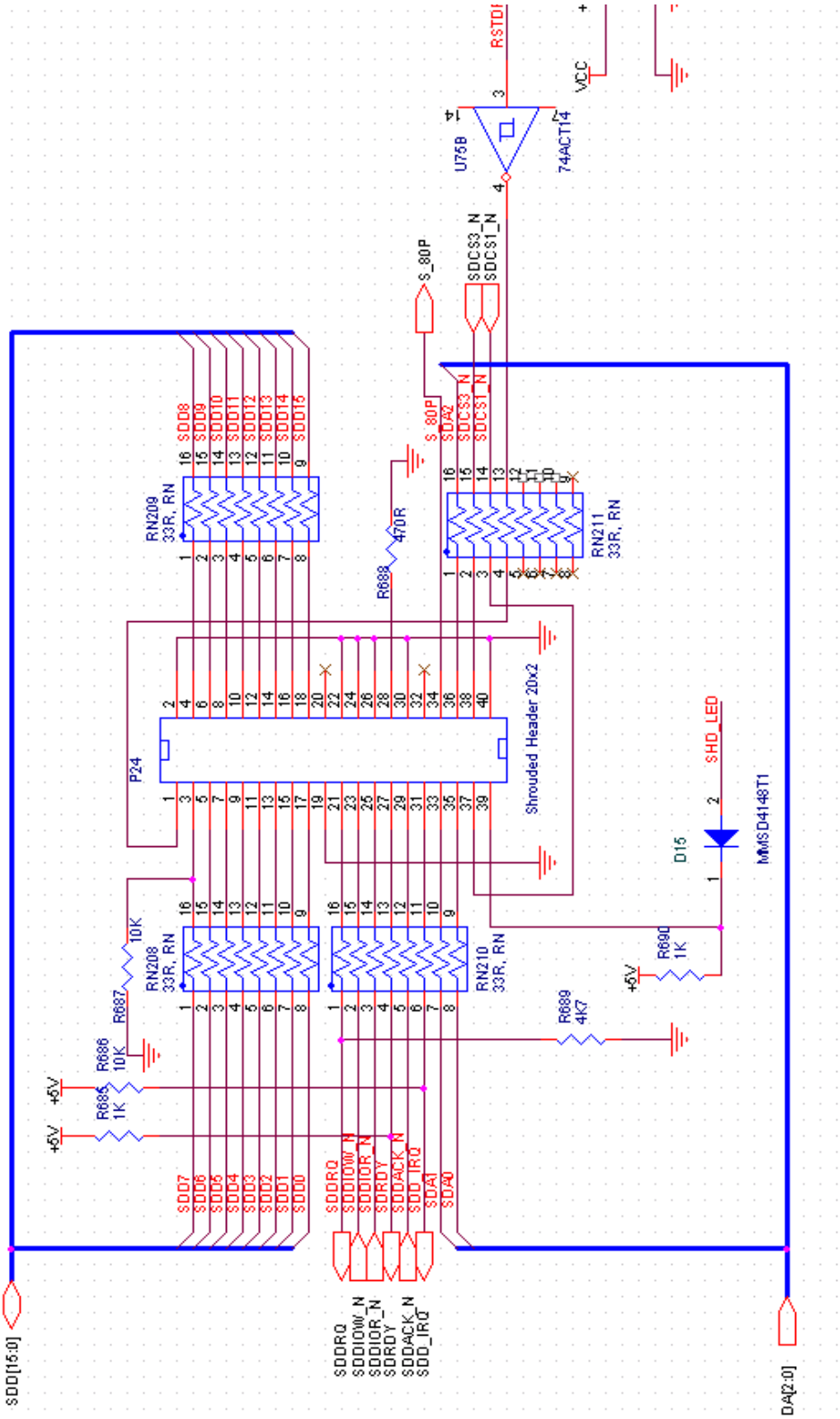


Figure 11-2. Secondary IDE Interface - Schematics

11.2.1 Compact Flash Support

11.2.1.1 Overview

A CompactFlash card is essentially a small form factor card version of PCMCIA PC Card ATA (AT Attachment) specification and includes a True IDE (Integrated Drive Electronics) mode which is compatible with the ATA/ATAPI-4 specification. As such, there are 3 distinct interface modes that a CompactFlash card can use:

- PC Card Memory Mode (uses WE#, OE# to access memory locations)
- PC Card I/O Mode (uses IOWR#, IORD# to access I/O locations)
- True IDE Mode (uses IOWR#, IORD# to access I/O locations)

11.2.1.2 Implementation on Torridon

The CompactFlash card is essentially a solid state ATA disk drive. On Torridon, the CompactFlash is configured in True IDE mode. True IDE mode is selected by the OE* signal (also known as the ATA_SEL* pin) which is grounded during the assertion of reset.

Note: In True IDE mode, removal and hot insertion (i.e. insertion and removal of the card while the system is powered on) is not supported.

CompactFlash on Torridon is supported via a 3rd party adapter board which connects into one of the IDE headers on the board. These boards provide a standard IDE interface. See Table 11-1and Figure 11-3below.

Table 11-1. CompactFlash Interconnect

Signal	Pin#	Description
A[2:0]	18,19,20	Address Pins. Used to select one of eight registers in the task file.
A[10:3]	8,10,11,12, 14,15,16,17	Address Pins. Not Used; connected to ground.
D[15:0]	31,30,29,28, 27,49,48,47, 6,5,4,3,2,23, 22,21	Data Pins. 0 is LSB, 15 is MSB. In True IDE mode, all task file operations are in byte mode on the low order bus and all the data transfers use the 16 bit bus.
CS_N[1:0]	32,7	Chip Selects. Used to select either the task file registers or Alternate Status Register and Device Control Register.
ATA_SEL*	9	Enables True IDE Mode. Tied to ground.
IORD*	34	IO Read Strobe. Indicates when the CompactFlash Card should drive its data on the bus.
IOWD*	35	IO Write Strobe. Indicates valid data is on the bus.

Table 11-1. CompactFlash Interconnect (continued)

Signal	Pin#	Description
CSEL*	39	Used to configure the CompactFlash card as a master or a slave. Tied to ground to configure card as a master.
RESET*	41	Reset the Compact Flash.
INTRQ	37	Interrupt request to controller.
IORDY*	42	IO Ready.
PDIAG*	46	Passed Diagnostic. Not connected. (No slave device connected)
DASP*	45	Drive Active/Slave Present. Led indicates activity
CD[2:1]*	25,26	Card Detect. Not connected. (Hot Insertion not supported)
IOIS16*	24	16 Bit Access. Not connected. (16 bit transfer assumed)
VS[2:1]*	40,33	Voltage Sense. Not Connected.
INPACK*	43	Input Acknowledge. Not used in True IDE mode; connected to +3.3V
REG	44	Register Select. Not used in True IDE mode; connected to +3.3V
WE*	36	Write Enable. Not used in True IDE mode; connected to +3.3V
VCC	13,38	+3.3Volts
GND	1,50	0 Volts.

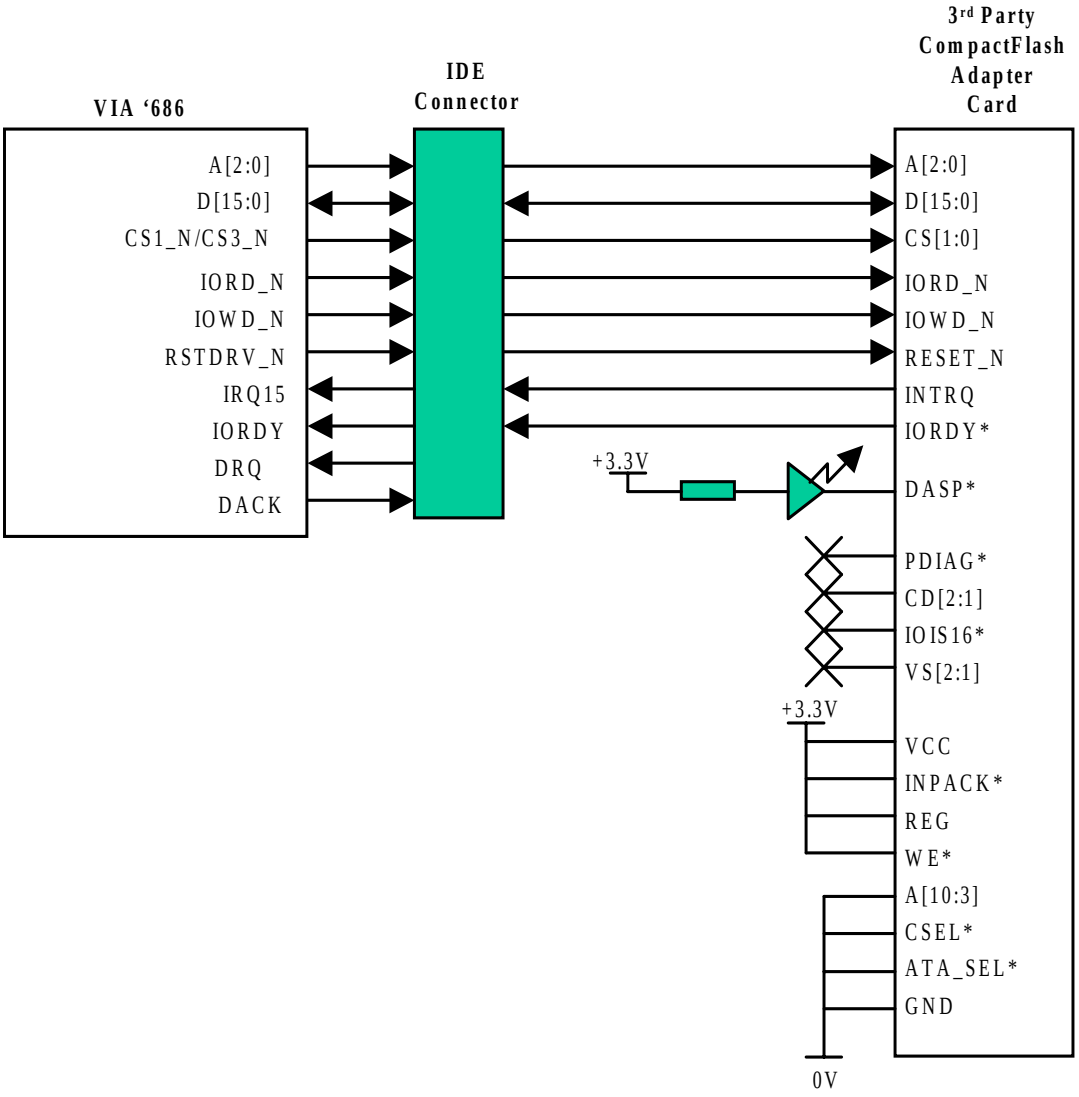


Figure 11-3. CompactFlash Connection

11.3 USB

The Via chip provides two USB interfaces. A 10 pin header, HD27, allows connectivity to a standard USB connector. The schematics are shown in Figure 11-4.

The following should be noted

- The USB interface is clocked from a separate 48MHz clock source
- Fuses (F1, F2) protect against incorrect connectivity. In the event of a USB cable being connected incorrectly, theses fuses will protect the power supply on the board. Incorrect connectivity may lead to the fuse being blown. In this event, the fuse would need to be replaced.

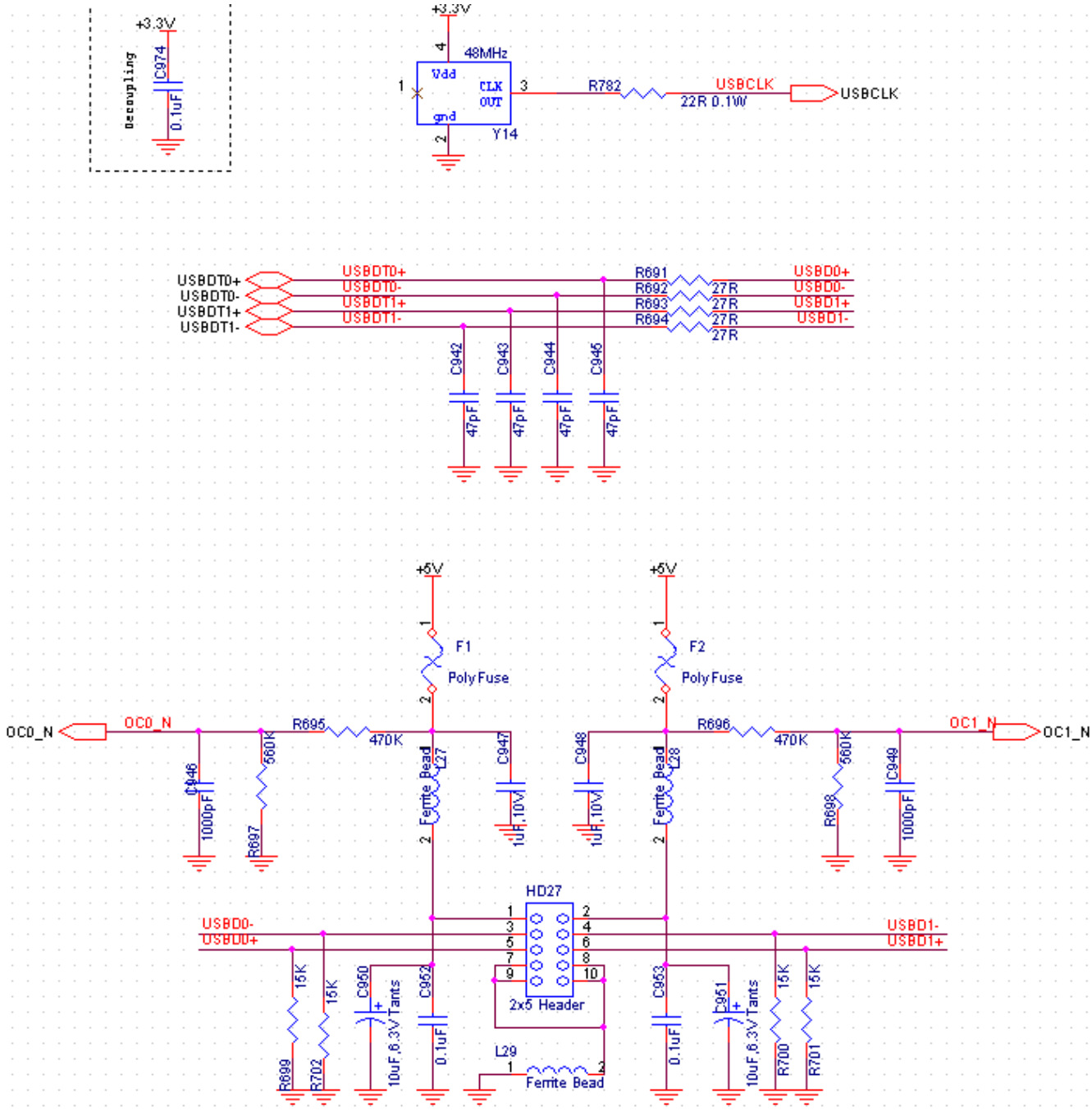


Figure 11-4. USB - Schematics

11.4 PS2

The ability to use a PS2 keyboard and mouse is also provided by the Via chip. A stacked 6 pin DIN, P35, provides the interface. The schematics are shown in Figure 11-5.

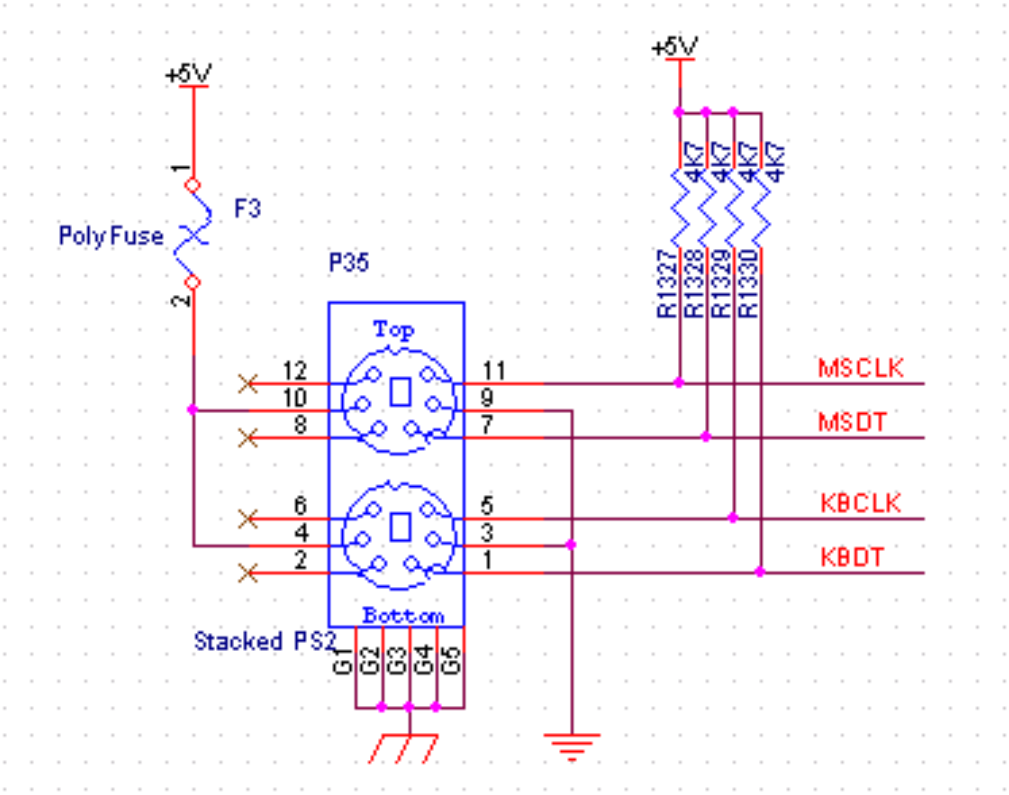


Figure 11-5. PS2 - Schematics

The following should be noted.

- A fuse (F3) protects the 5 Volt supply
- Pull-ups are added to all the data/clock signals.

Chapter 12 Communications

This section describes the Communications sub-section on the Torridon Motherboard.

12.1 Overview

12.2 Test

In addition to the five GBit Ethernet ports, Torridon provides connectivity to the outside world via

1. Two 128 pin connectors. These “QUADS” compatible connectors are pin compatible with the family of ADS boards from Motorola.
2. A UTOPIA Interface

12.3 QUADS Compatible Headers

The QUADS compatible connectors are implemented using two 128 pin headers. These provide connection to the processor’s CPM and host bus. On Torridon, these connectors are controlled by Work Processor 1. These would allow the connection of an add on card which would typically provide additional PHYs.

For example, the TCOM card shown in Figure 12-1 provides the PHYS necessary to connect to an E1/T1 interface.

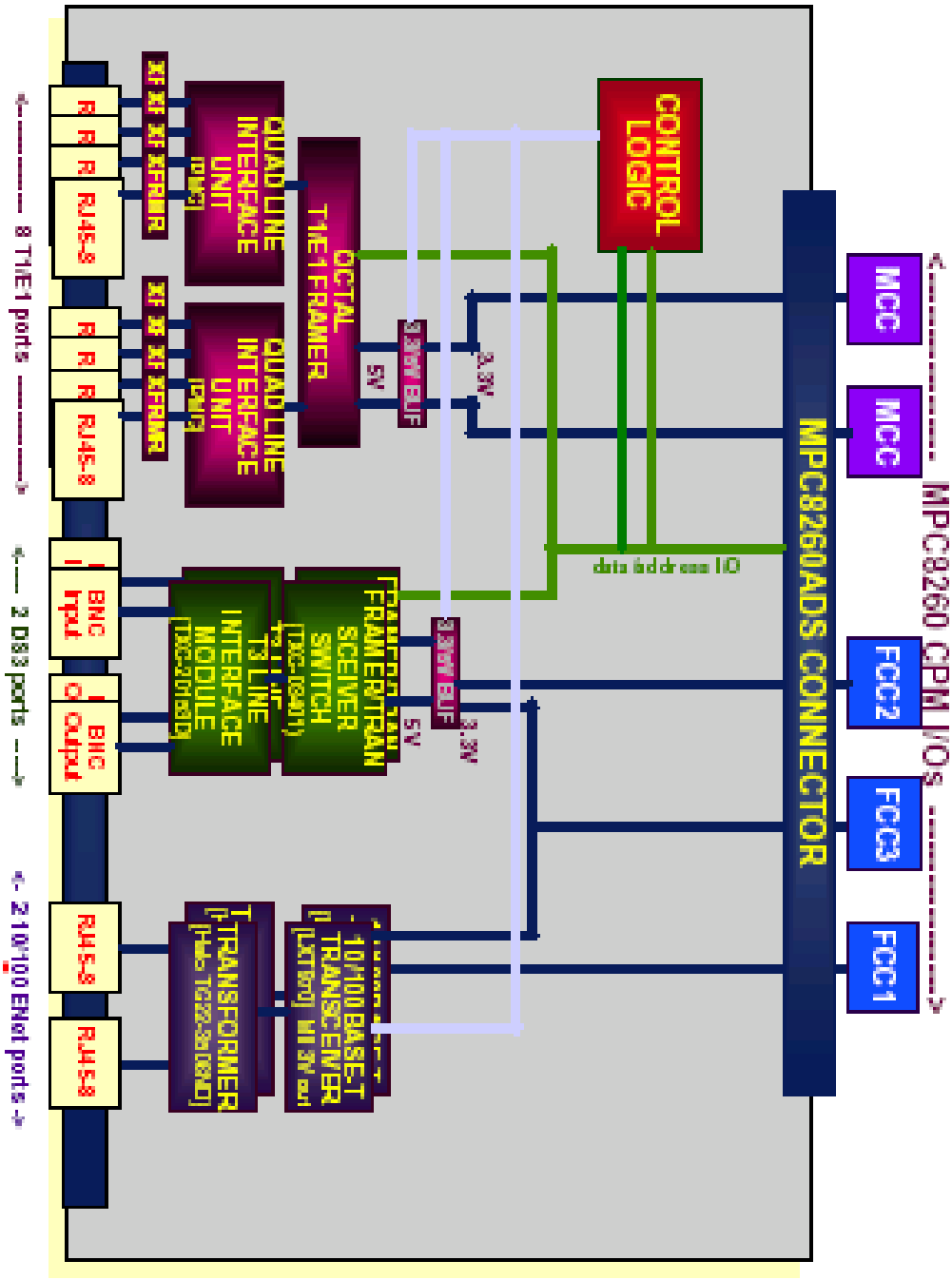


Figure 12-1. E1/T1 Card

As shown in Figure 12-2, two headers are provided for connectivity. As shown in Figure 12-3, one of these provides access to the CPM; the other to a de-multiplexed version of the host bus.

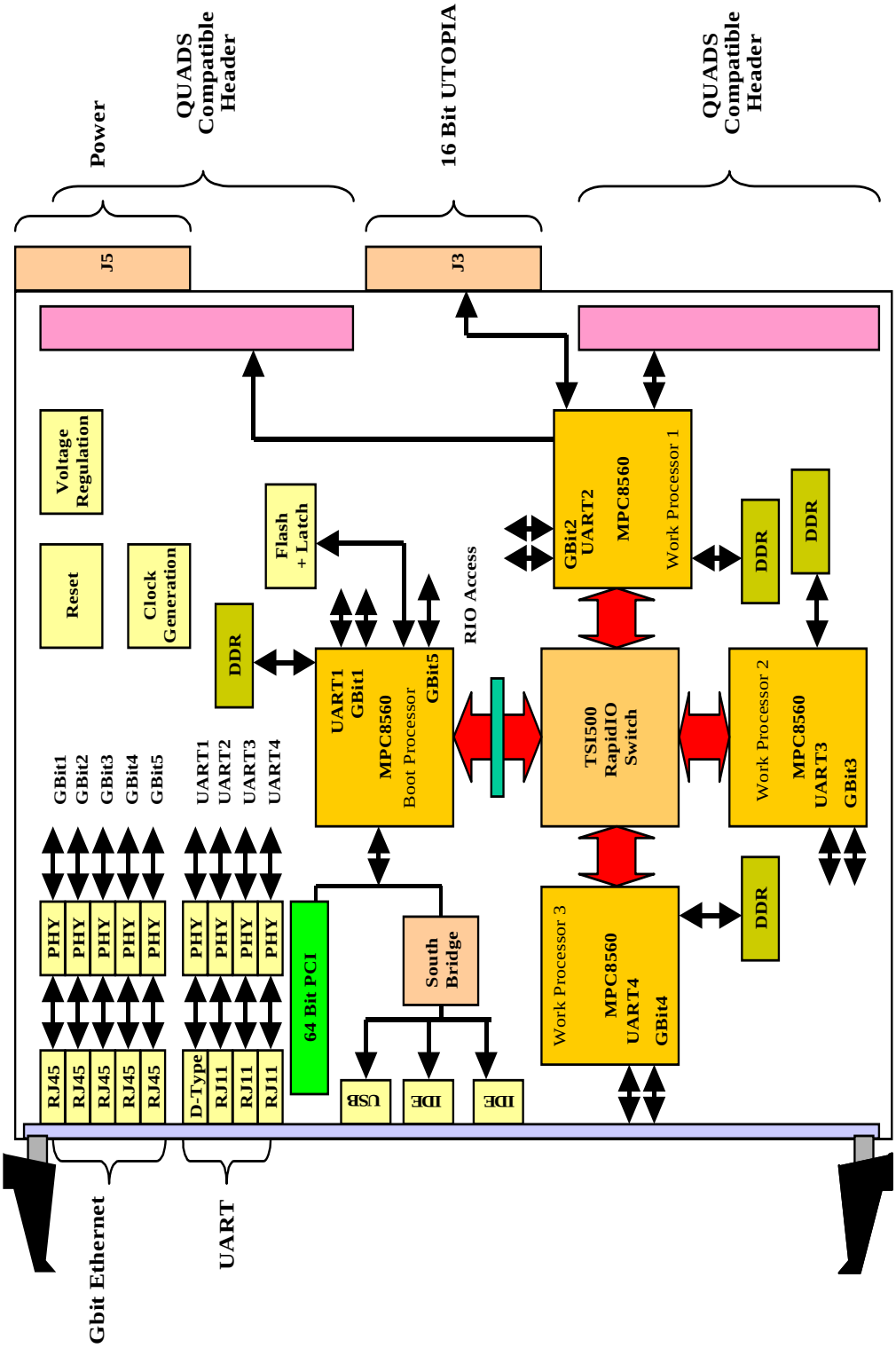


Figure 12-2. QUADS Compatible Headers

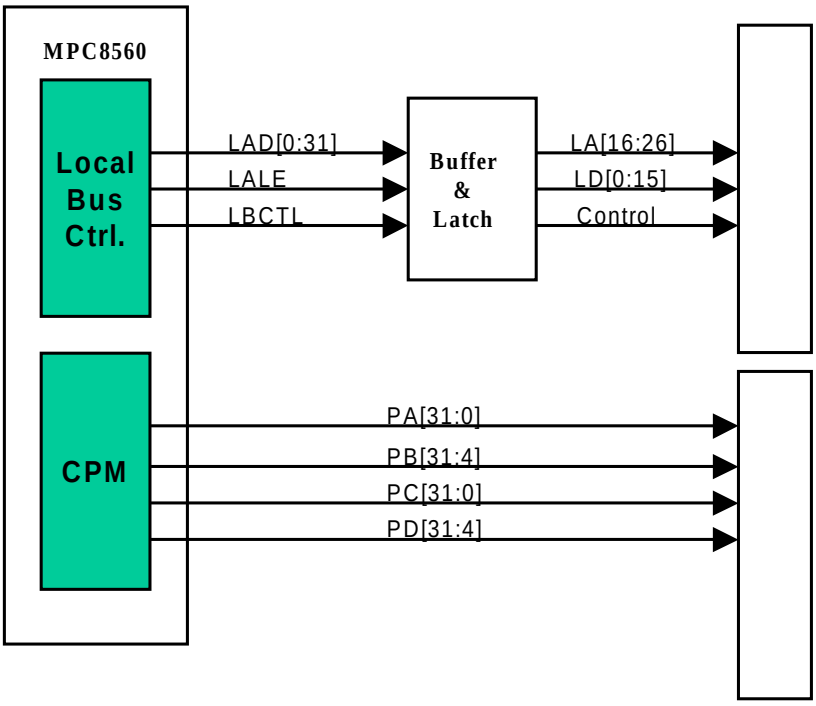


Figure 12-3. Connectivity to the QUADS Headers

The following tables (Table 12-1, Table 12-2, Table 12-3, Table 12-4, Table 12-5, Table 12-6, Table 12-7, and Table 12-8) detail the pinout required to allow QUADS compatible expansion cards to be used.

Table 12-1. ADS Compatible Expansion Connector - P28 - Row A

CONNECTOR PIN#	SIGNAL	DESCRIPTION
A1	LA16	Local Address Bus [16]
A2	LA17	Local Address Bus [17]
A3	LA18	Local Address Bus [18]
A4	LA19	Local Address Bus [19]
A5	LA20	Local Address Bus [20]
A6	LA21	Local Address Bus [12]
A7	LA22	Local Address Bus [22]
A8	LA23	Local Address Bus [23]
A9	LA24	Local Address Bus [24]
A10	LA25	Local Address Bus [25]
A11	LA26	Local Address Bus [26]
A12	BLA27	Burst Local Address Bus [27]
A13	BLA28	Burst Local Address Bus [28]
A14	BLA29	Burst Local Address Bus [29]
A15	BLA30	Burst Local Address Bus [30]
A16	BLA31	Burst Local Address Bus [31]
A17	+12V	+ 12 Volts
A18	+12V	+ 12 Volts
A19	NC	Not Connected
A20	+3.3V	+ 3.3 Volts
A21	+3.3V	+ 3.3 Volts
A22	+3.3V	+ 3.3 Volts
A23	+3.3V	+ 3.3 Volts
A24	+3.3V	+ 3.3 Volts
A25	NC	Not Connected
A26	+5V	+ 5 Volts
A27	+5V	+ 5 Volts
A28	+5V	+ 5 Volts
A29	+5V	+ 5 Volts
A30	+5V	+ 5 Volts
A31	+5V	+ 5 Volts
A32	+5V	+ 5 Volts

Table 12-2. ADS Compatible Expansion Connector - P28 - Row B

CONNECTOR PIN#	SIGNAL	DESCRIPTION
B1	0V	0 Volts
B2	0V	0 Volts
B3	0V	0 Volts
B4	NC	Not Connected
B5	NC	Not Connected
B6	NC	Not Connected
B7	NC	Not Connected
B8	NC	Not Connected
B9	NC	Not Connected
B10	NC	Not Connected
B11	NC	Not Connected
B12	NC	Not Connected
B13	NC	Not Connected
B14	NC	Not Connected
B15	NC	Not Connected
B16	0V	0 Volts
B17	0V	0 Volts
B18	NC	Not Connected
B19	NC	Not Connected
B20	NC	Not Connected
B21	+3.3V	+ 3.3 Volts
B22	+3.3V	+ 3.3 Volts
B23	+3.3V	+ 3.3 Volts
B24	+3.3V	+ 3.3 Volts
B25	NC	Not Connected
B26	+5V	+ 5 Volts
B27	+5V	+ 5 Volts
B28	+5V	+ 5 Volts
B29	+5V	+ 5 Volts
B30	+5V	+ 5 Volts
B31	+5V	+ 5 Volts
B32	+5V	+ 5 Volts

Table 12-3. ADS Compatible Expansion Connector - P28 - Row C

CONNECTOR PIN#	SIGNAL	DESCRIPTION
C1	0V	0 Volts
C2	BCLK2	Buffered Clock 2
C3	0V	0 Volts
C4	BLCS_N6	Buffered Local Chip Select 6
C5	BLCS_N7	Buffered Local Chip Select 7
C6	0V	0 Volts
C7	NC	Not Connected
C8	NC	Not Connected
C9	NC	Not Connected
C10	HRESET	Hard Reset
C11	IRQ6*	Interrupt 6
C12	IRQ7*	INterrupt 7
C13	0V	0 Volts
C14	LD0	Local Data Bus [0]
C15	LD1	Local Data Bus [1]
C16	LD2	Local Data Bus [2]
C17	LD3	Local Data Bus [3]
C18	LD4	Local Data Bus [4]
C19	LD5	Local Data Bus [5]
C20	LD6	Local Data Bus [6]
C21	LD7	Local Data Bus [7]
C22	LD8	Local Data Bus [8]
C23	LD9	Local Data Bus [9]
C24	LD10	Local Data Bus [10]
C25	LD11	Local Data Bus [11]
C26	LD12	Local Data Bus [12]
C27	LD13	Local Data Bus [13]
C28	LD14	Local Data Bus [14]
C29	LD15	Local Data Bus [15]
C30	NC	Not Connected
C31	NC	Not Connected
C32	NC	Not Connected

Table 12-4. ADS Compatible Expansion Connector - P28 - Row B

CONNECTOR PIN#	SIGNAL	DESCRIPTION
D1	0V	0 Volts
D2	0V	0 Volts
D3	0V	0 Volts
D4	BLWE_N0	Buffered Local Write Enable 0
D5	BLWE_N0	Buffered Local Write Enable 0
D6	0V	0 Volts
D7	BLGPL0	Buffered Local General Purpose Line 0
D8	BLGPL1	Buffered Local General Purpose Line 1
D9	BLGPL2	Buffered Local General Purpose Line 2
D10	BLGPL3	Buffered Local General Purpose Line 3
D11	BLGPL4	Buffered Local General Purpose Line 4
D12	BLGPL5	Buffered Local General Purpose Line 5
D13	0V	0 Volts
D14	BALE	Buffered Address Latch Enable
D15	BLBCTL	Buffered Local Bus Control
D16	0V	0 Volts
D17	0V	0 Volts
D18	0V	0 Volts
D19	0V	0 Volts
D20	0V	0 Volts
D21	0V	0 Volts
D22	0V	0 Volts
D23	0V	0 Volts
D24	0V	0 Volts
D25	0V	0 Volts
D26	0V	0 Volts
D27	0V	0 Volts
D28	0V	0 Volts
D29	0V	0 Volts
D30	0V	0 Volts
D31	0V	0 Volts
D32	0V	0 Volts

Table 12-5. ADS Compatible Expansion Connector - P29 - Row A

CONNECTOR PIN#	SIGNAL	DESCRIPTION
A1	PD[31]	Port D [31]
A2	PD[30]	Port D [30]
A3	PD[29]	Port D [29]
A4	PD[28]	Port D [28]
A5	PD[27]	Port D [27]
A6	PD[26]	Port D [26]
A7	PD[25]	Port D [25]
A8	PD[24]	Port D [24]
A9	PD[23]	Port D [23]
A10	PD[22]	Port D [22]
A11	PD[21]	Port D [21]
A12	PD[20]	Port D [20]
A13	PD[19]	Port D [19]
A14	PD[18]	Port D [18]
A15	PD[17]	Port D [17]
A16	PD[16]	Port D [16]
A17	PD[15]	Port D [15]
A18	PD[14]	Port D [14]
A19	PD[13]	Port D [13]
A20	PD[12]	Port D [12]
A21	PD[11]	Port D [11]
A22	PD[10]	Port D [10]
A23	PD[9]	Port D [9]
A24	PD[8]	Port D [8]
A25	PD[7]	Port D [7]
A26	PD[6]	Port D [6]
A27	PD[5]	Port D [5]
A28	PD[4]	Port D [4]
A29	+5V	+ 5 Volts
A30	+5V	+ 5 Volts
A31	+5V	+ 5 Volts
A32	+5V	+ 5 Volts

Table 12-6. ADS Compatible Expansion Connector - P29 - Row B

CONNECTOR PIN#	SIGNAL	DESCRIPTION
B1	PA[31]	Port A [31]
B2	PA[30]	Port A [30]
B3	PA[29]	Port A [29]
B4	PA[28]	Port A [28]
B5	PA[27]	Port A [27]
B6	PA[26]	Port A [26]
B7	PA[25]	Port A [25]
B8	PA[24]	Port A [24]
B9	PA[23]	Port A [23]
B10	PA[22]	Port A [22]
B11	PA[21]	Port A [21]
B12	PA[20]	Port A [20]
B13	PA[19]	Port A [19]
B14	PA[18]	Port A [18]
B15	PA[17]	Port A [17]
B16	PA[16]	Port A [16]
B17	PA[15]	Port A [15]
B18	PA[14]	Port A [14]
B19	PA[13]	Port A [13]
B20	PA[12]	Port A [12]
B21	PA[11]	Port A [11]
B22	PA[10]	Port A [10]
B23	PA[9]	Port A [9]
B24	PA[8]	Port A [8]
B25	PA[7]	Port A [7]
B26	PA[6]	Port A [6]
B27	PA[5]	Port A [5]
B28	PA[4]	Port A [4]
B29	PA[3]	Port A [3]
B30	PA[2]	Port A [2]
B31	PA[1]	Port A [1]
B32	PA[0]	Port A [0]

Table 12-7. ADS Compatible Expansion Connector - P29 - Row C

CONNECTOR PIN#	SIGNAL	DESCRIPTION
C1	PB[31]	Port B [31]
C2	PB[30]	Port B [30]
C3	PB[29]	Port B [29]
C4	PB[28]	Port B [28]
C5	PB[27]	Port B [27]
C6	PB[26]	Port B [26]
C7	PB[25]	Port B [25]
C8	PB[24]	Port B [24]
C9	PB[23]	Port B [23]
C10	PB[22]	Port B [22]
C11	PB[21]	Port B [21]
C12	PB[20]	Port B [20]
C13	PB[19]	Port B [19]
C14	PB[18]	Port B [18]
C15	PB[17]	Port B [17]
C16	PB[16]	Port B [16]
C17	PB[15]	Port B [15]
C18	PB[14]	Port B [14]
C19	PB[13]	Port B [13]
C20	PB[12]	Port B [12]
C21	PB[11]	Port B [11]
C22	PB[10]	Port B [10]
C23	PB[9]	Port B [9]
C24	PB[8]	Port B [8]
C25	PB[7]	Port B [7]
C26	PB[6]	Port B [6]
C27	PB[5]	Port B [5]
C28	PB[4]	Port B [4]
C29	NC	Not Connected
C30	0V	0 Volts
C31	0V	0 Volts
C32	0V	0 Volts

Table 12-8. ADS Compatible Expansion Connector - P29 - Row D

CONNECTOR PIN#	SIGNAL	DESCRIPTION
D1	PC[31]	Port C [31]
D2	PC[30]	Port C [30]
D3	PC[29]	Port C [29]
D4	PC[28]	Port C [28]
D5	PC[27]	Port C [27]
D6	PC[26]	Port C [26]
D7	PC[25]	Port C [25]
D8	PC[24]	Port C [24]
D9	PC[23]	Port C [23]
D10	PC[22]	Port C [22]
D11	PC[21]	Port C [21]
D12	PC[20]	Port C [20]
D13	PC[19]	Port C [19]
D14	PC[18]	Port C [18]
D15	PC[17]	Port C [17]
D16	PC[16]	Port C [16]
D17	PC[15]	Port C [15]
D18	PC[14]	Port C [14]
D19	PC[13]	Port C [13]
D20	PC[12]	Port C [12]
D21	PC[11]	Port C [11]
D22	PC[10]	Port C [10]
D23	PC[9]	Port C [9]
D24	PC[8]	Port C [8]
D25	PC[7]	Port C [7]
D26	PC[6]	Port C [6]
D27	PC[5]	Port C [5]
D28	PC[4]	Port C [4]
D29	PC[3]	Port C [3]
D30	PC[2]	Port C [2]
D31	PC[1]	Port C [1]
D32	PC[0]	Port C [0]

12.4 UTOPIA Interface

Some of the CPM pins from Work Processor 1are pinned out to a 105 pin connector to provide access to a 16 bit UTOPIA interface. This header is compatible with the Compact PCI specification. This interface is purely digital, Torridon does not support any UTOPIA PHYs. The pinout of this connector is shown in the following tables (Table 12-9, Table 12-10, Table 12-11, Table 12-12, Table 12-13, and Table 12-14.

Table 12-9. 16 Bit UTOPIA Connector - P7 - Row A

CONNECTOR PIN#	SIGNAL	DESCRIPTION
A1	+3.3V	+ 3.3 Volts
A2	0V	0 Volts
A3	0V	0 Volts
A4	TXADD4	Transmit Address [4]
A5	TXADD2	Transmit Address [2]
A6	TXADD0	Transmit Address [0]
A7	TXCLAV	Transmit Cell Available
A8	TXSOC	Transmit Start of Cell
A9	TXADD14	Transmit Address [14]
A10	TXADD12	Transmit Address [12]
A11	TXADD10	Transmit Address [10]
A12	TXADD8	Transmit Address [8]
A13	0V	0 Volts
A14	TXADD6	Transmit Address [6]
A15	TXADD4	Transmit Address [4]
A16	TXADD2	Transmit Address [2]
A17	TXADD0	Transmit Address [0]
A18	0V	0 Volts
A19	+3.3V	+ 3.3 Volts

Table 12-10. 16 Bit UTOPIA Connector - P7 - Row B

CONNECTOR PIN#	SIGNAL	DESCRIPTION
B1	0V	0 Volts
B2	+3.3V	+ 3.3 Volts
B3	0V	0 Volts
B4	TXADD3	Transmit Address [3]
B5	TXADD1	Transmit Address [1]
B6	TXPRTY	Transmit Data Parity
B7	TXENB	Transmit Enable
B8	TXD15	Transmit Data [15]
B9	TXD13	Transmit Data [13]
B10	TXD11	Transmit Data [11]
B11	TXD9	Transmit Data [9]
B12	TCLK	Transmit Clock
B13	TXD7	Transmit Data [7]
B14	TXD5	Transmit Data [5]
B15	TXD3	Transmit Data [3]
B16	TXD1	Transmit Data [1]
B17	0V	0 Volts
B18	+3.3V	+ 3.3 Volts
B19	0V	0 Volts

Table 12-11. 16 Bit UTOPIA Connector - P7 - Row C

CONNECTOR PIN#	SIGNAL	DESCRIPTION
C1	0V	0 Volts
C2	0V	0 Volts
C3	0V	0 Volts
C4	0V	0 Volts
C5	0V	0 Volts
C6	0V	0 Volts
C7	0V	0 Volts
C8	0V	0 Volts
C9	0V	0 Volts
C10	0V	0 Volts

Table 12-11. 16 Bit UTOPIA Connector - P7 - Row C (continued)

CONNECTOR PIN#	SIGNAL	DESCRIPTION
C11	0V	0 Volts
C12	0V	0 Volts
C13	0V	0 Volts
C14	0V	0 Volts
C15	0V	0 Volts
C16	0V	0 Volts
C17	0V	0 Volts
C18	0V	0 Volts
C19	0V	0 Volts

Table 12-12. 16 Bit UTOPIA Connector - P7- Row D

CONNECTOR PIN#	SIGNAL	DESCRIPTION
D1	0V	0 Volts
D2	+3.3V	+ 3.3 Volts
D3	0V	0 Volts
D4	RXADD3	Receive Address [3]
D5	RXADD1	Receive Address [1]
D6	RXPRTY	Receive Data Parity
D7	RXENB	Receive Enable
D8	RXD15	Receive Data [15]
D9	RXD13	Receive Data [13]
D10	RXD11	Receive Data [11]
D11	RXD9	Receive Data [9]
D12	RCLK	Receive Clock
D13	RXD7	Receive Data [7]
D14	RXD5	Receive Data [5]
D15	RXD3	Receive Data [3]
D16	RXD1	Receive Data [1]
D17	0V	0 Volts
D18	+3.3V	+ 3.3 Volts
D19	0V	0 Volts

Table 12-13. 16 Bit UTOPIA Connector - P7 - Row E

CONNECTOR PIN#	SIGNAL	DESCRIPTION
E1	+3.3V	+ 3.3 Volts
E2	0V	0 Volts
E3	0V	0 Volts
E4	RXADD4	Receive Address [4]
E5	RXADD2	Receive Address [2]
E6	RXADD0	Receive Address [0]
E7	RXCLAV	Receive Cell Available
E8	RXSOC	Receive Start of Cell
E9	RXADD14	Receive Address [14]
E10	RXADD12	Receive Address [12]
E11	RXADD10	Receive Address [10]
E12	RXADD8	Receive Address [8]
E13	0V	0 Volts
E14	RXADD6	Receive Address [6]
E15	RXADD4	Receive Address [4]
E16	RXADD2	Receive Address [2]
E17	RXADD0	Receive Address [0]
E18	0V	0 Volts
E19	+3.3V	+ 3.3 Volts

Table 12-14. 16 Bit UTOPIA Connector - P7 - Row F

CONNECTOR PIN#	SIGNAL	DESCRIPTION
F1	0V	0 Volts
F2	0V	0 Volts
F3	0V	0 Volts
F4	0V	0 Volts
F5	0V	0 Volts
F6	0V	0 Volts
F7	0V	0 Volts
F8	0V	0 Volts
F9	0V	0 Volts
F10	0V	0 Volts

Chapter 13 Reset

This section describes the reset sub-section on the Torridon Motherboard.

13.1 Overview

All the reset signals on the motherboard are handled by a CPLD. The CPLD monitors the various reset sources and asserts the required outputs.

13.2 Reset Sources

There are four main sources of reset on the motherboard.

- Power On - After initial power on, the CPLD ensures all peripherals are brought out of reset in a controlled sequence
- Push Button - A board reset can be issued at any time by pressing the reset switch.
- COP Reset - A debugger, connected to the COP interface of any of the four processors, may cause a reset.
- Boot Processor - The boot processor is capable of resetting the other processors on the board

13.3 Reset Scheme

The diagram in Figure 13-1 shows the reset scheme utilised on Torridon. A CPLD responsible for controlling the resets on the board.

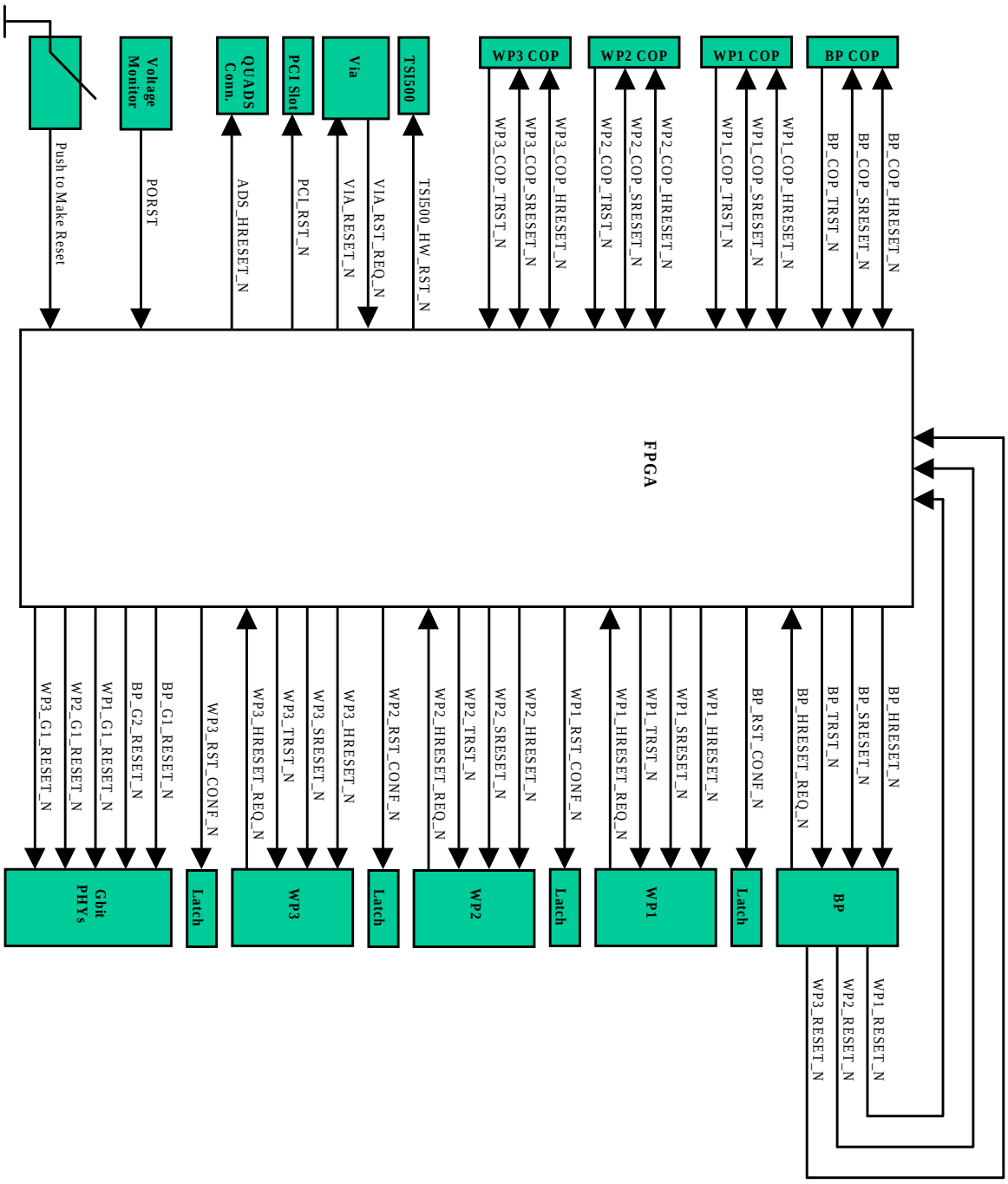


Figure 13-1. Reset Scheme

Table 13-1 details the reset signals used on Torridon.

Table 13-1. Reset Signals

Signal	Description	Asserted When?	I/O (w.r.t. CPLD)
PORST	Power on Reset	On system power up	Input
Push to Make Reset	Push to Make Reset	By user depressing switch	Input
BP_COP_HRESET_N	Boot Processor COP Hard Reset	By COP tools By processor following a system reset	Input/Output
BP_COP_SRESET_N	Boot Processor COP Soft Reset	By COP tools By processor following a system reset	Input/Output
BP_COP_TRST_N	Boot Processor COP Test Reset	By COP tools	Input
BP_HRESET_N	Boot Processor Hard Reset	By CPLD following system reset, COP hard reset or Boot Processor hard reset request	Output
BP_SRESET_N	Boot Processor Soft Reset	By CPLD following system reset, COP soft reset	Output
BP_TRST_N	Boot Processor Test Reset	By CPLD following COP test reset	Output
BP_HRESET_REQ_N	Boot Processor Hard Reset Request	By Boot Processor	Input
BP_RST_CONF_N	Boot Processor Reset Configuration	On power up or any hard reset. Used to latch configuration pins	Output
WP1_COP_HRESET_N	Work Processor 1 COP Hard Reset	By COP tools By processor following a system reset	Input/Output
WP1_COP_SRESET_N	Work Processor 1 COP Soft Reset	By COP tools By processor following a system reset	Input/Output
WP1_COP_TRST_N	Work Processor 1 COP Test Reset	By COP tools	Input
WP1_HRESET_N	Work Processor 1 Hard Reset	By CPLD following system reset, COP hard reset or Work Processor 1 hard reset request	Output
WP1_SRESET_N	Work Processor 1 Soft Reset	By CPLD following system reset, COP soft reset	Output
WP1_TRST_N	Work Processor 1 Test Reset	By CPLD following COP test reset	Output
WP1_HRESET_REQ_N	Work Processor 1 Hard Reset Request	By Work Processor 1	Input
WP1_RST_CONF_N	Work Processor 1 Reset Configuration	On power up or any hard reset. Used to latch configuration pins	Output
WP2_COP_HRESET_N	Work Processor 2 COP Hard Reset	By COP tools By processor following a system reset	Input/Output
WP2_COP_SRESET_N	Work Processor 2 COP Soft Reset	By COP tools By processor following a system reset	Input/Output
WP2_COP_TRST_N	Work Processor 2 COP Test Reset	By COP tools	Input
WP2_HRESET_N	Work Processor 2 Hard Reset	By CPLD following system reset, COP hard reset or Work Processor 2 hard reset request	Output

Table 13-1. Reset Signals (continued)

Signal	Description	Asserted When?	I/O (w.r.t. CPLD)
WP2_SRESET_N	Work Processor 2 Soft Reset	By CPLD following system reset, COP soft reset	Output
WP2_TRST_N	Work Processor 2 Test Reset	By CPLD following COP test reset	Output
WP2_HRESET_REQ_N	Work Processor 2 Hard Reset Request	By Work Processor 2	Input
WP2_RST_CONF_N	Work Processor 2 Reset Configuration	On power up or any hard reset. Used to latch configuration pins	Output
WP3_COP_HRESET_N	Work Processor 3 COP Hard Reset	By COP tools By processor following a system reset	Input/Output
WP3_COP_SRESET_N	Work Processor 3 COP Soft Reset	By COP tools By processor following a system reset	Input/Output
WP3_COP_TRST_N	Work Processor 3 COP Test Reset	By COP tools	Input
WP3_HRESET_N	Work Processor 3 Hard Reset	By CPLD following system reset, COP hard reset or Work Processor 3 hard reset request	Output
WP3_SRESET_N	Work Processor 3 Soft Reset	By CPLD following system reset, COP soft reset	Output
WP3_TRST_N	Work Processor 3 Test Reset	By CPLD following COP test reset	Output
WP3_HRESET_REQ_N	Work Processor 3 Hard Reset Request	By Work Processor 3	Input
WP3_RST_CONF_N	Work Processor 3 Reset Configuration	On power up or any hard reset. Used to latch configuration pins	Output
BP_G1_RESET_N	Boot Processor's TSEC PHY1 Reset	On power up or any hard reset. Used to reset PHY	Output
BP_G2_RESET_N	Boot Processor's TSEC PHY2 Reset	On power up or any hard reset. Used to reset PHY	Output
WP1_G1_RESET_N	Work Processor 1's TSEC PHY1 Reset	On power up or any hard reset. Used to reset PHY	Output
WP2_G1_RESET_N	Work Processor 2's TSEC PHY1 Reset	On power up or any hard reset. Used to reset PHY	Output
WP3_G1_RESET_N	Work Processor 3's TSEC PHY1 Reset	On power up or any hard reset. Used to reset PHY	Output
TSI500_HW_RST_N	TSI500 RapidIO Switch Reset	On power on or Boot Processor reset	Output
VIA_RESET_N	Via Southbridge Reset	On power on or Boot Processor reset	Output
VIA_RESET_REQ_N	Via Southbridge Reset Request	Via requires a reset. (Software controlled)	Input
PCI_RST_N	PCI Bus Reset	On power on or Boot Processor reset	Output
ADS_HRESET_N	Reset for QUADS Compatible Connections	On power on or Boot Processor reset	Output

The following diagram in Figure 13-2 shows how the resets are handled.

The majority of the reset signals are simply ANDed together. As they are all active low, this effectively act as an active low ORing function.

A delay is added to some of the signals (e.g. the reset of the PHYS) to ensure they power up in a specific order.

A delay is also added to the signals used to latch in the configuration pins. (e.g. BP_RST_CONF_N, WP1_RST_CONF_N etc.). The timing of this signal is critical. Refer to the MPC8560 User Manual for mode details.

Please note: This diagram illustrates the functionally of the CPLD, not the actual implementation.

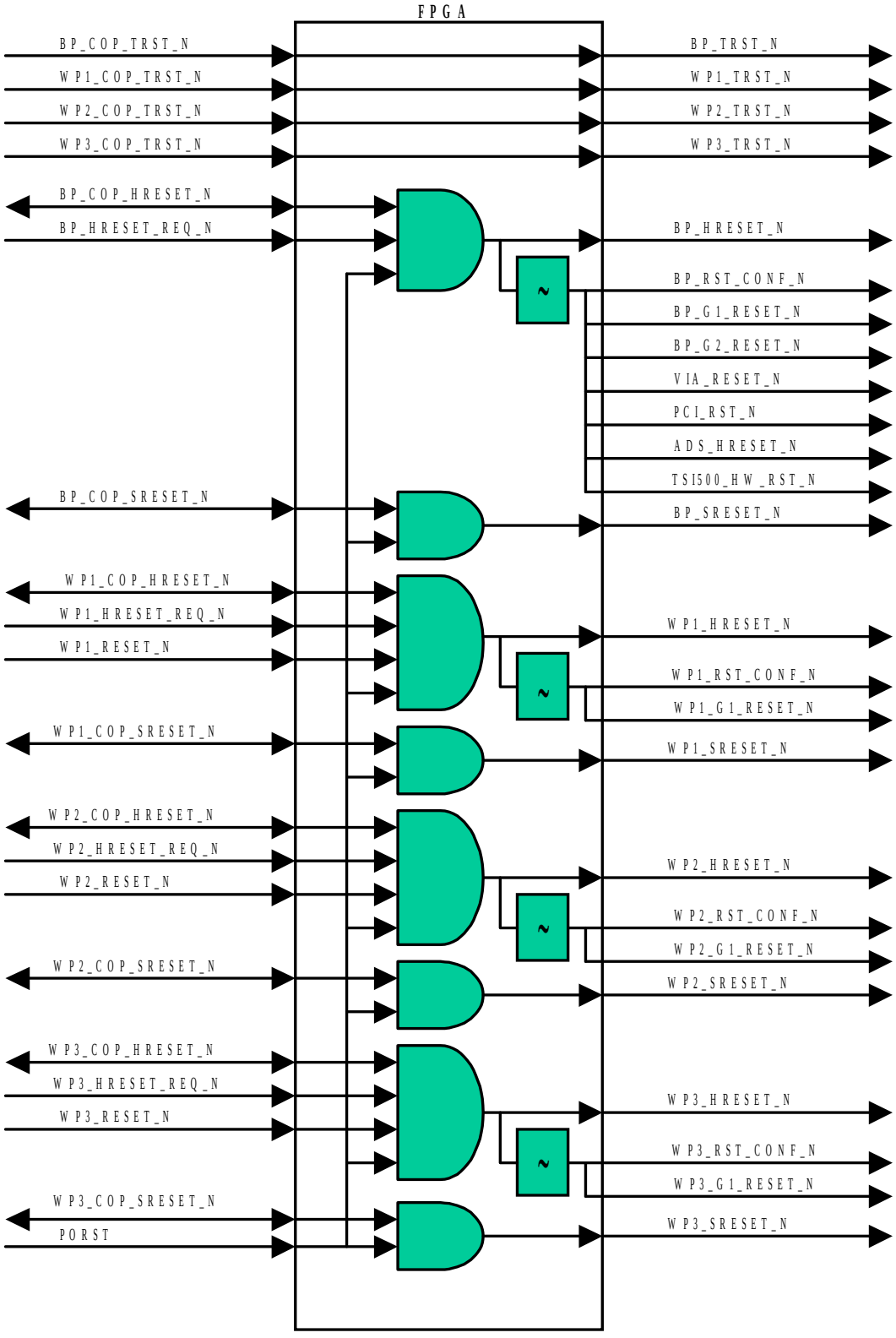


Figure 13-2. Resets

Chapter 14 Clocking

This section describes the Clocking sub-section on the Torridon Motherboard.

14.1 Overview

All of the clocks used on the Torridon system are generated locally, it does not rely on any external stimulus.

There are four distinct clocking environments on the board

- System Clocks
- RapidIO Clocks
- Processor Real Time Clock
- GBit Ethernet PHY Clocks
- Southbridge Real Time Clock

14.2 System Clocks

The system clock is provided by a 33.33MHz crystal oscillator. This clock is distributed, via a zero delay buffer, to produce the required system clocks. (i.e. processor, PCI, Southbridge and logic analyser.)

The diagram in Figure 14-1 shows the clocking mechanism.

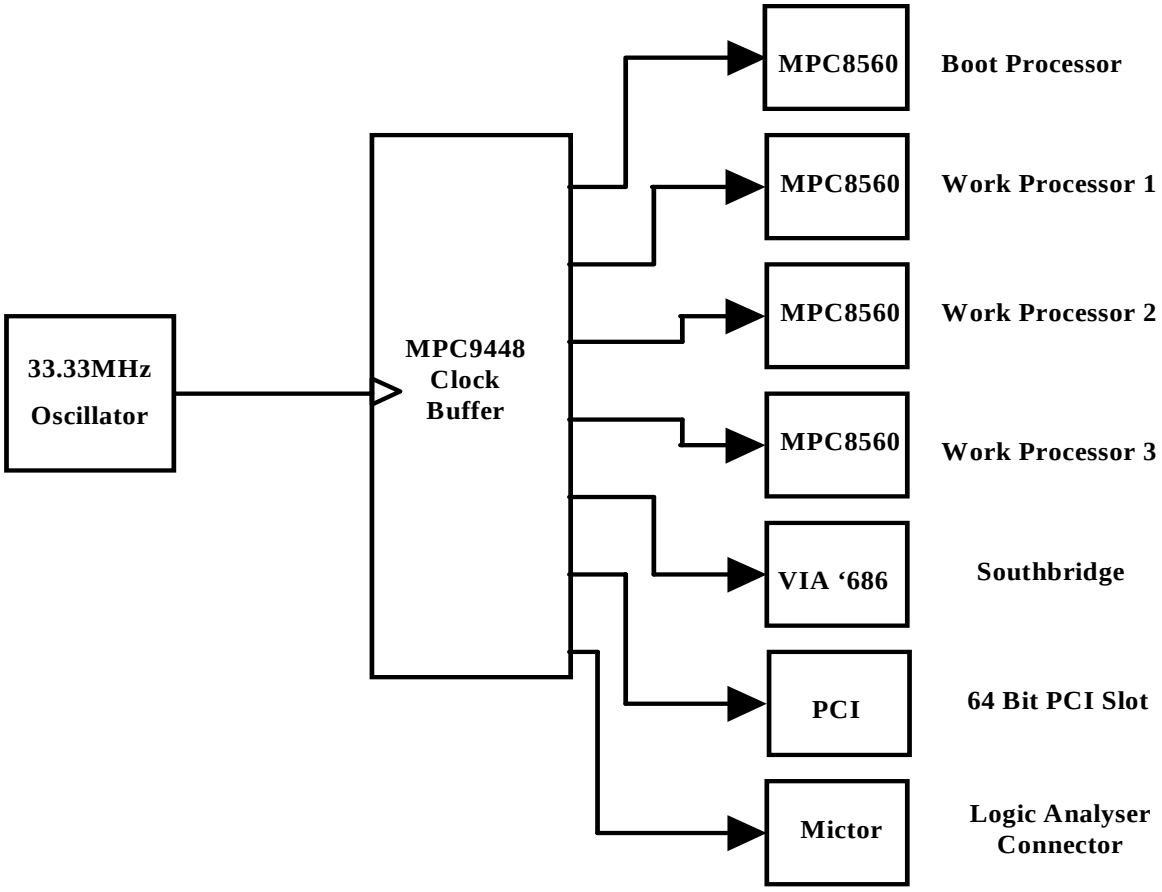


Figure 14-1. System Clocks

The diagram in Figure 14-2 shows the schematics for the system clock circuitry.

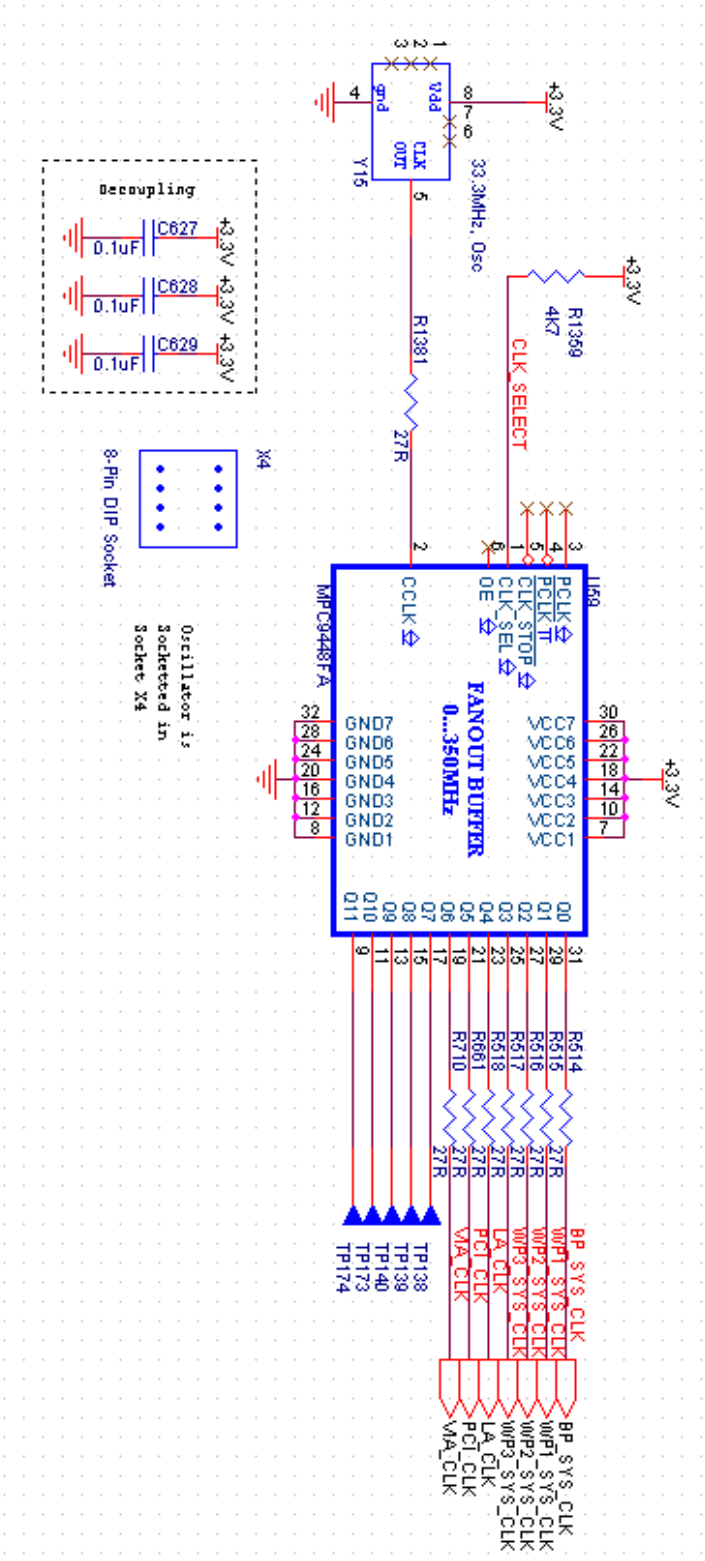


Figure 14-2. System Clocks - Schematics

The following should be noted about the circuitry.

- The oscillator is socketed to allow different frequencies to be used (if required)
- Series resistors (27 ohm) are inserted on all the clock lines to avoid any over/under shoot
- The CLK_SEL input on the MPC9448 fan out buffer is pulled high to select the TTL clock input. (as opposed to the differential input)
- Adequate de coupling is added to the 3.3V power rail

14.3 RapidIO Clocks

14.3.1 Overview

The RapidIO interface has independent receive and transmit clocks. These are referred to as inbound and outbound clocks.

A RapidIO endpoint receives the inbound clock as a LVDS pair from an adjacent RapidIO device through the RapidIO interface, then generates an internal clock using its own clock synchronizer.

The outbound (transmit) clock is generated from an internal PLL clock generator which provides the transmit clock by multiplexing the input clock (LVTTL).

The diagram in Figure 14-3 shows the RapidIO clocking scheme.

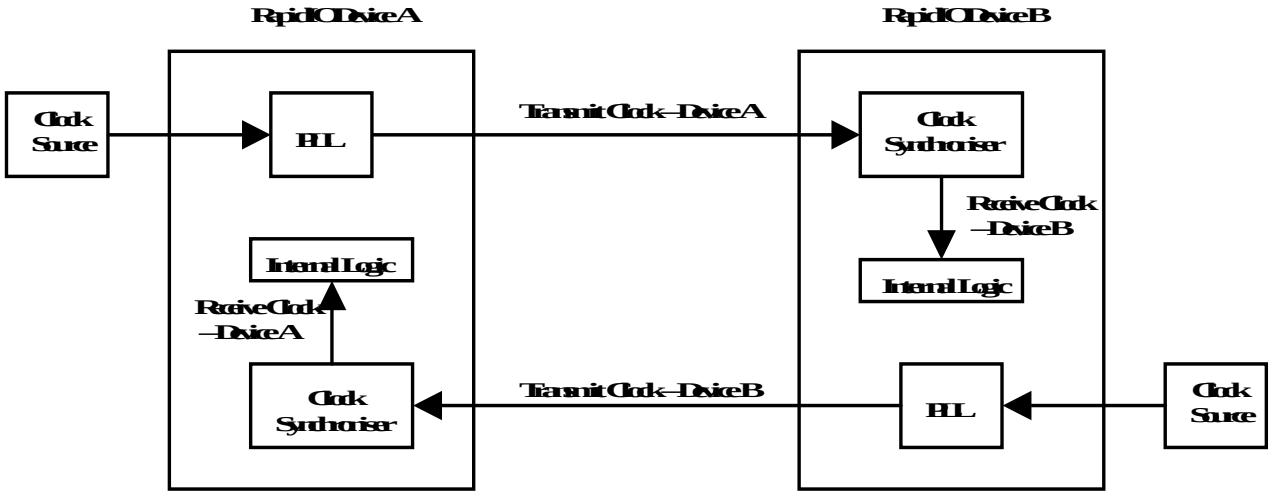


Figure 14-3. RapidIO Clocking

A RapidIO system can be designed to operate either asynchronously or synchronously to each RapidIO device. For asynchronous operation, each RapidIO device has its own separate outbound clock input. For synchronous operation, each RapidIO device shares a common clock source.

14.3.2 Torridon's RapidIO Sub-System

As shown in Figure 14-4, Torridon's RapidIO sub-system consists of four PowerQUICCIIIs connected to a four port RapidIO switch. All the connections to the respective ports are identical apart from the connection between the boot processor and Port 0 of the TSI500. Although this particular link also incorporates the connections to allow the bus to be probed by a logic analyser, this does not influence the clocking scheme.

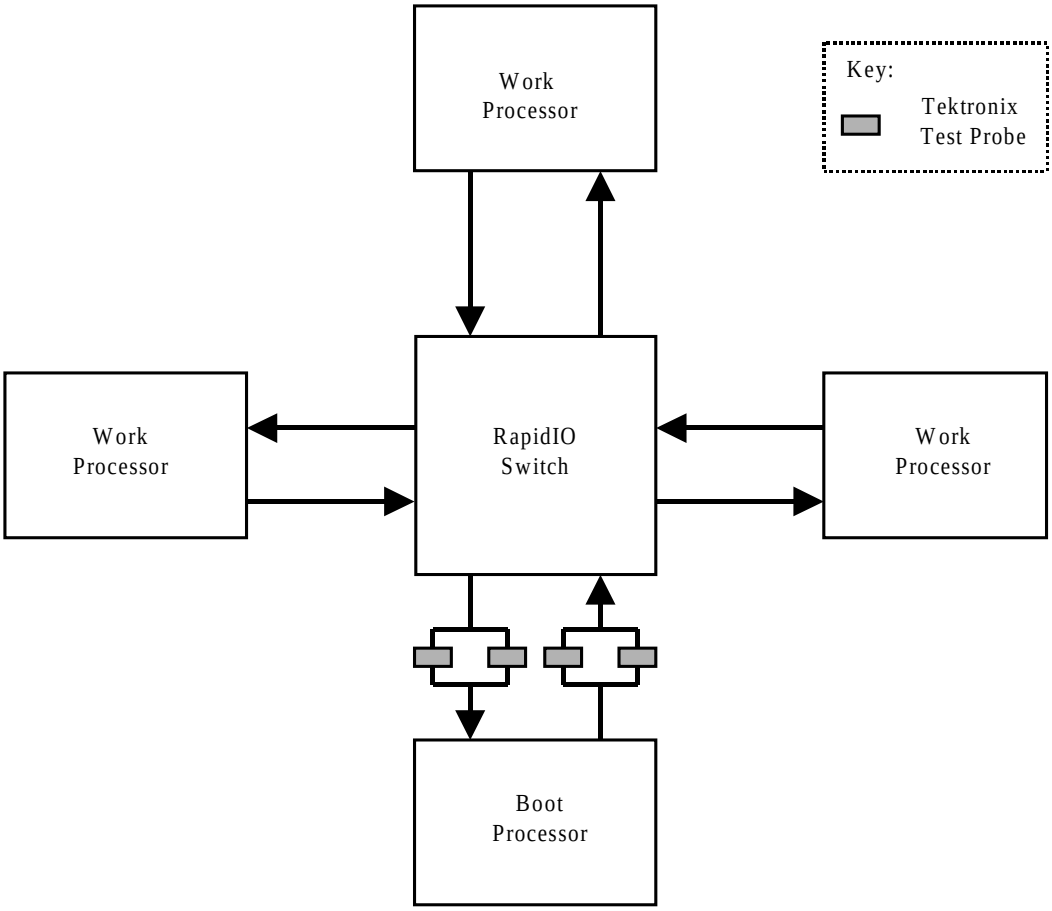


Figure 14-4. RapidIO Sub-System

14.3.3 Processor Clocks

The processor can generate the source of its RapidIO transmit clock from one of three separate sources. These sources are

- The RapidIO receive Clock
- The internal CCB clock
- The RapidIO_TX_CLK+/RapidIO_TX_CLK- inputs

The diagram in Figure 14-5 shows the different clock options available.

On Torridon, these options can be chosen using DIP switches, which set the appropriate configuration pins (LGPL0, LGPL1) on the PowerQUICCIII.

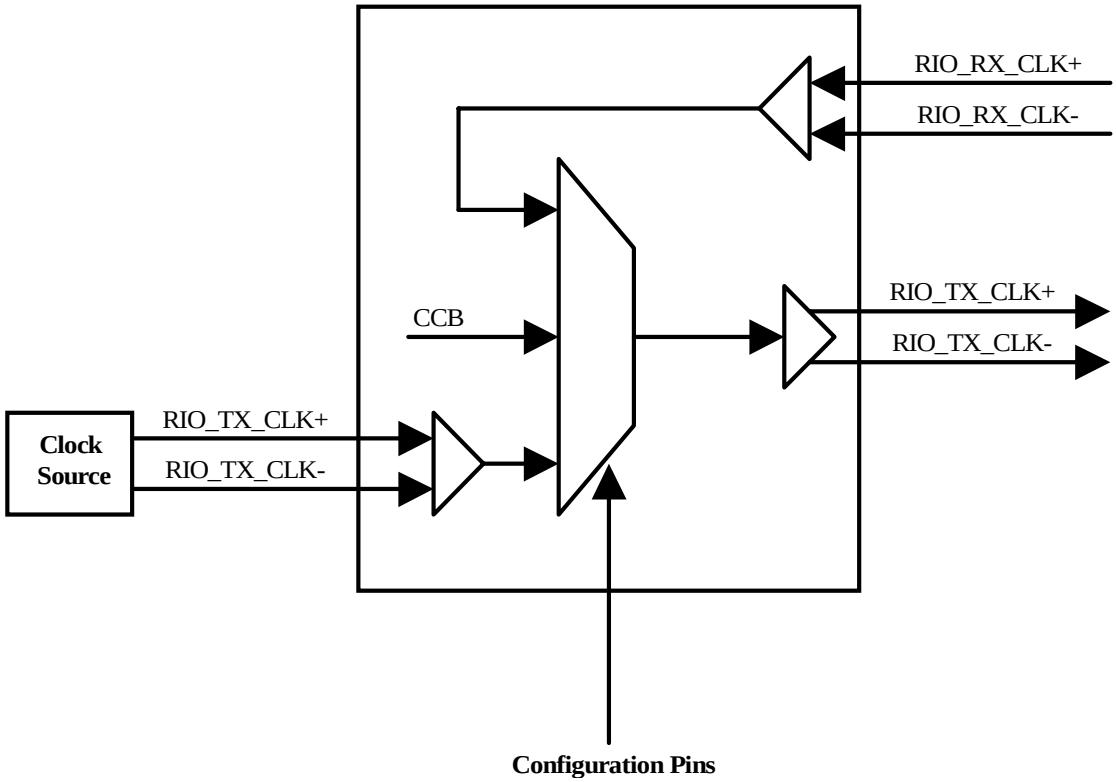


Figure 14-5. RapidIO Clock Options

14.3.4 TSI500 Clocks

The TSI500 switch may be clocked from one of two sources.

- A “slow speed” TTL clock
- A high speed differential clock

As with the processor, the selection of the clock source is made via configurations pins as shown in Figure 14-6.

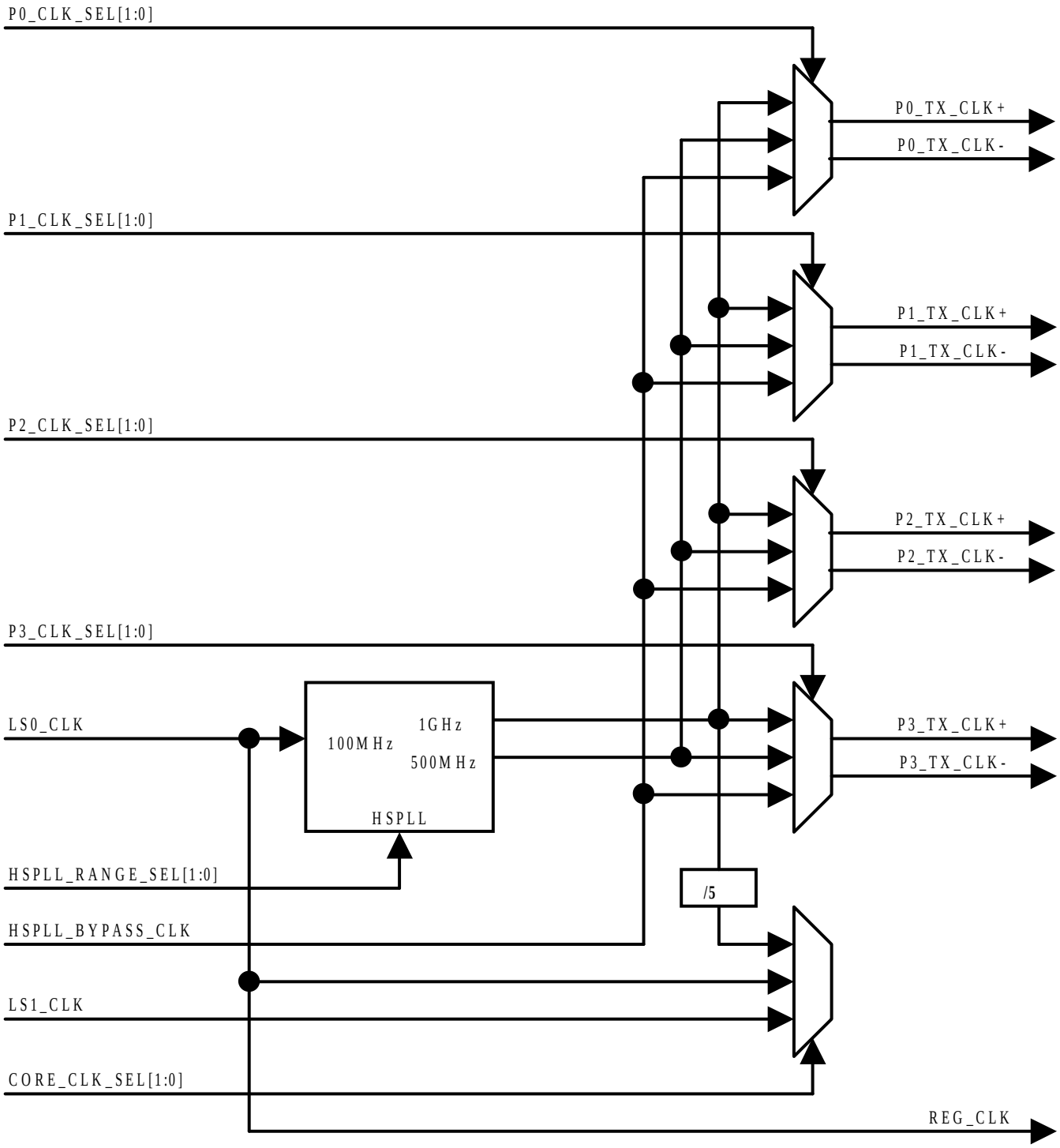


Figure 14-6. TSI500 RapidIO Clock Options

The selection of clock is made on a per port basis; each port being individually configurable.

The “slow” speed clock is provided by two separate clock signals, LS0_CLK and LS1_CLK. Although these are running at the same frequency, they must be provided to the TSI500 out of sync. This is achieved by a “RoboClock” device which skews the two clocks by a fixed amount, again, selectable on Torridon via jumpers/switches.

The high speed clock pair is generated from the same circuitry as the processors RapidIO_TX_CLK+/RapidIO_TX_CLK- clocks.

14.3.5 Clock Distribution on Torridon

The RapidIO sub-system in Torridon can operate either synchronously or asynchronously.

For synchronous operation, each RapidIO device shares a common clock source. The clock source is generated by a 16MHz oscillator. This clock source is fed into a clock synthesizer (ICS8442) where the frequency is multiplied by a PLL. The multiplication factor is set via switches. This multiplied clock frequency is distributed around the board via a clock buffer (ICS8516).

Asynchronous operation is very similar. The four processors operate from a common clock as described above but the switch operates from a separate source.

The diagram in Figure 14-7 shows the RapidIO clock distribution around Torridon.

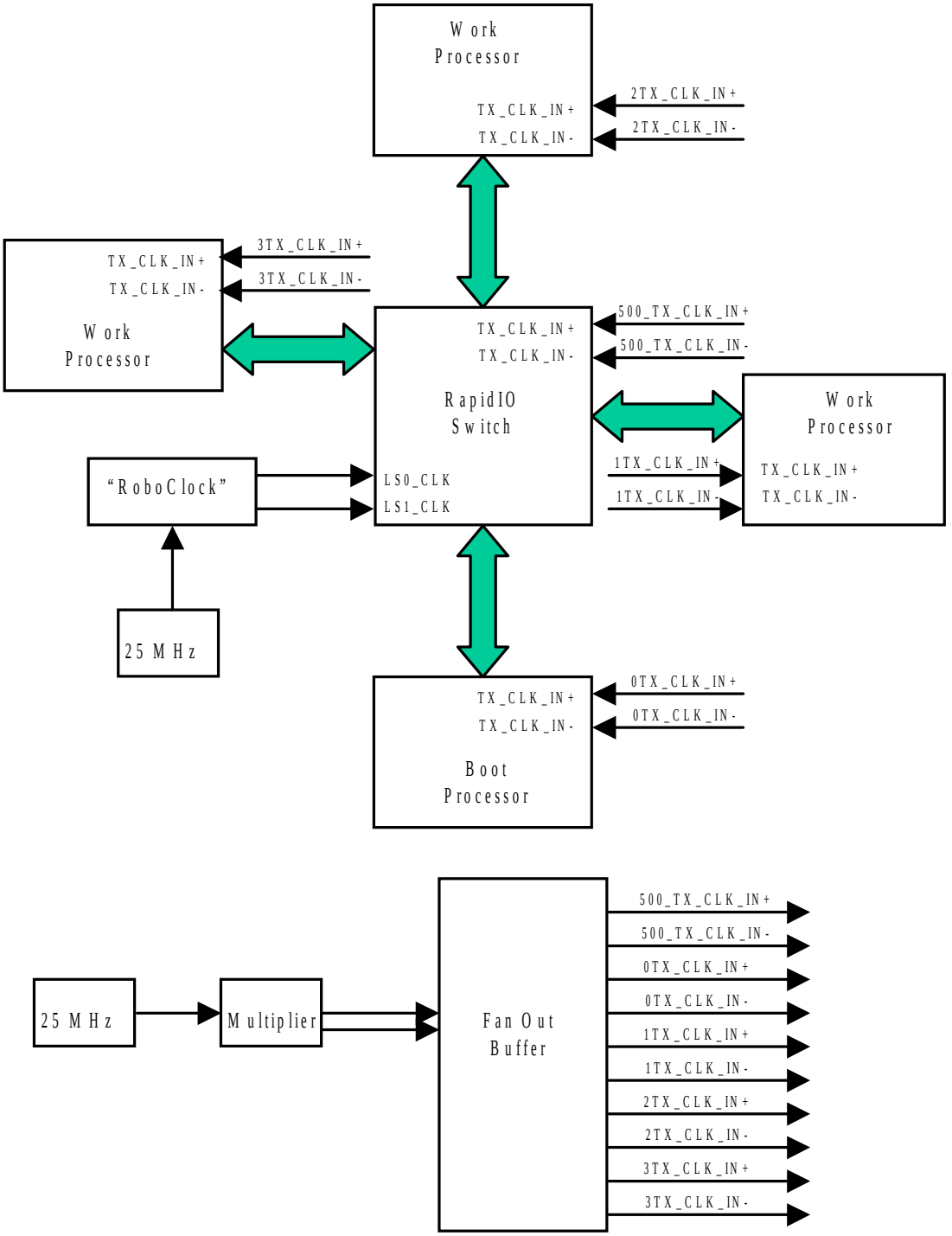


Figure 14-7. RapidIO Clock Distribution on Torridon

The schematics in Figure 14-8 show how this is implemented.

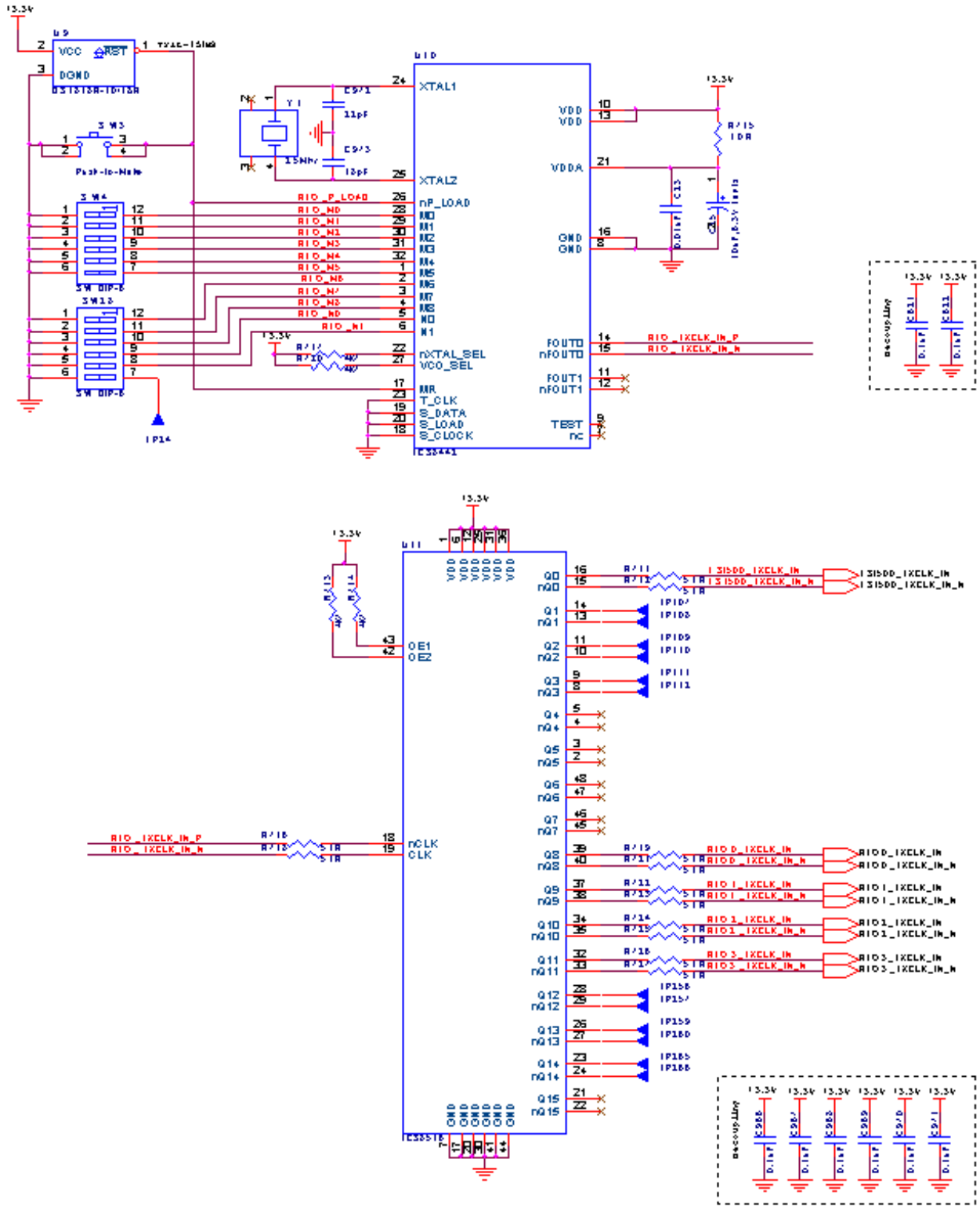


Figure 14-8. High Speed Clock Generation

The following should be noted about the circuitry.

- The base clock frequency is provided by a 25MHz crystal
- Switches select the multiplication factor
- A separate push to make switch allows the frequency multiplication to be changed on the fly without the need to power cycle the system
- Multiple, exact copies of the clock pairs are generated via a fan out buffer
- In line resistors reduce any over/under shoot on the clock lines.
- Adequate de coupling is required

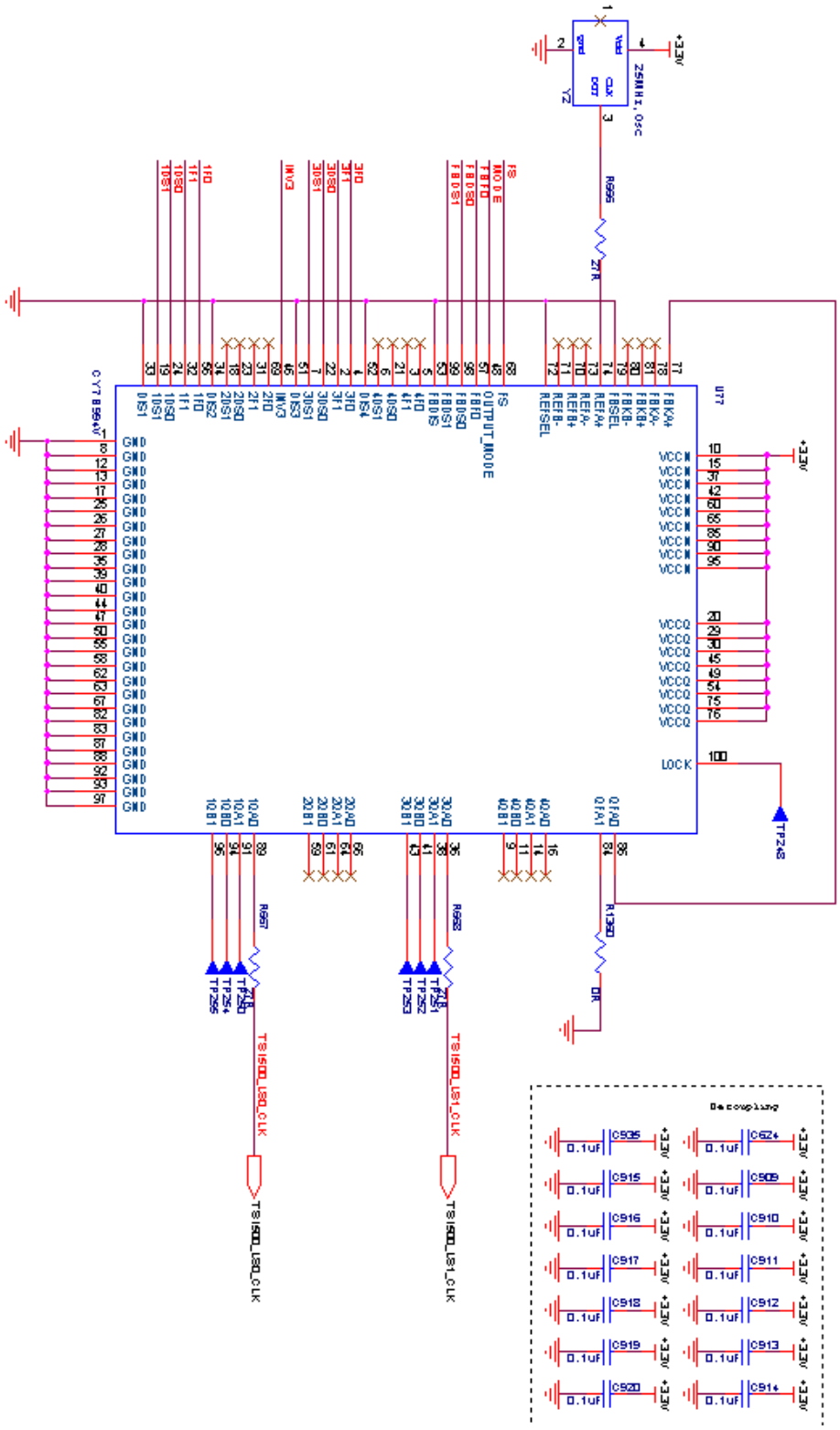


Figure 14-9. Slow Speed Clock Generation

The following should be noted about the circuitry.

- The configurations pins which adjust the frequency multiplication and skew are set via jumpers (not shown for simplicity)
- In line resistors reduce any over/under shoot on the clock lines.
- Adequate de coupling is required

14.4 Processor Real Time Clock

As well as the main clock, each processor uses a separate real time clock input. This clock has to be separate from the system clock and must be driven independently of the system clock.

On Torridon, a 16MHz crystal produces this clock input. As shown in Figure 14-10, a fan out buffer is used to distribute this clock signal so it may be driven to all four processors.

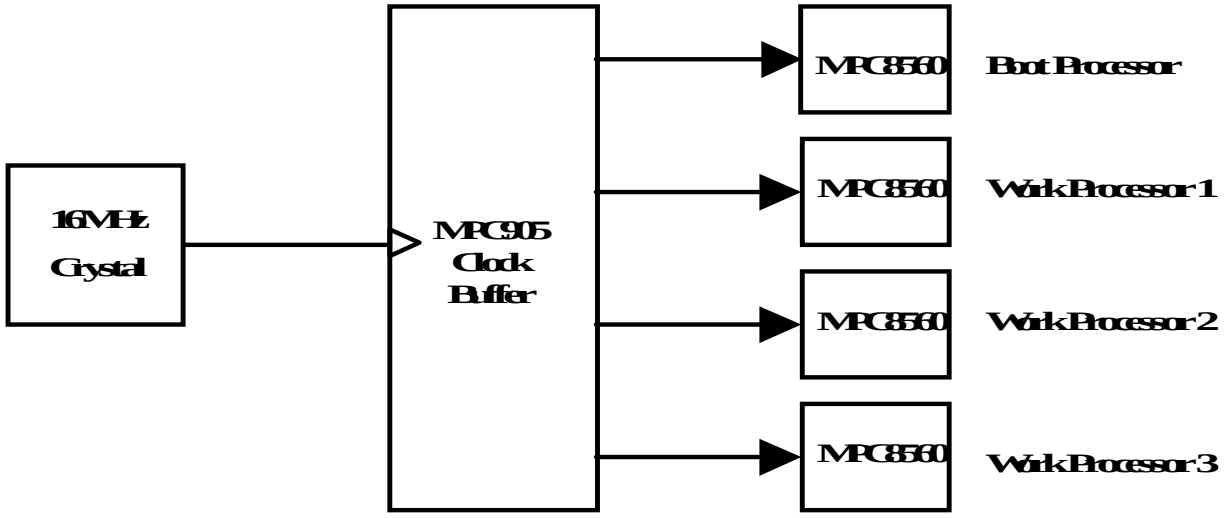


Figure 14-10. Processor Real Time Clocks

The diagram in Figure 14-11 shows the schematics for the real time clock circuitry

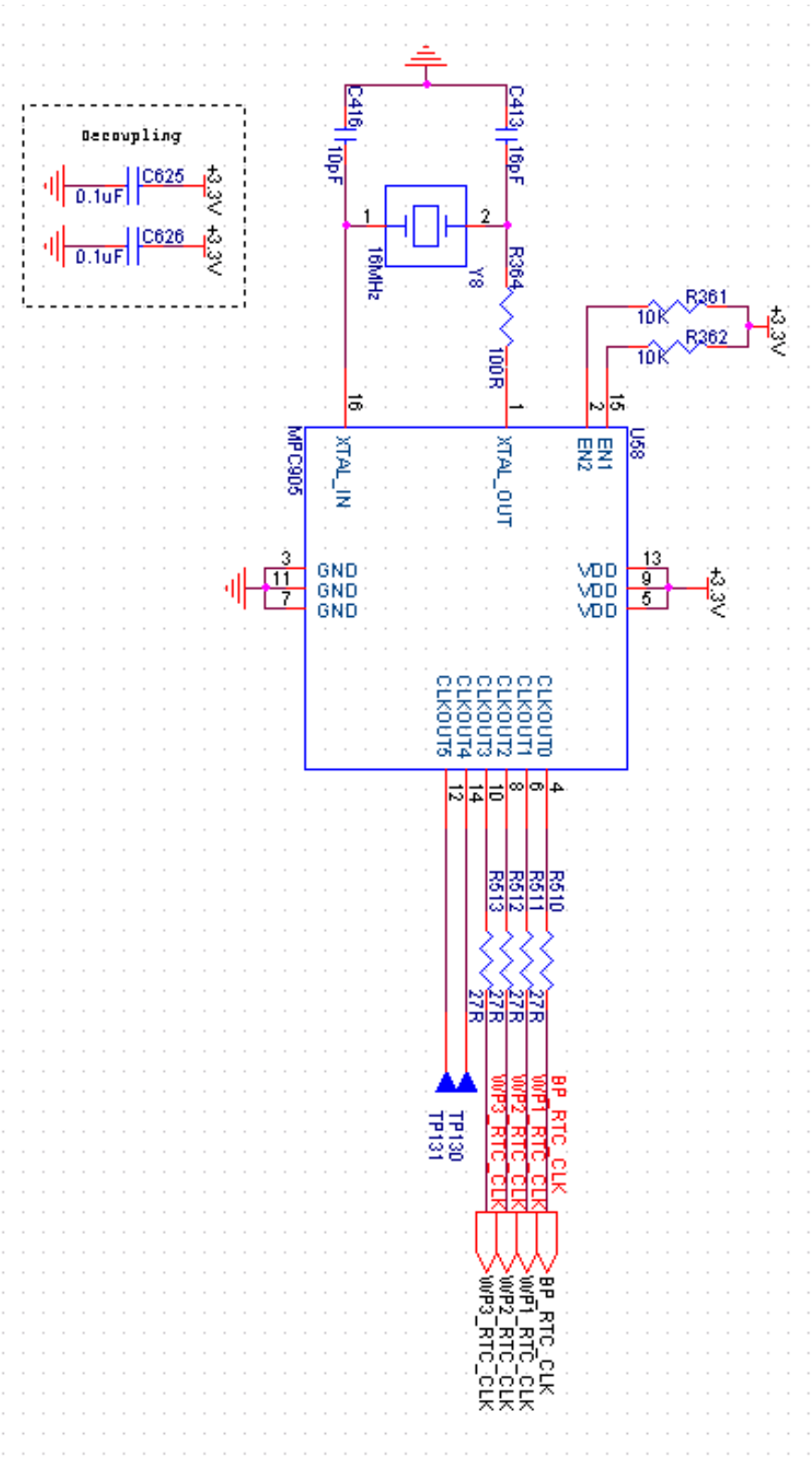


Figure 14-11. Processor Real Time Clocks - Schematics

The following should be noted about the circuitry.

- The capacitors (C413, C416) have been chosen to match the characteristics of the crystal
- Series resistors (27 ohm) are inserted on all the clock lines to avoid any over shoot
- As only four clock signals are required, a smaller part (MPC905) fan out buffer is used
- Adequate de coupling is required to the 3.3V power rail

14.5 GBit Ethernet Clocks

The MPC8560's Triple Speed Ethernet Controller (TSEC) requires an external clock to provide the stimulus for its transmit operation. A 125MHz clock input is require to operate the TSEC block. As shown in Figure 14-12, both of the TSEC blocks in an MPC8560 operate from the same clock input so only a single input is required.

On Torridon, Marvel 88E1011 devices provide the on-board GBit PHYs. The Marvel device provides the 125MHz clock to the MPC8560 from a 25MHz clock input.

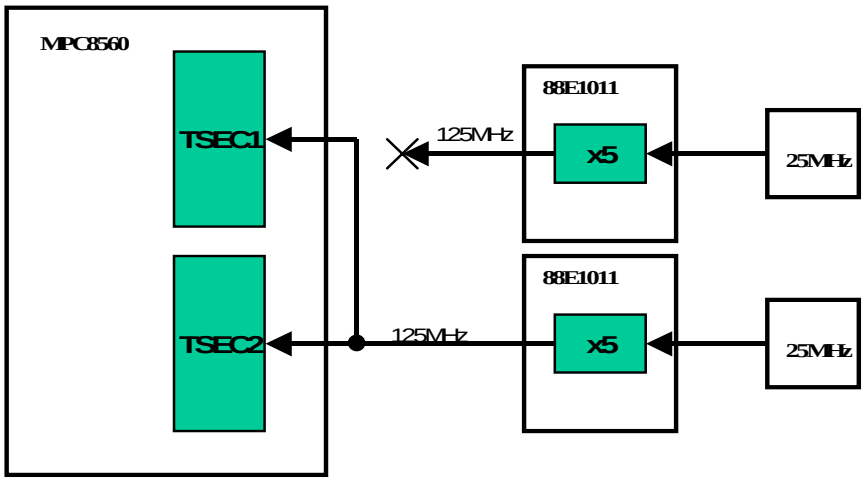


Figure 14-12. GBit Ethernet Clocks

Note: Although both PHYs produce a 125MHz clock, only one is required to drive both PHYs. The other is a no connect on the board.

14.6 Southbridge Real Time Clock

The Via Southbridge chip provides a real time clock. This clock is required by some operating systems, e.g. Linux, to monitor the absolute time. This is used for various operations such as time stamping files, monitoring file backups etc.

On Torridon, this clock is provided by a dedicated 32kHz crystal. To enable the real time clock to operate when the main power supply is not present, a battery may be fitted to the system. A “standard” 3.3 V battery (similar to those used in personal computers) may be plugged into a 4 pin header. (HD33 in the schematics below).

A 3 pin jumper, JP19, is used to select the source of power. When the battery is fitted, a jumper between pin 2 and 3 on JP19 will select the battery as the power source for the real time clock.

To operate the real time clock in the event of the battery not being present, a jumper should be placed across pins 1 and 2 on JP19. This will route the boards main 3.3V power supply to the real time clock. Although this will allow the real time clock to function, it will only run when the main power is applied to the system. Hence, if this mode of operation is used, the real time clock will not correctly indicate the actual time.

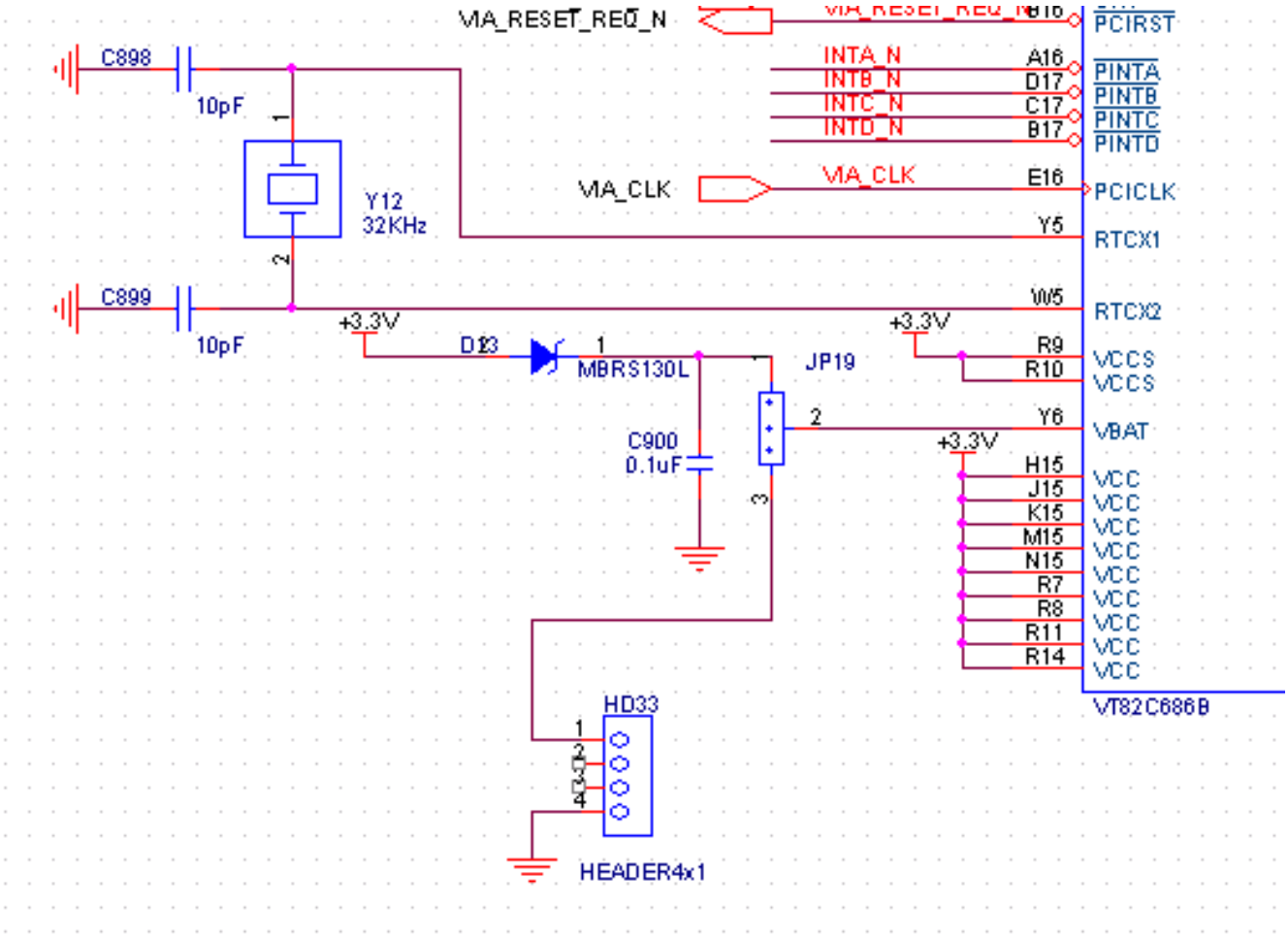


Figure 14-13. Real Time Clock Schematics

Chapter 15 Voltage Regulation

This section describes the Voltage Regulation sub-section on the Torridon Motherboard.

15.1 Overview

The Torridon system requires a number of different voltages to power the various components on board. In fact, the board uses seventeen different power supplies. The majority of these voltages are generated on board.

15.2 Power Available

The board receives its power from one of two sources.

- The backplane
- An ATX power supply.

The backplane will be provided by the end customer, so the supplied current will be variable depending on the specific implementation.

Table 15-1 shows the current supplied from an ATX power supply.

Table 15-1. Power Supplied from an ATX Power Supply

Voltage (Volts)	Current (Amps)
+3.3 V	28 A
+5 V	30 A
+12 V	15 A
+5VSB	2 A
-12 V	0.8 A
- 5 V	0.3 A

NB: Numbers given for a 300W, ATX 12V supply.

15.3 Power Required

Table 15-2 shows the main components on the board and their respective power requirements.

Table 15-2. Power Required

Device	no. On Board	I/O Voltage (Volts)	Core Voltage (Volts)	Power per Device (Watts)	Total POwer (Watts)
MPC8560	4	3.3 V	1.2 V	8 W	32 W
RapidIO Switch	1	3.3 V	3.3 V	1.5 W	1.5 W
DDR SDRAM	4	2.5 V	2.5 V	2.5 W	10 W
Clock Buffer	1	3.3 V	3.3 V	2.6 W	2.6 W
GBit PHY	5	3.3 V	3.3 V	1.2 W	6 W
Total					52.1 W

15.4 Power Distribution

Torridon requires four voltages to operate correctly. These are as follows

- +12V
- +5V
- +3.3V
- +5VSB

All the other voltages are generated from these stimulus.

The diagram in Figure 15-1 shows the power distribution around the board.

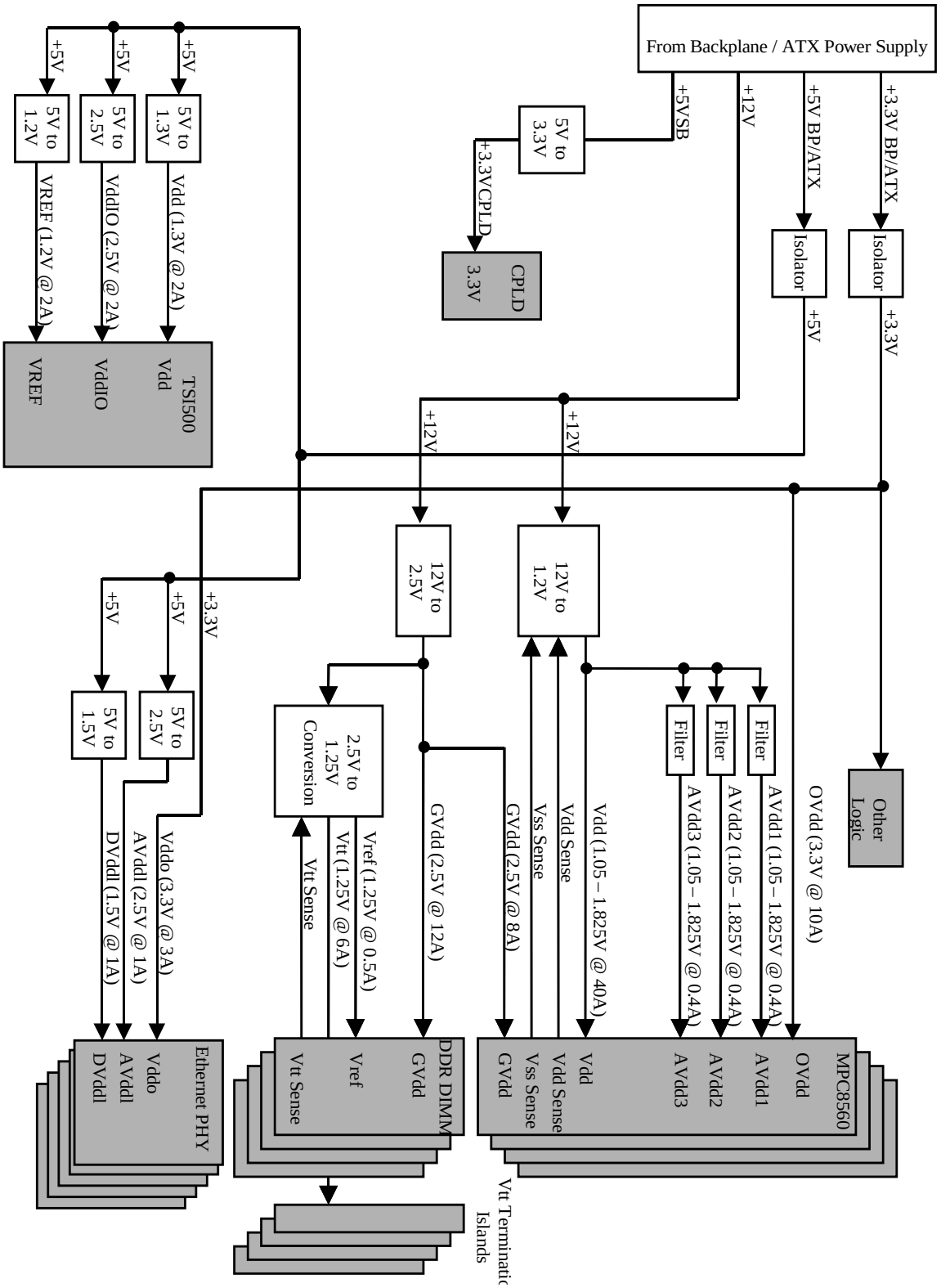


Figure 15-1. Power Distribution

The board must be supplied by four separate power supplies; +3.3V, +5V, +12V and +5VSB. All the other voltages are produced on board. The +5VSB is used to power the CPLD which is responsible for system reset and power up sequencing. Two separate isolators are used to turn the 5V and 3.3V onto the board. These switches allow the voltages to be turned on in a specific sequence. The sequence is detailed in Section 15.6, “Power Sequencing”.

15.5 Voltage Generation

The diagram in Figure 15-1 above shows the power distribution around the system. The areas to be discussed are

- CPLD Power
- 5V/3.3V Switching
- MPC8560
- DDR SDRAM
- GBit Ethernet
- TSI500 RapidIO Switch

Each of these will be discussed in detail.

15.5.1 CPLD Power

The CPLD is responsible for controlling the resets and sequencing the power supply. This means that the CPLD must be powered on first. The 3.3V power supply for the CPLD is generated from the 5V Stand By (+5VSB). This voltage is present even before the ATX power supply is turned on with its “Power ON” signal. The CPLD is responsible for turning on the ATX power supply so it can not be powered from the “normal” 5V or 3.3V supply as they will not be present initially.

The 3.3V power is generated from the +5VSB using a MAXIM MAX1831 voltage regulator. See Figure 15-2.

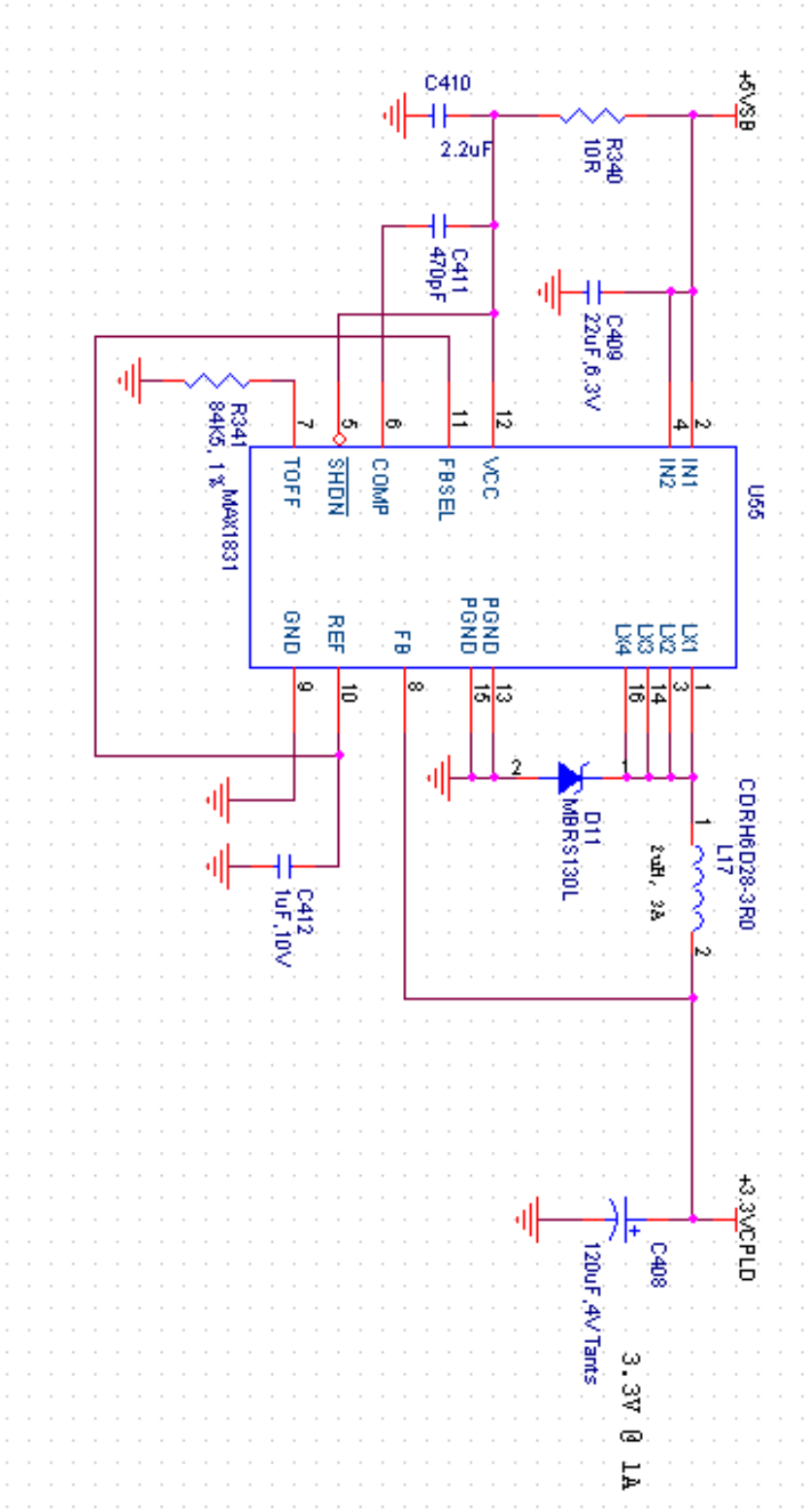


Figure 15-2. CPLD Power - Schematics

The following should be noted about the schematics in Figure 15-2 above:

- The stand by voltage (+5VSB) provides the input power
- Connecting the FBSEL pin directly to the REF pins sets the voltage to 3.3V. No resistor divider network is required.

15.5.2 5V/3.3V Switching

The 5V and 3.3V power supplies, which come directly from the ATX (or the backplane), are turned on via FETs. This allows the various voltages on the board to be turned on in a specific sequence. See Figure 15-3.

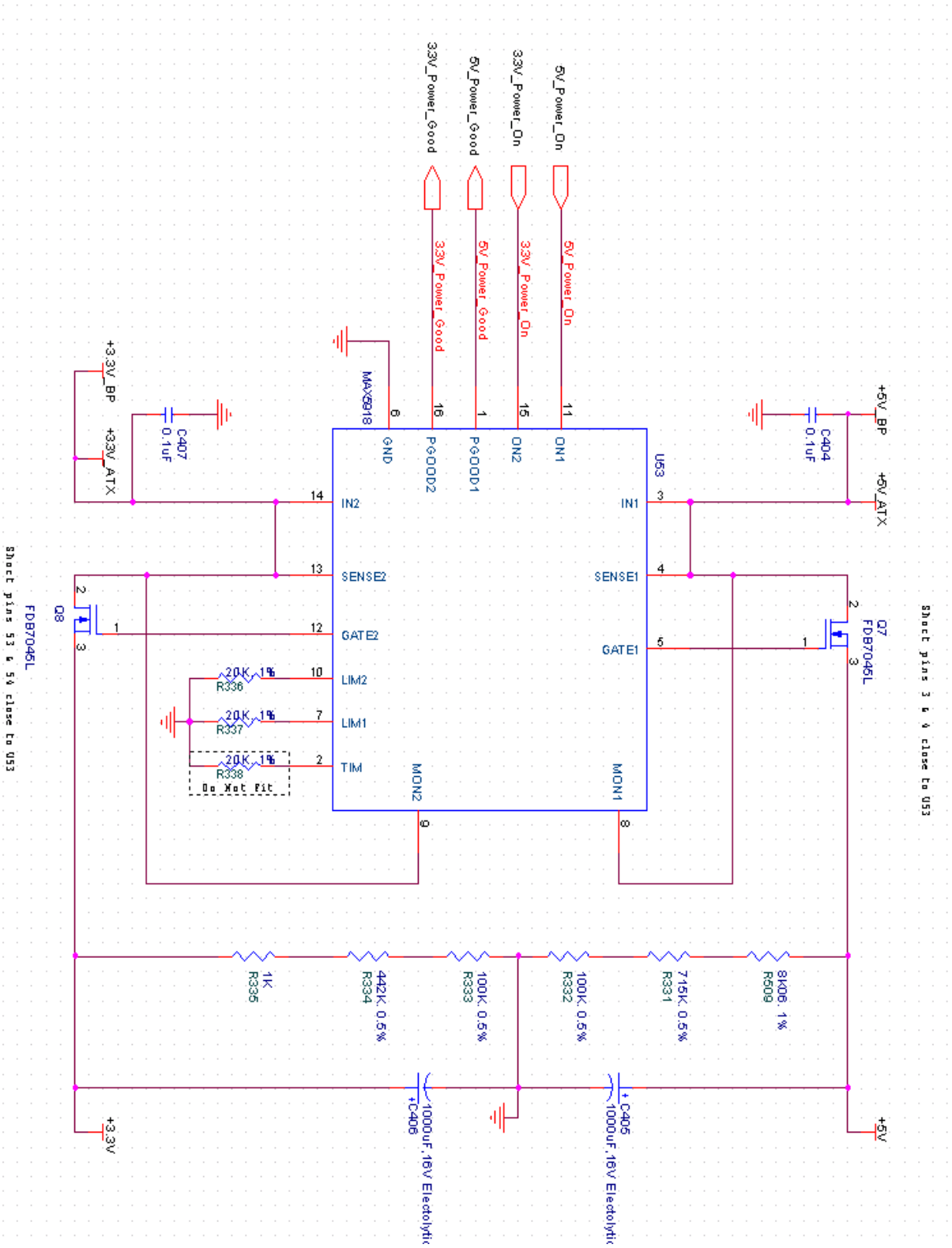


Figure 15-3. 3.3V/5V Isolator - Schematics

The following should be noted about the schematics in Figure 15-3 above: The sense resistors are not used. (This simplifies layout)

15.5.3 MPC8560

15.5.3.1 MPC8560 Power Requirements

Table 15-3 details the power requirements for one of the processors.

Table 15-3. MPC8560 Power Requirements

Characteristic	Power Source	Voltage	Est. Current	Max. Current
Core Supply Voltage	V_{DD}	0.8V - 1.5V	10A	20A
PLL Supply Voltage	AV_{DD}[1:3]	0.8V - 1.5V	0.1A	0.1A
DDR DRAM I/O Voltage	GV_{DD}	2.5V	XA	2A
Three-speed Ethernet I/O, MII Management Voltage	LV_{DD}	3.3V	xA	1A
PCI/PCI-X, local bus, RapidIO, 10/100 Ethernet, DUART, system control and power management, I^2C, and JTAG I/O voltage	OV_{DD}	3.3V	XA	1.5V

15.5.3.2 Core & PLL Voltage

The MPC8560's core and PLL circuitry requires a voltage of between 0.8 and 1.5V at a maximum current of 20.1A. Hence for the four processors, a maximum current of 80.4A should be available. This power supply is generated from the 12V power rail using a POL (Point of Load) power module from Artesyn, the NXI100, shown in Figure 15-4.

Figure 15-4. NXI100 Power Module

The NXI100 is a point of load DC/DC convertor capable of delivering up to 81A. The module complies to the VRM9.0 specification.

The output voltage from the NXI100 is set using five configuration pins, VID0–VID4. The NXI100 uses an internal 5-bit DAC as a feedback-resistor voltage divider. The output voltage can be digitally set in 25mV increments from 1.1V to 1.85V using the VID0–VID4 inputs. The schematics in Figure 15-5 and Figure 15-6 show how the NXI100 module is used on Torridon.

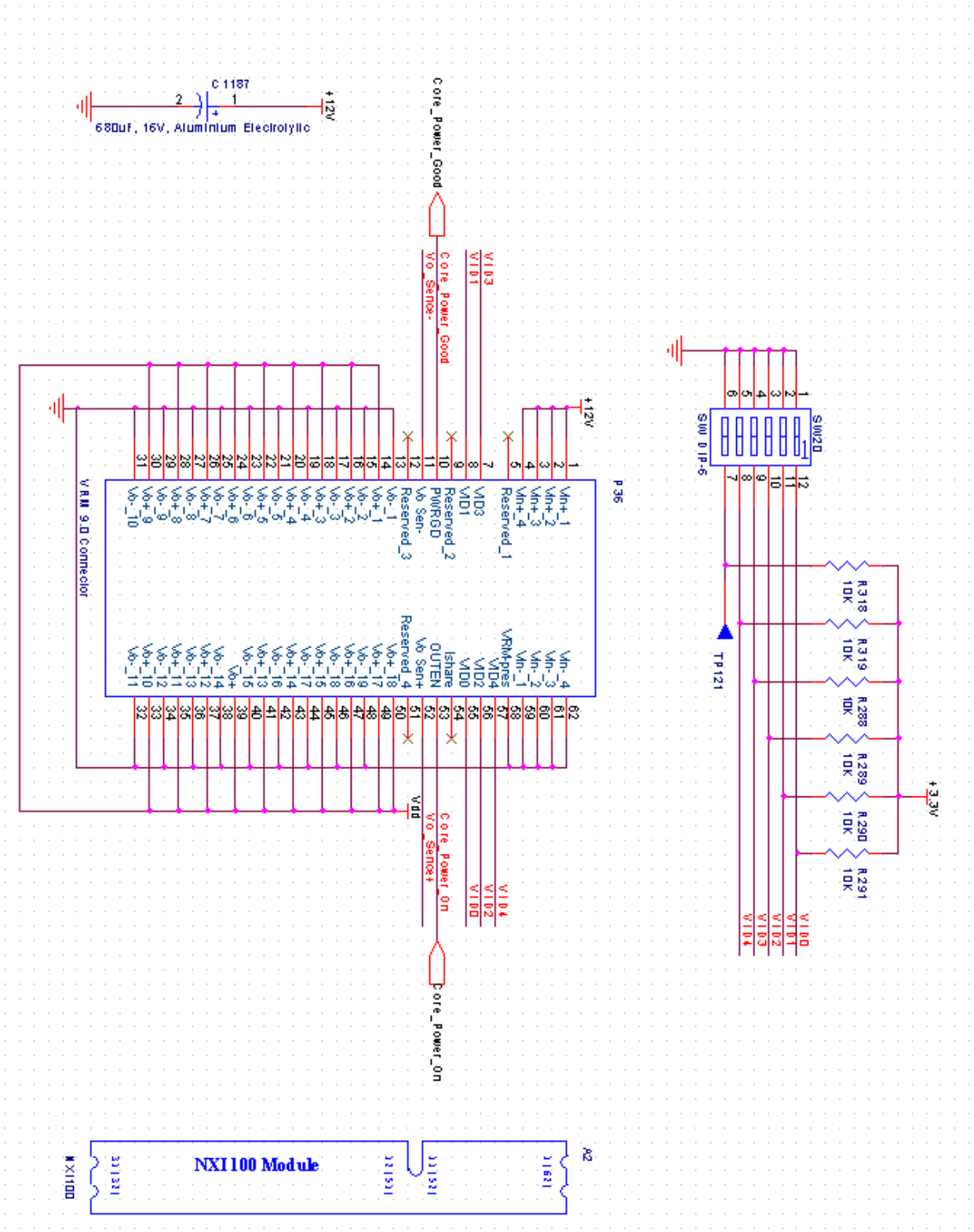


Figure 15-5. Vdd Power - Schematics

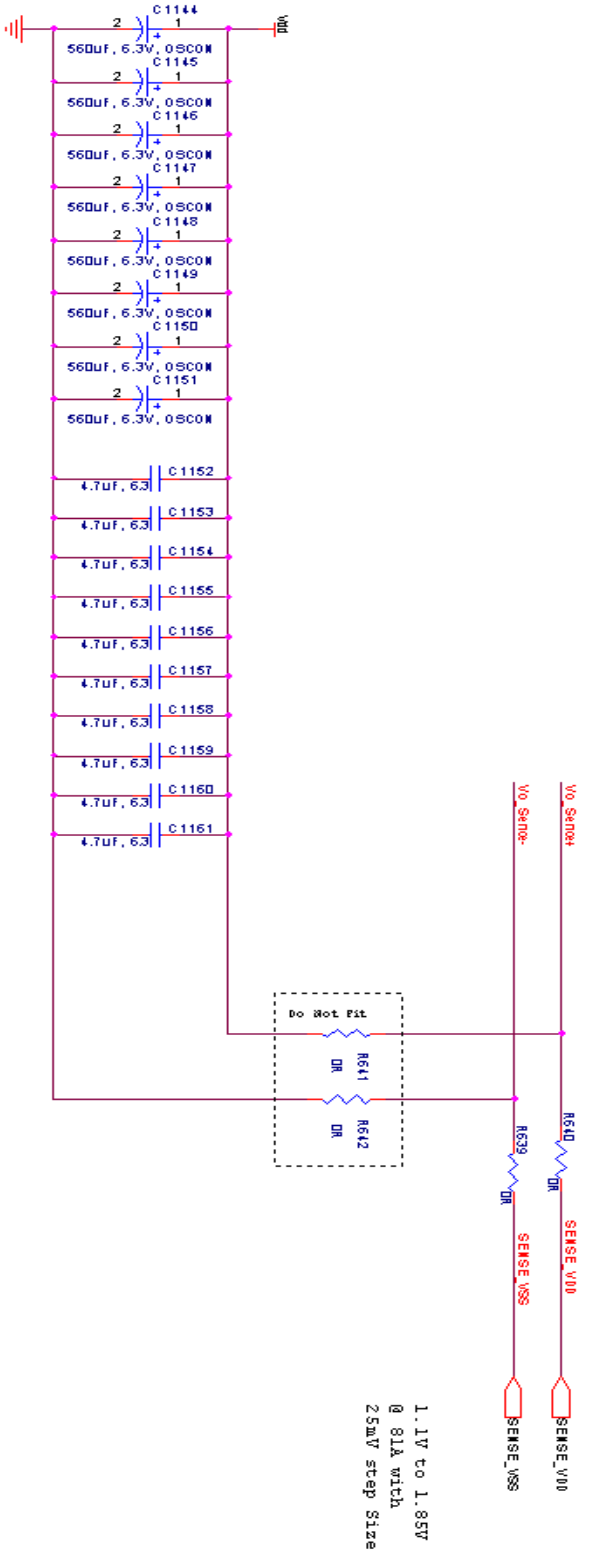


Figure 15-6. Vdd Power - Feedback- Schematics

The following should be noted about the schematics in Figure 15-5 and Figure 15-6 above.

- The VID settings are configured using DIP switches. This allows the voltages to be easily changed. For example, to allow for a subsequent, low power version of the processor
- Low ESR (Equivalent Series Resistance) capacitors are used to de couple the output (Vdd) voltage
- The NXI100 uses a feedback network to monitor the voltage at point of load and, if necessary, adjust to allow for any voltage drop. (For example, if the point of load was physically a long distance away). Zero ohm resistors are used to allow the point of testing to be changed.

As well as the core voltage, the NXI100 also provides the voltage for the processors PLL circuitry. The Vdd power is fed through an RC network to provide the PLL voltage. See Figure 15-7.

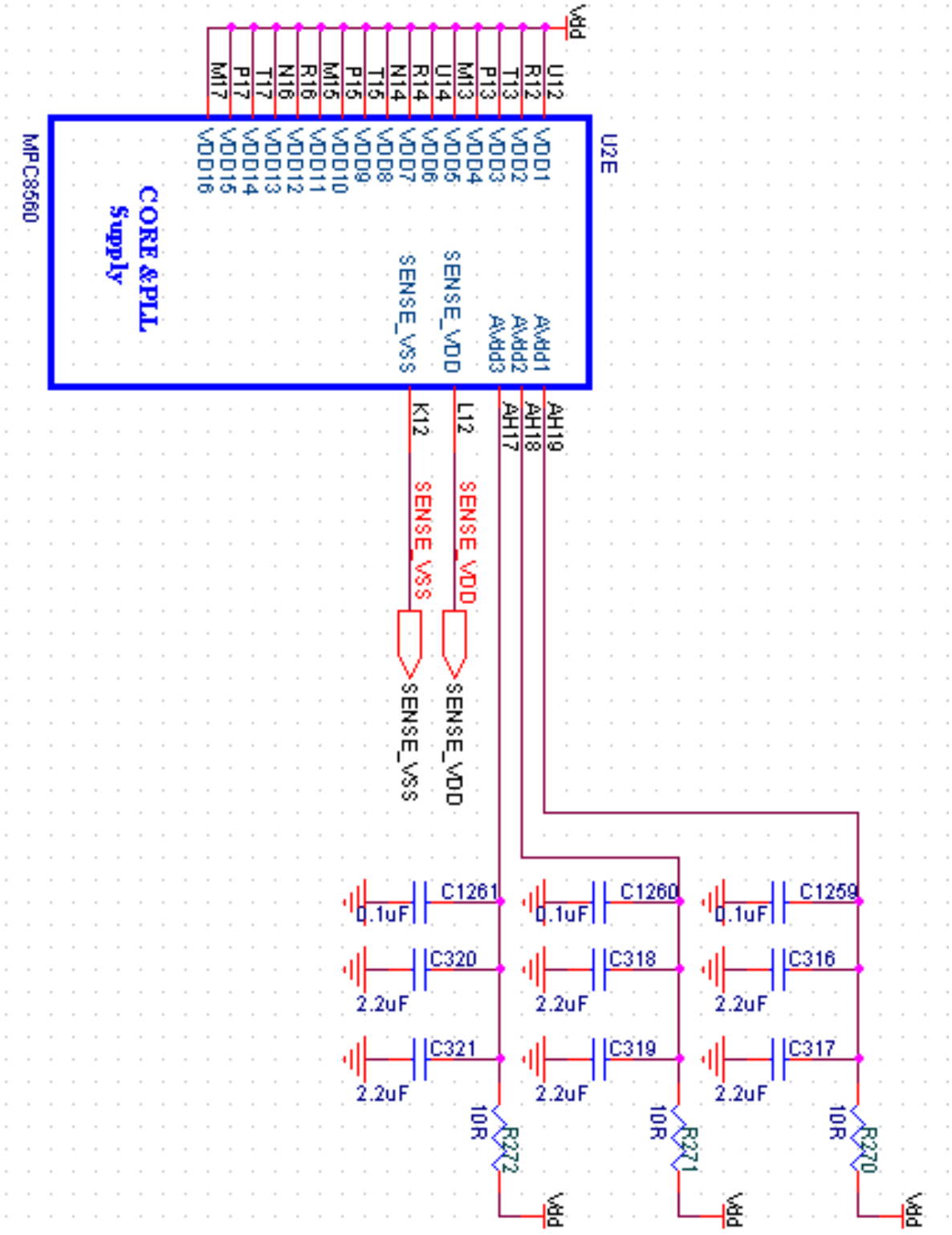


Figure 15-7. PLL Power - Schematics

15.5.3.3 DDR DRAM I/O Voltage

The MPC8560's DDR DRAM I/O circuitry requires a voltage of 2.5V at a maximum current of 2A. This power supply is generated from the 12V power rail using an Artesyn module, DDR12, shown in Figure 15-8.

Figure 15-8. DDR12 Module

The DDR12 is also a point of load DC/DC convertor capable of producing 2.5V at 25A and 1.25V at 8A.

Note: Although the module is capable of generating the Vdd voltage (2.5 V) and the Vtt voltage (1.25V); on Torridon the DDR12 module is only used to supply the Vdd voltage (2.5V). The termination voltage (V_{TT}) is generated locally for each individual V_{TT} island. This method simplified the board layout.

Unlike the NXI100 module which used voltage ID pins (VIDs) to specify the output voltage, the DDR12 uses a simple resistor divider network to set the required output voltage. This voltage can be adjusted from 2.25V to 2.75V by changing a resistor value from open circuit to 41.7 ohms. The schematics in Figure 15-9 show how the 2.5V is generated on Torridon.

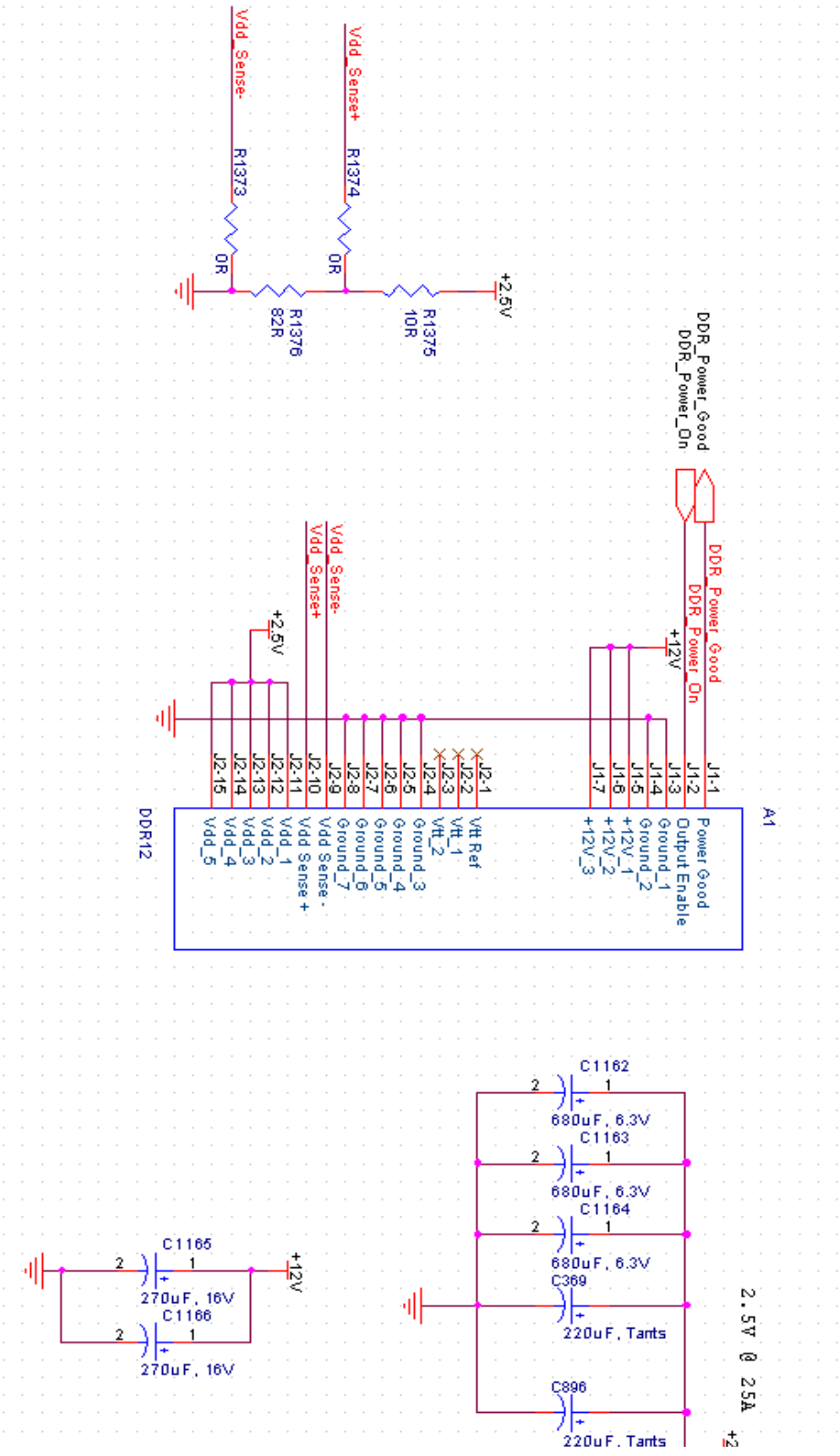


Figure 15-9. 2.5V Voltage Generation

The following should be noted about the schematics in Figure 15-9 above:

- The output voltage is set to 2.5V using R1376.
- Low ESR (Equivalent Series Resistance) capacitors are used to de couple the output (Vdd) voltage
- Power On/Power Good signals are available for control/monitoring by the power on state machine.

15.5.3.4 I/O Voltage

The MPC8560's I/O circuitry requires a voltage of 3.3V at a maximum current of 2.5A. This power supply is taken directly from the 3.3V power rail provided.

15.5.4 DDR SDRAM

As well as 2.5V, the DDR SDRAM requires a termination voltage of 1.25V. Although it is possible to produce this voltage rail from the DDR12 module, the 1.25V required for each DIMM is generated locally. This method simplifies signal routing and layout.

A National Semiconductor LP2995 device is used to generate a 1.25V signal from the 2.5 V signal. The schematics are shown in Figure 15-10.

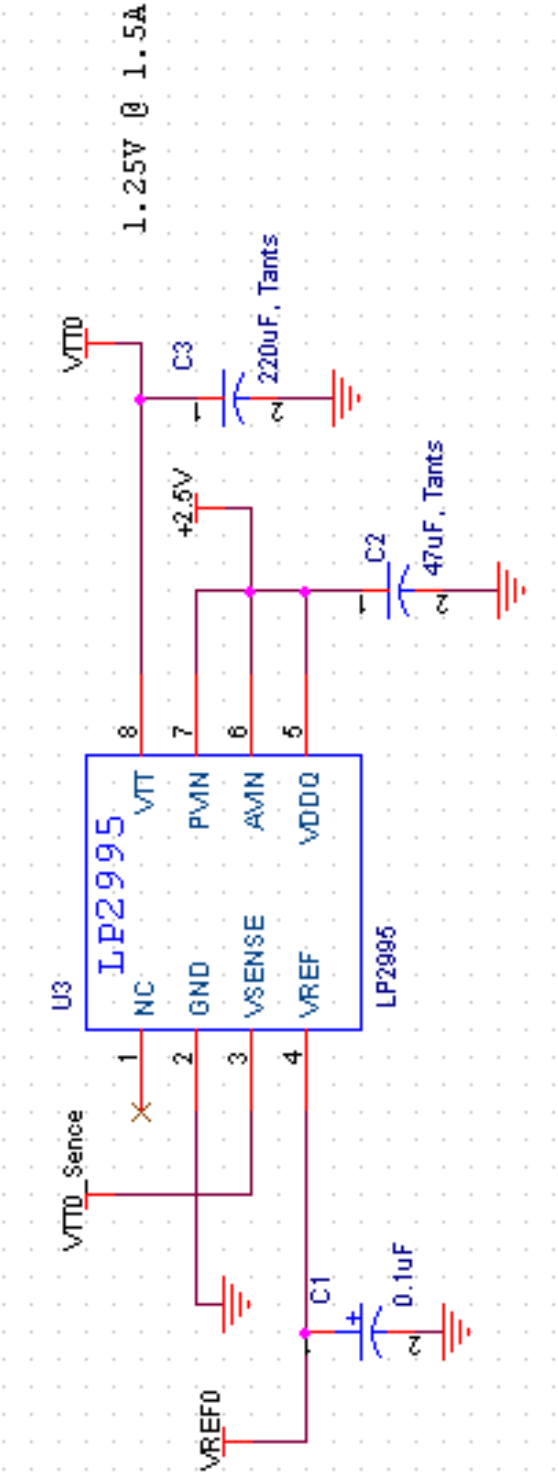


Figure 15-10. 1.25V Signal Generation

The following should be noted about the schematics in Figure 15-10 above:

- To distinguish the four separate 1.25V islands on Torridon, they are labeled VTT0, VTT1, VTT2 and VTT3.
- A sense signal, VTTx_Sense, is a tap taken from the midpoint of the VTT island. This tracks the voltage and adjusts, if required.

15.5.5 GBit Ethernet

In addition to a 3.3V supply, (which is taken from the 3.3V ATX power rail/backplane), the Ethernet PHYS also require 2.5V and 1.5V. Both of these voltage are generated using two separate MAXIM ‘1831 devices. The schematics are shown in Figure 15-11 and Figure 15-12.

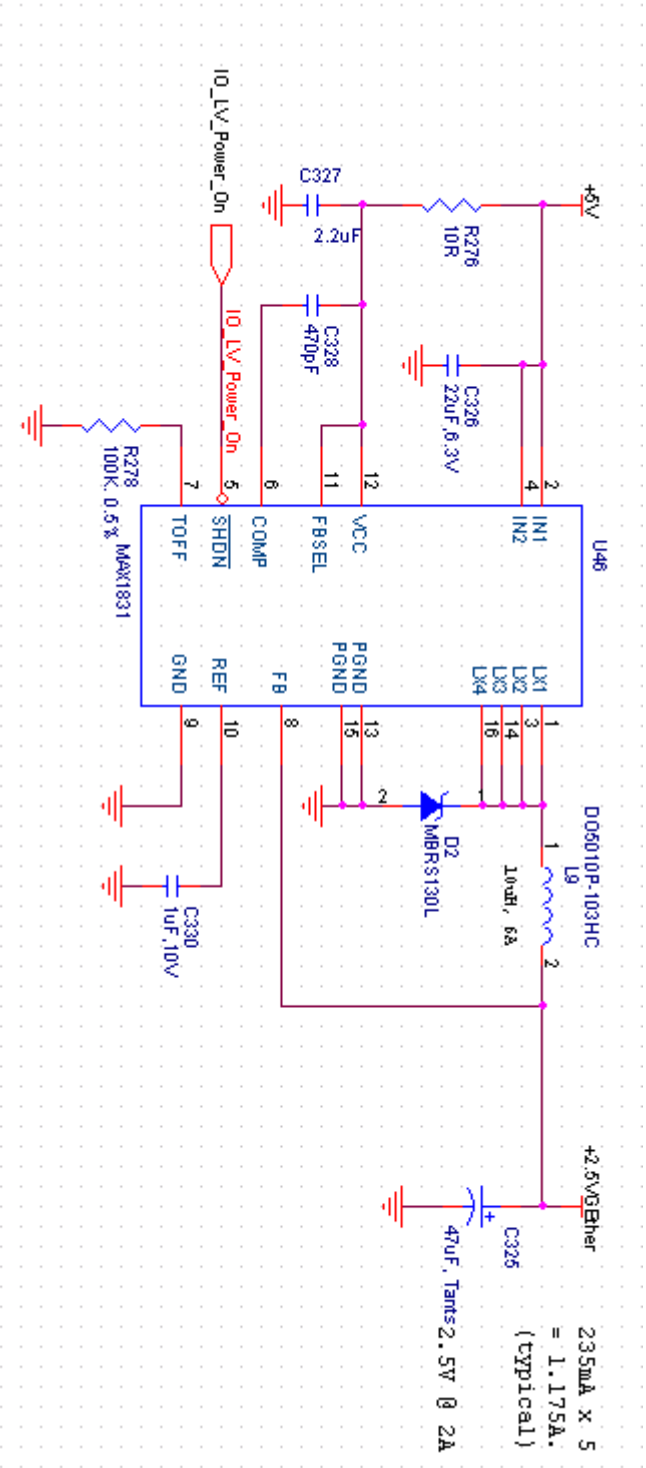


Figure 15-11. GBit Ethernet - 2.5V Generation

The following should be noted about the schematics in Figure 15-11 above: The output voltage is fixed at 2.5V by tying the FBSEL pin to VCC (+5V)

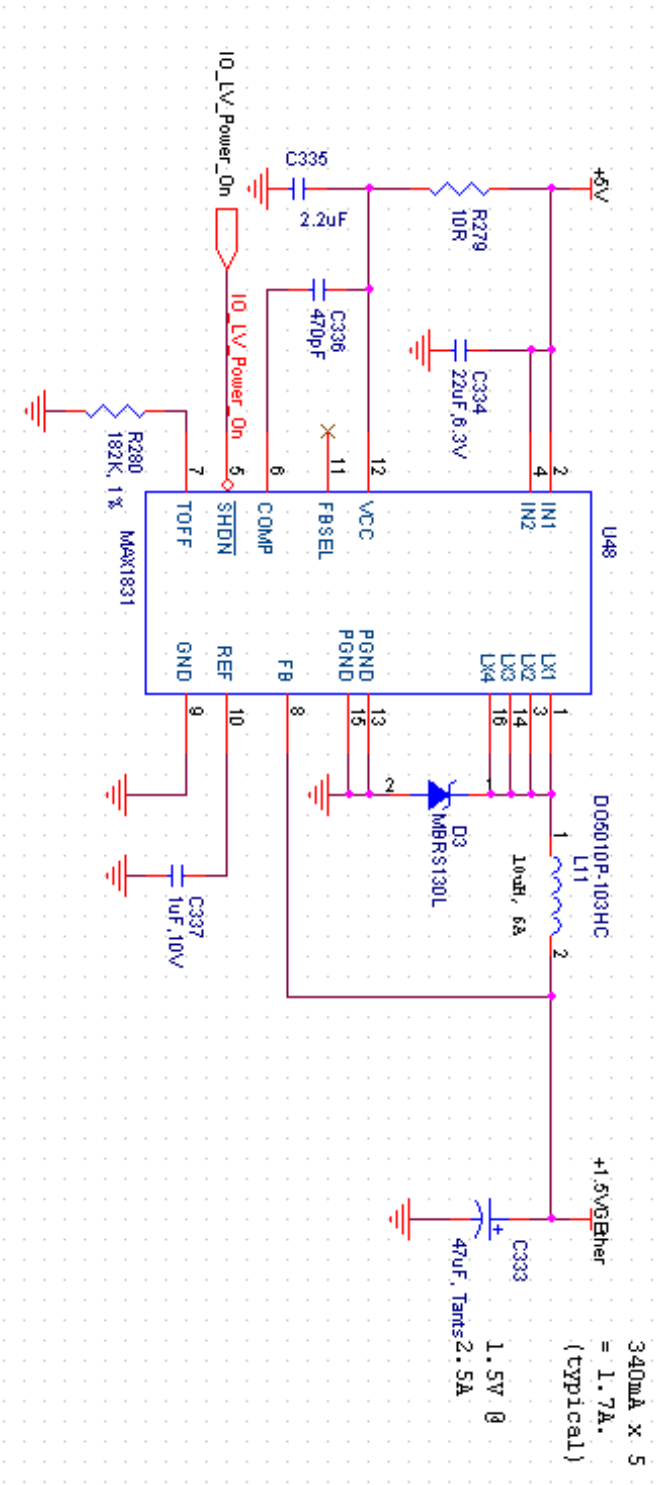


Figure 15-12. GBit Ethernet - 1.5V Generation

The following should be noted about the schematics in Figure 15-12 above: The output voltage is fixed at 1.5V by leaving the FBSEL pin unconnected.

15.5.6 TSI500

In addition to a 3.3V supply, (which is taken from the 3.3V ATX power rail), the TSI500 also requires 2.5V, 1.3V and 1.2V. These voltages are generated using three separate MAXIM ‘1831 devices. The schematics are shown in Figure 15-13, Figure 15-14, and Figure 15-15.

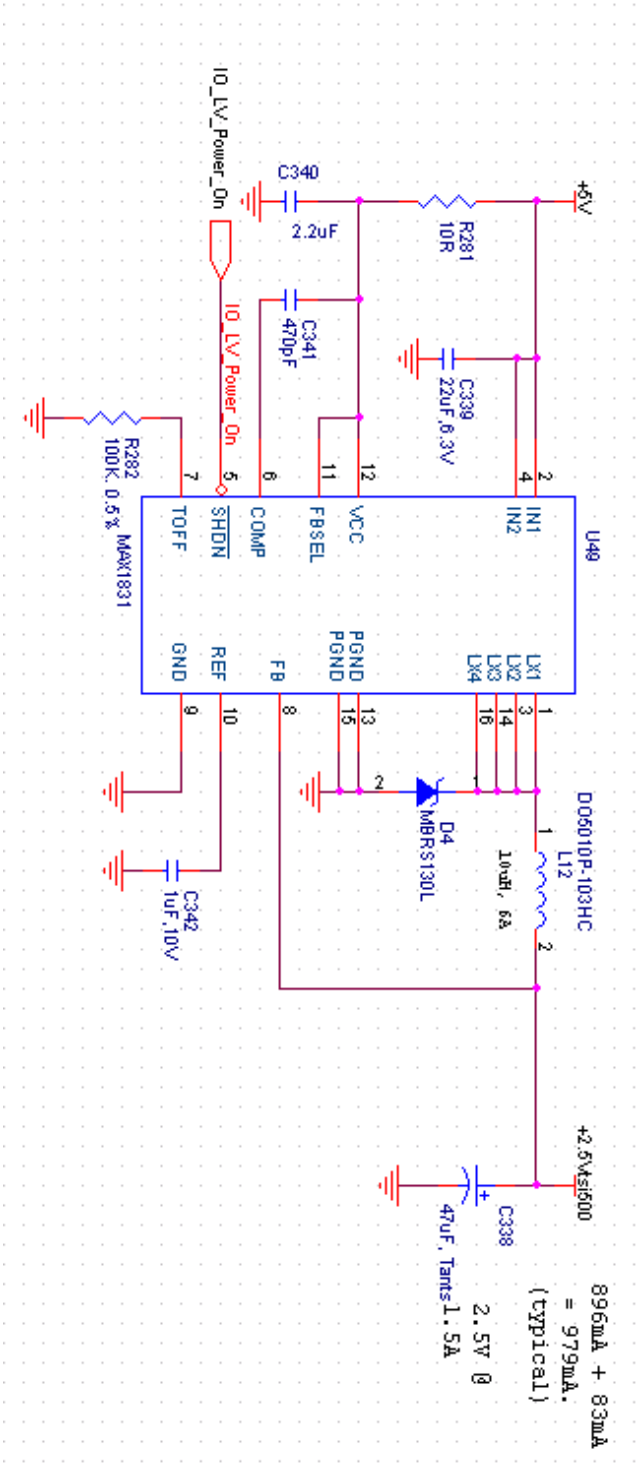


Figure 15-13. TSI500 - 2.5V Generation

The following should be noted about the schematics in Figure 15-13 above: The output voltage is fixed at 2.5V by tying the FBSEL pin to VCC (+5V)

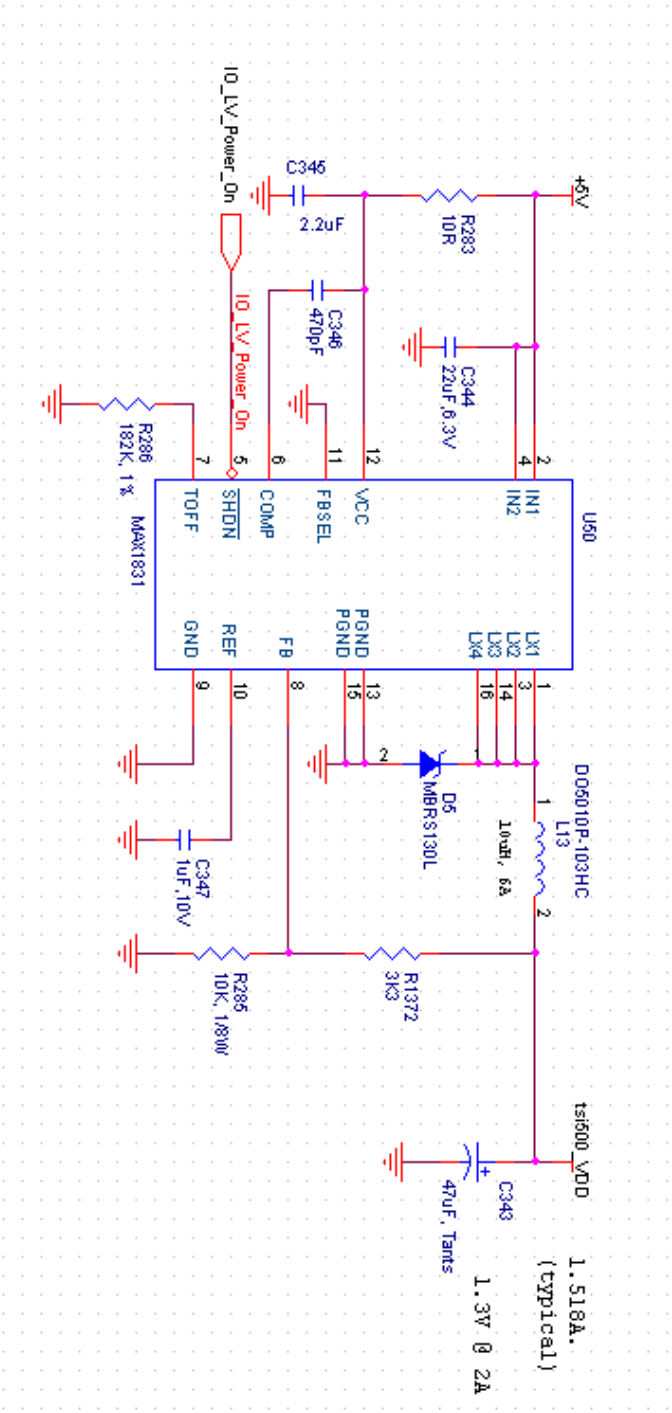


Figure 15-14. TSI500 - 1.3V Generation

The following should be noted about the schematics in Figure 15-14 above:

- The output voltage is fixed at 1.3V using a resistor divider network. (R1372 & R285)
- FBSEL is tied to ground

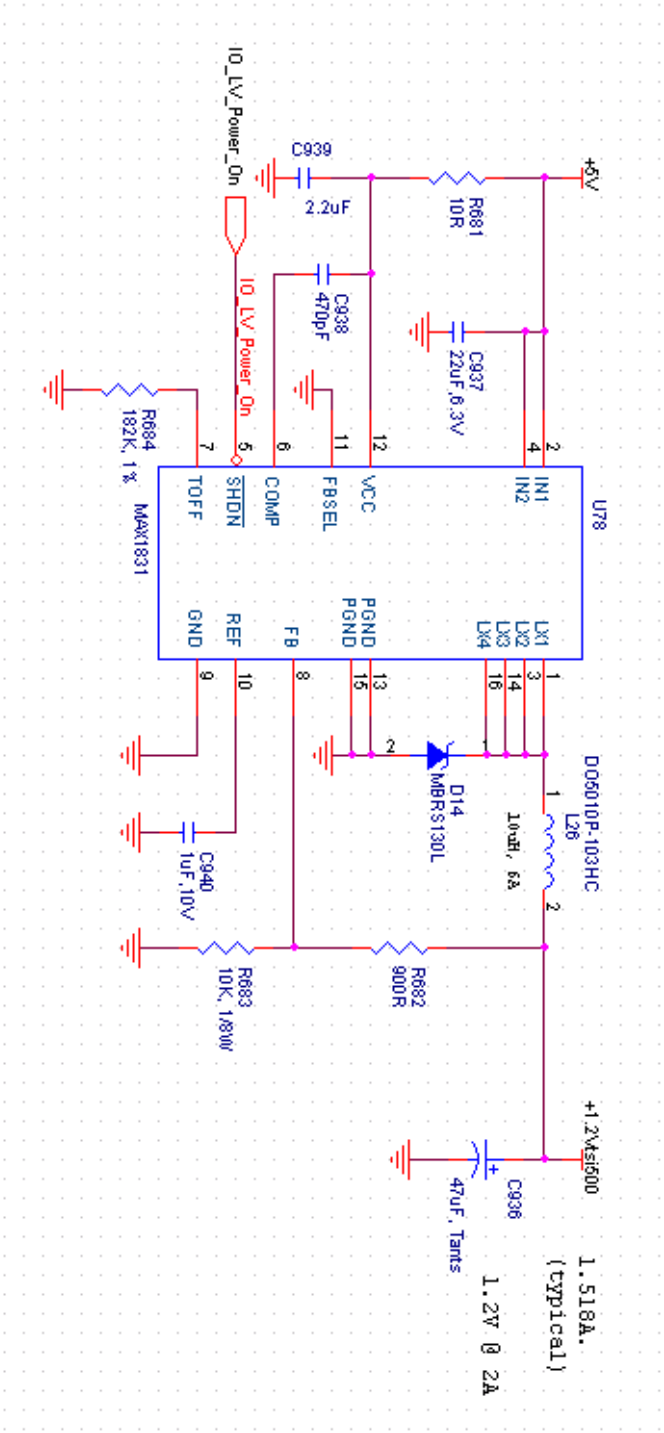


Figure 15-15. TSI500 - 1.2V Generation

The following should be noted about the schematics in Figure 15-15 above:

- The output voltage is fixed at 1.2V using a resistor divider network. (R682 & R683)
- FBSEL is tied to ground

15.6 Power Sequencing

To ensure correct operation, it is imperative that the board is powered up in a controlled manner. This is achieved by the use of a simple state machine implemented in a CPLD.

A CPLD (EMP3128) is responsible for the power up sequence of the board. The diagram in Figure 15-16 shows the sequence of events.

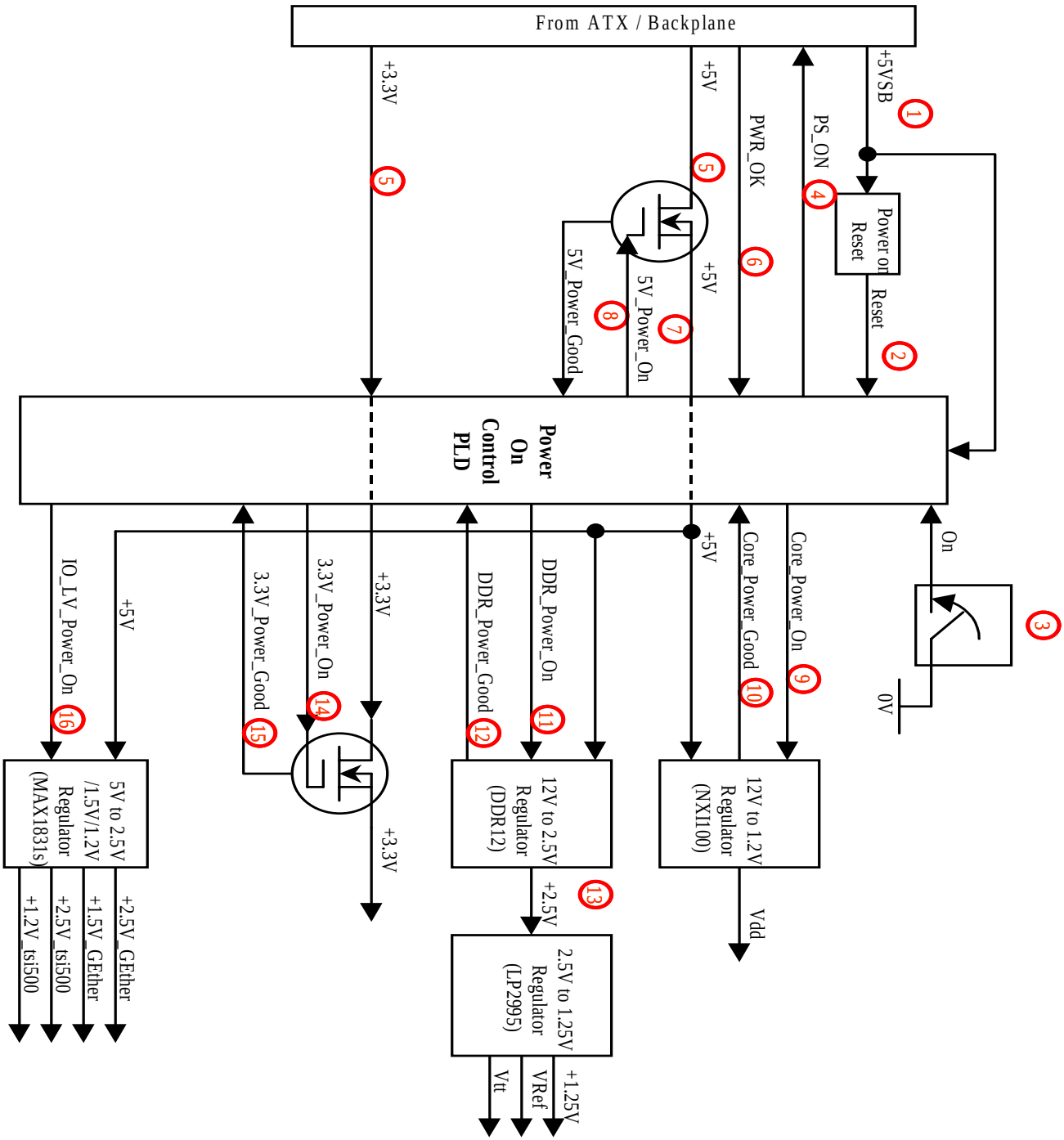


Figure 15-16. Power-Up Sequence

The power up sequence for Torridon is as follows:

1. The ATX/Backplane Power Supply supplies +5VSB (+5V Stand By) immediately after power is applied. PS_Ready LED lights
2. This voltage (+5VSB) is used by a DS1818 voltage monitor chip to generate a system power on reset signal, (PORST), to the CPLD only. At this point, the sequence stops, awaiting intervention from the user.
3. Operator pushes the on/off switch to turn the system on.
4. A Power Supply On (PS_ON) signal is sent back to the power supply.
5. The power supply generates all the required voltages (i.e. 3.3V, 5V and 12V)
6. The power supply sends a Power OK (PWR_OK) signal to Torridon to indicate that the power is on.
7. Torridon turns on the 5V power rail via the 5V_Power_On Signal.
8. A voltage monitoring device (MAX5918) checks the 5V rail and sends a 5V_Power_Good signal to the power on state machine
9. Torridon turns on the core power rail via the Core_Power_On Signal
10. A voltage monitor (NXI100) checks the Vdd rail and sends a Core_Power_Good signal to the power on state machine
11. Torridon turns on the +2.5V power rail (for DDR) via the DDR_Power_On Signal
12. A voltage monitor (DDR12) checks the +2.5V rail and sends a DDR_Power_Good signal to the power on state machine
13. The +2.5V power rail is regulated via four National Semiconductor ('2995) devices (one per processor) to generate the other required voltages for DDR (+1.25V, VRef, Vtt)
14. Torridon turns on the 3.3V power rail via the 3.3V_Power_On Signal
15. A voltage monitoring device (MAX5918) checks the 3.3V rail and sends a 3.3V_Power_Good signal to the power on state machine
16. Torridon turns on the lower voltages to the peripherals (2.5V, 1.5V, 1.2V) via the IO_LV_Power_On Signal

Chapter 16 Processor Sockets

This section describes the processor socket used on the Torridon Motherboard.

16.1 Overview

During the development of the Torridon system, the PowerQUICCIII silicon was very new and fresh out of fabrication. In such an situation, it was deemed necessary to be able to easily change the processors on the motherboard. This prompted the decision to use sockets for the processors.

16.2 The Need For Sockets

Typically during the initial release of new silicon, different behaviors can been seen over the range of parts available. These differences in behavior can be due to numerous reasons such as differences in process, test screening or device errata. Whatever the reason, it is advantageous to be able to easily replace processors on the motherboard.

Typically, processors would be removed simply by de soldering. However, as well as being time consuming, this adds undue stress to the board as it is baked to remove moisture and then locally heated to attach the new processor.

As well as allowing for faulty processors to be replaced, a socket also allows for new revisions of the processor to be tested.

16.3 Socket Criteria

Numerous solutions exist in the market place for processor sockets. When choosing a socket, the following criteria were considered.

- Cost: With each motherboard requiring up to 4 sockets, cost was particularly sensitive.
- Size: Both in terms of height and width. An excessively tall socket could potentially foul on an adjacent board when Torridon is plugged into a rack environment. A wide socket would use up valuable real estate limiting the number of components that could be placed on the board.
- Board Attachment: Some sockets require special modifications to the board. For example additional fixing holes may be required. The addition of fixing holes will adversely impact the available board space for other components both on top and bottom of the board. Some sockets may require a “rear bracket” for board attachment and rigidity. This has the potential problem of fouling on adjacent boards in a rack environment or against the metal box in a chassis environment.

- Socket Foot Print: Ideally, the same foot print should be used for both the socket and the processor. Typically sockets are only used in the first few boards. Once the silicon is deemed stable, the sockets are no longer necessary and the processors can be mounted directly on the motherboard. This means that during assembly, either a socket or a processor may be populated. Alternatively, a board may be fitted with a socket during initial debug. This socket may then be removed, and potentially re-used, and a processor fitted in its place. Some sockets use a different foot print than the processor itself. Using such a socket will obviously not allow processors and sockets to be swapped in/out of boards. Using such a socket will dictate that two versions of the mother board be manufactured, a version to take sockets and a version to take processors.
- Heat Sink Attachment: Depending on the environment (e.g. ambient temperature, air flow etc.), it may be necessary to add a heat sink to the processor. Ideally the heat sink used with the socket should also be usable on the “bare processor”. This means only one type of heat sink is required. Again, this allows flexibility where, at the assembly stage, a board may be populated with or without sockets.

16.4 The Choice of a Socket

Based on the criteria detailed above, a socket solution from Emulation Technology was chosen. The socket had the following advantages.

- Low Cost (Approximately $300 each)
- Reliability: This socket technology has been used by many customers in numerous systems operating in various environments.
- Foot Print: The socket uses the same foot print as the silicon. This would allow a socketed and a non-socketed processor to be used on the same motherboard.
- Size: The socket is only 2mm wider and 2mm deeper than the processor itself.
- Height: The socket only adds 3mm to the overall height of the processor.
- Board Attachment: No board changes (e.g. fitting holes) are required to accommodate the socket
- Heat Sink: The socket does not impair the top or sides of the processor meaning the same heat sink may be used on a socketed and non-socketed processor.

16.5 Socket Mechanics

The socket solution is made up of two component parts.

1. The BPE (Base Package Emulator) is soldered to the motherboard. The BPE provides a 783 female connector into which a male socket can be inserted.

2. The processor itself is soldered onto an FPA (Flat Pin Array).The FPA provides the processor with pins which mate with the BPE. Effectively the FPA turns the processor from a BGA (Ball Grid Array) package to a PGA (Pin Grid Array) package

The diagram in Figure 16-1 shows how the component parts fit together.

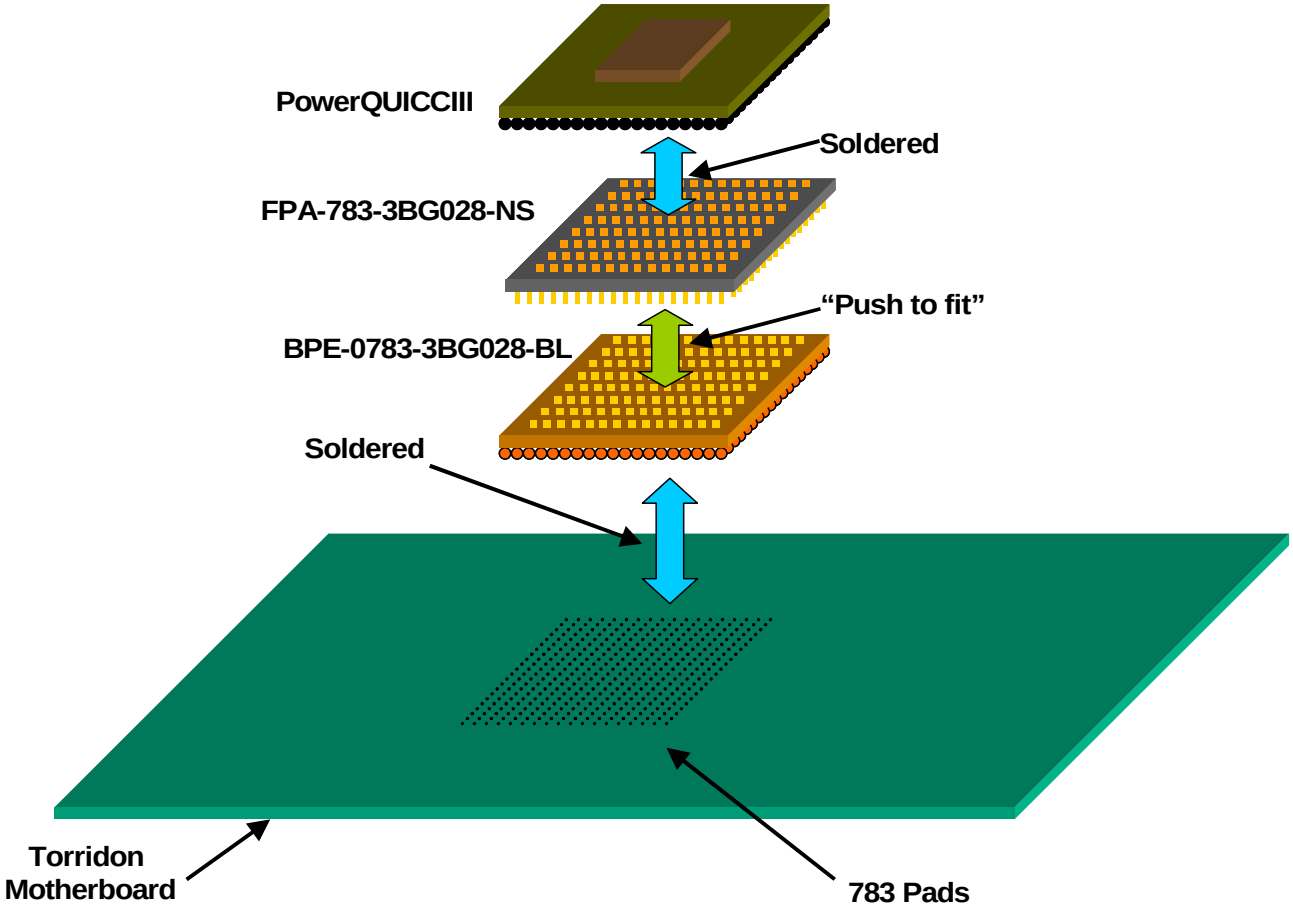


Figure 16-1. Socket Mechanics

The foot print of the BPE is identical to that of the PowerQUICCIII processor. This allows the BPE and the processor to be easily interchanged.

The diagram in Figure 16-2 illustrates how the processor and the socket may be inter-changed.

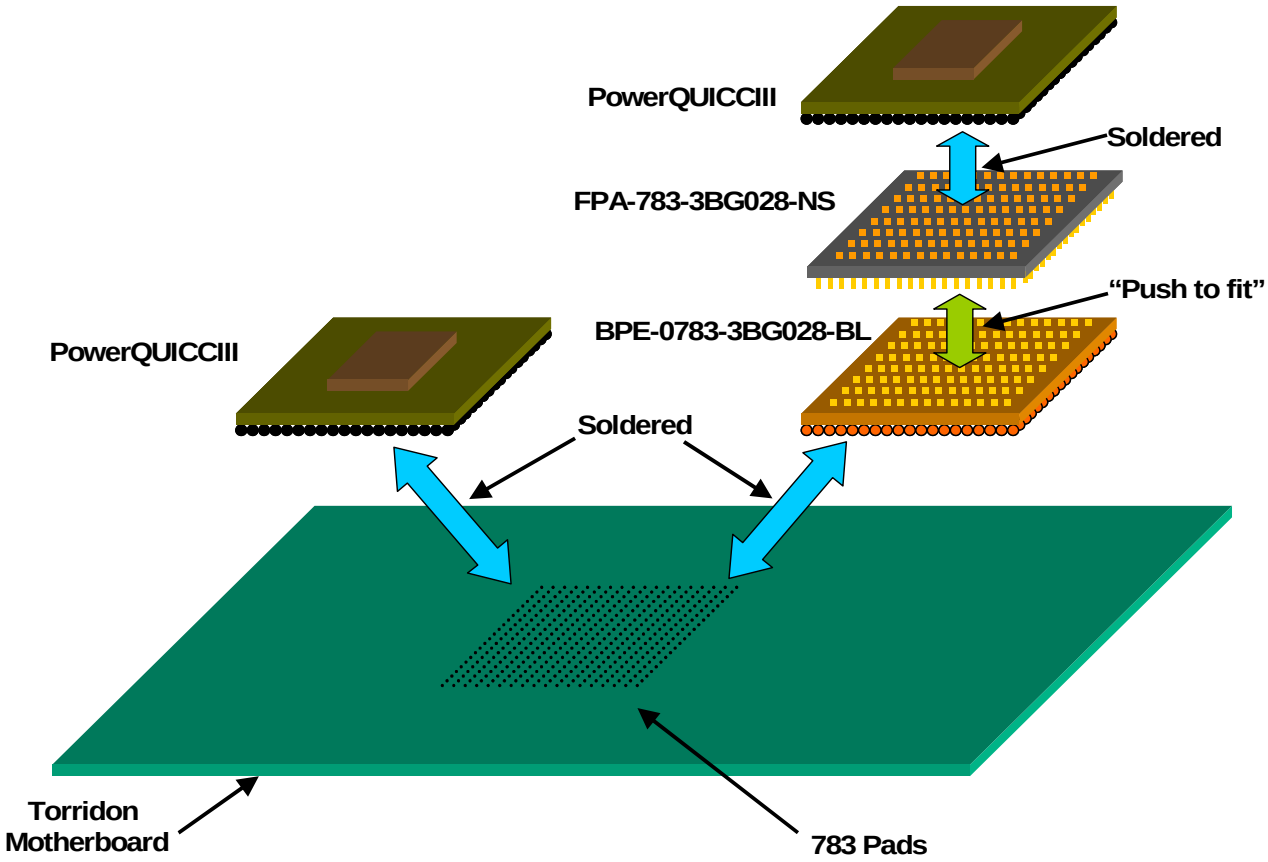


Figure 16-2. Processor - Socket Swapping

16.6 The Base Package Emulator (BPE)

The Base Package Emulator (BPE) is soldered directly onto the motherboard. 783 spheres present on the bottom of the BPE are used to attach it to the motherboard. The socket provides 783 female sockets on top. They accept the pins on the bottom of the FPA (Flat Pin Array) adapter. See Figure 16-3.

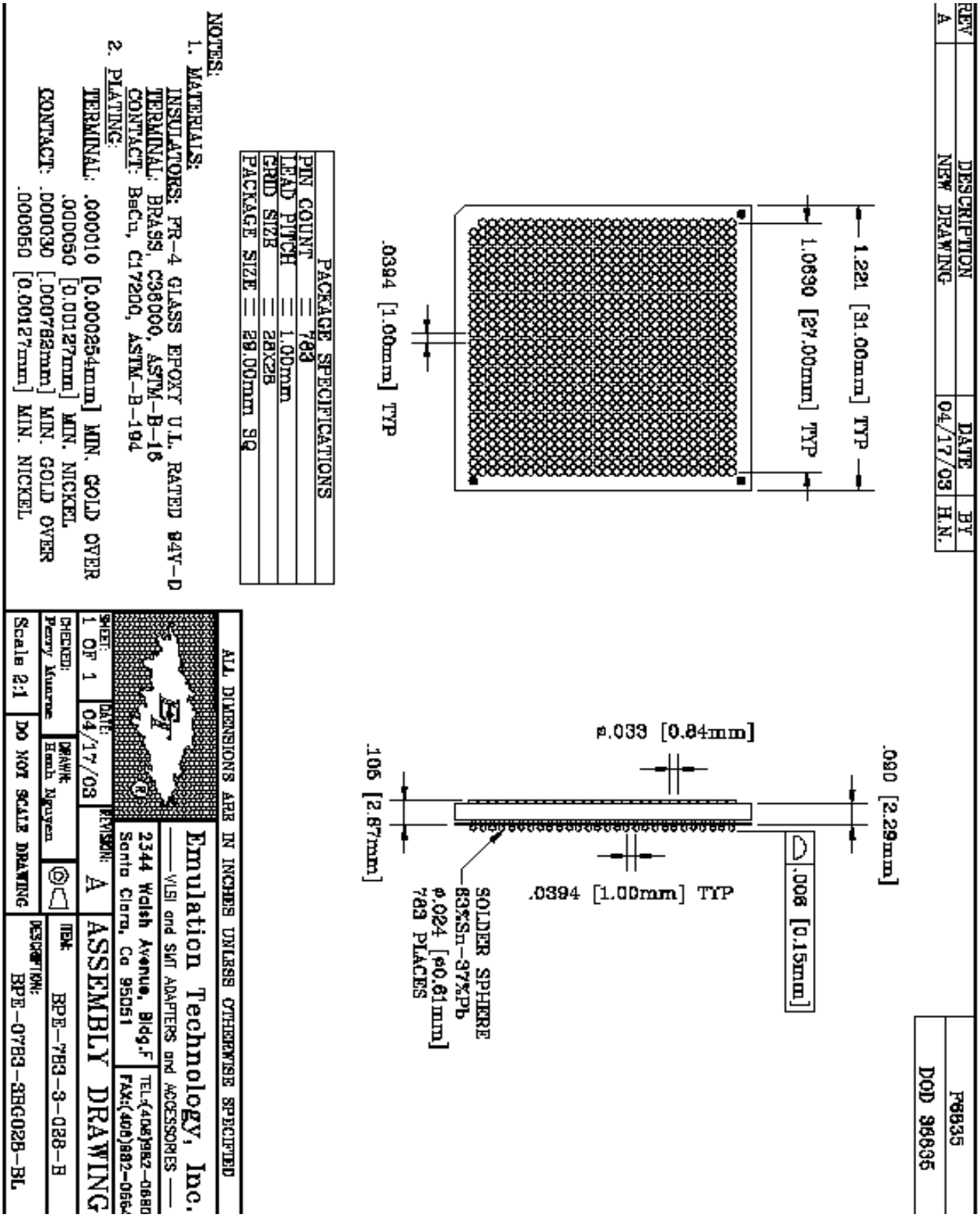


Figure 16-3. The BPE

16.7 The Flat Pin Array (FPA)

The Flat Pin Array (FPA) adapter allows the processor to mate with the BPE. 783 pads are present on top of the FPA. The PowerQUICCIII is soldered directly on to these pads. The bottom of the adapter provides pins which fit directly into the BPE. See Figure 16-4.

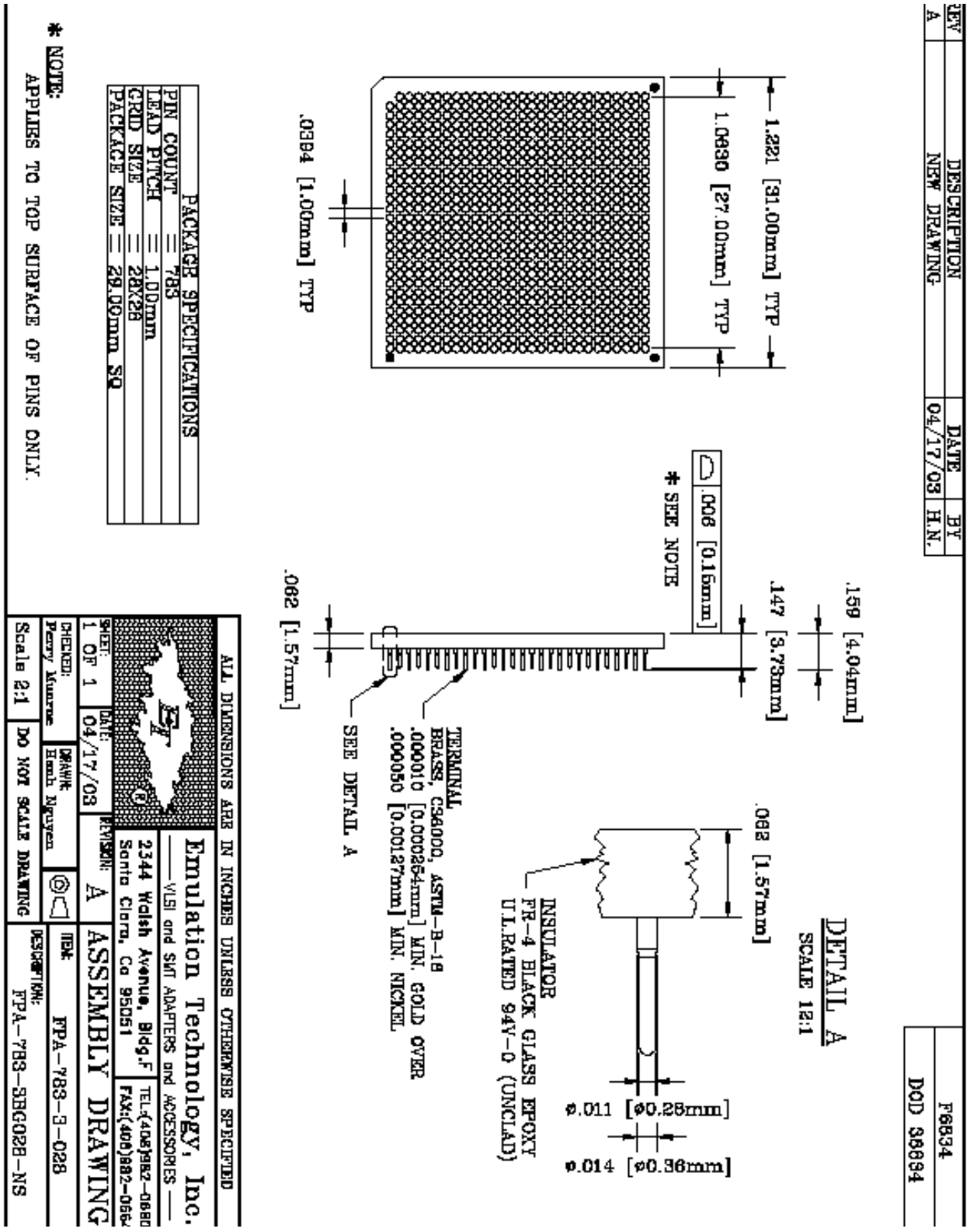


Figure 16-4. The FPA

16.8 Alternative Parts

Although Torridon used the parts from Emulation Technology, similar socket are available from other companies. Table 16-1 provides alternative sockets that may be used.

Table 16-1. Alternative Socket Vendors

Component Part	Vendor	Part Number
BPE	Emulation Technology	BPE-0783-3BG028-BL
BPE	Advanced Interconnect	FHA783-715G
FPA	Emulation Technology	FPA-783-3BG028-NS
FPA	Advanced Interconnect	FHS783-715-GG

16.9 Sockets on Torridon

The following pictures show the sockets on the Torridon motherboard: Table 16-5, Table 16-6, Table 16-7, Table 16-8, and Table 16-9.

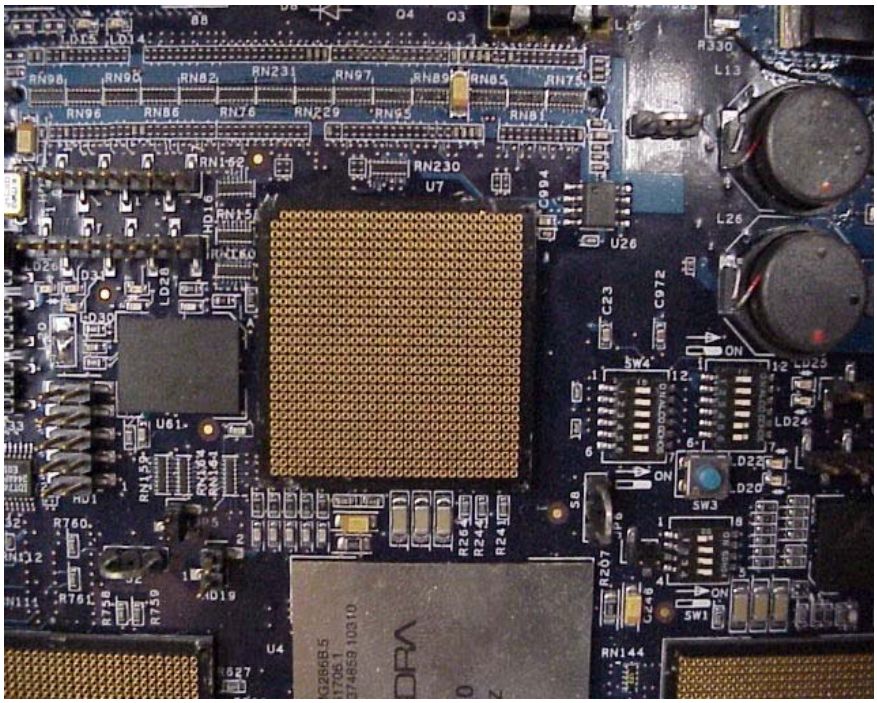


Figure 16-5. BPE

Figure 16-6. PowerQUICCIII in FPA

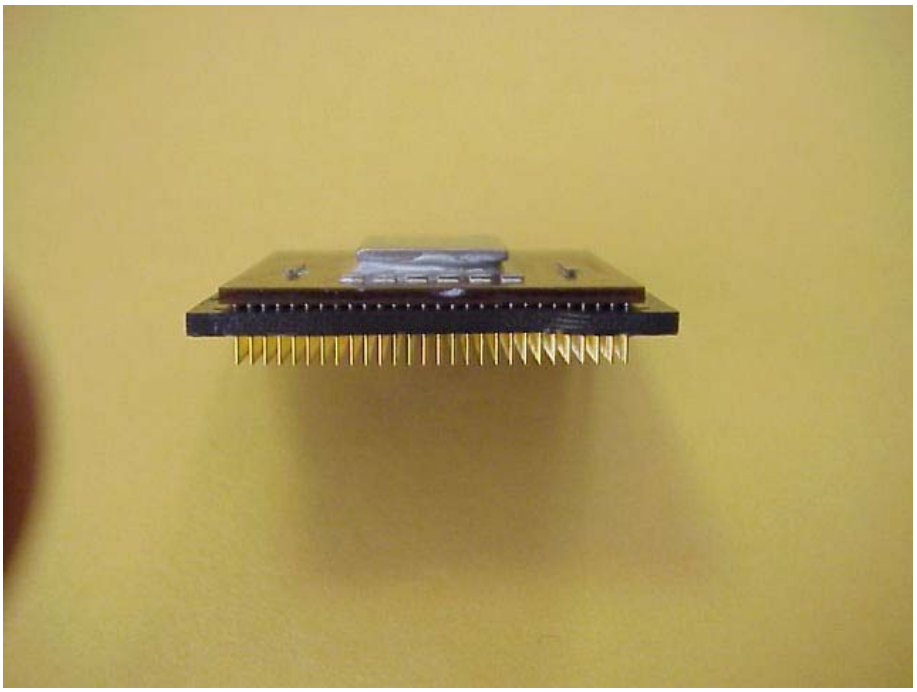


Figure 16-7. PowerQUICCIII in FPA - Side View

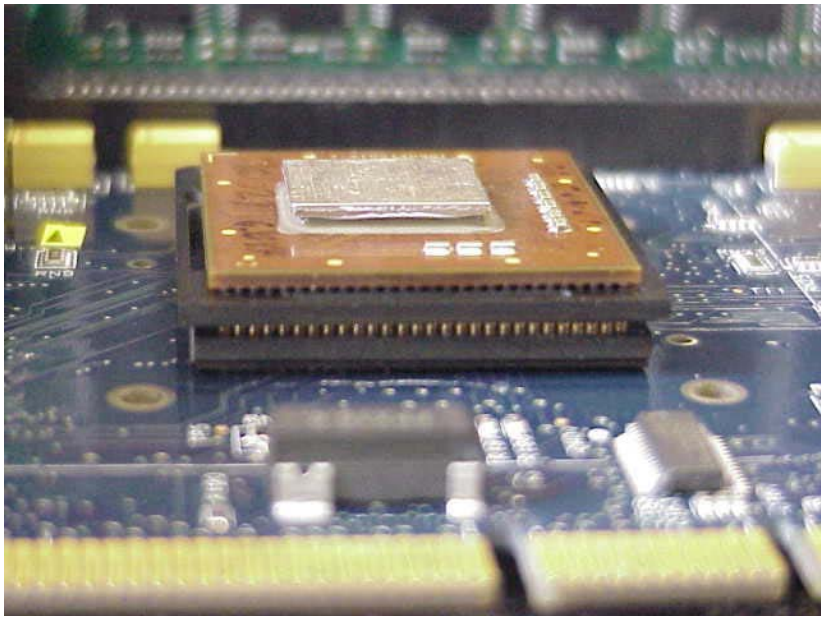


Figure 16-8. PowerQUICCIII + FPA + BPE

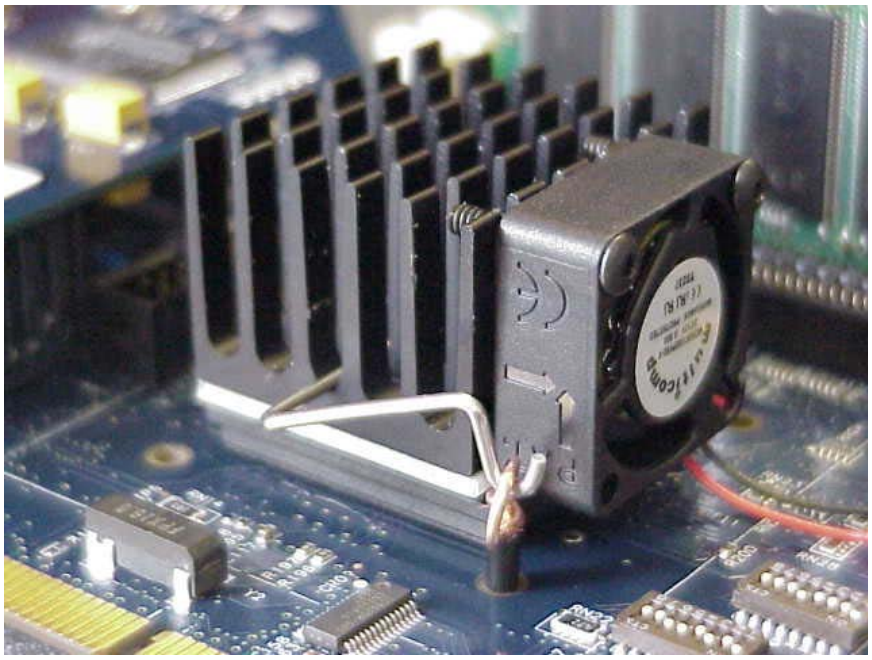


Figure 16-9. Heat Sink Attached

Chapter 17 Heat Sinks

This section describes the Heat Sinks used on the Torridon Motherboard.

17.1 Overview

The processors on Torridon are each fitted with a heat sink. The choice of size and type of heat sink is dependant on the environment in which the board is situated. Factors such as processor speed, ambient temperature and air flow all dictate the specific characteristics of the heat sink used.

17.2 Processor Thermal Characteristics

Table 17-1 details the package thermal characteristics for the MPC8560 processor.

Table 17-1. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient resistance (Natural convection on 1S board)	θ_{JA}	30	°C/W	1,2
Junction-to-ambient resistance (Natural convection on 2S2P board)	θ_{JMA}	19	°C/W	1,3
Junction-to-ambient resistance (Forced airflow (200 ft/min) on 1S board)	θ_{JMA}	24	°C/W	1,3
Junction-to-ambient resistance (Forced airflow (200 ft/min) on 2S2P board)	θ_{JMA}	16	°C/W	1,3
Die junction-to-board thermal resistance	θ_{JB}	10	°C/W	4
Junction-to-case thermal resistance	θ_{JC}	0.3	°C/W	5

1 Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.

3 Per JEDEC JESD51-6 with the board horizontal.

4 Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface without thermal grease.

17.3 Thermal Management Information

Proper thermal control design is primarily dependent upon the system-level design i.e. the heat sink, airflow and thermal interface material. The recommended attachment method to the heat sink is illustrated in Figure 17-1. The heat sink should be attached to the printed circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force.

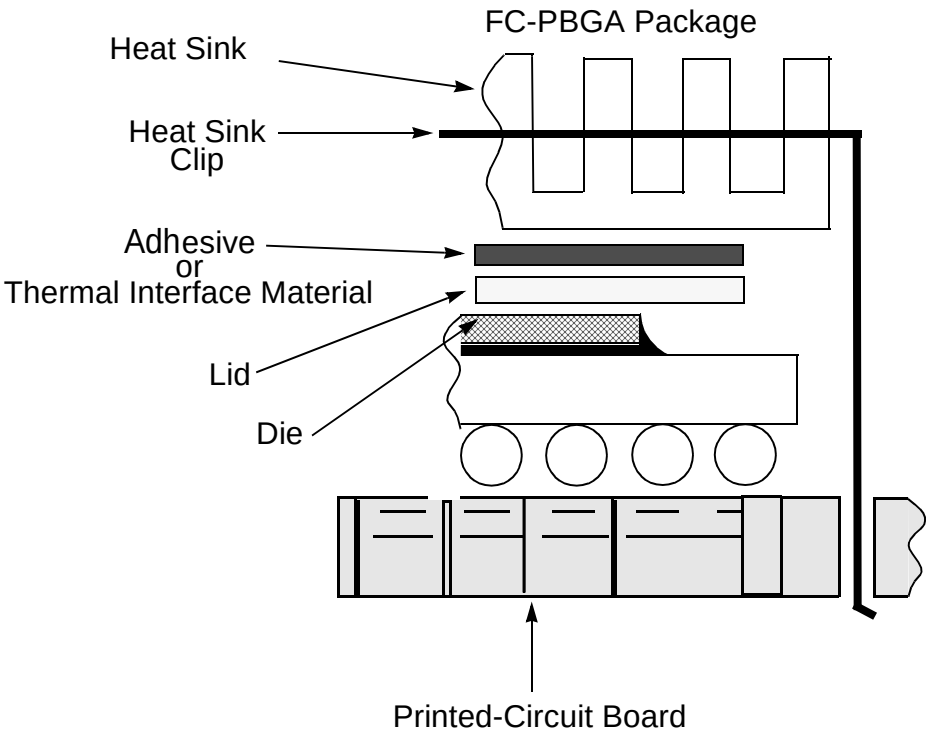


Figure 17-1. Heat Sink Attachment

17.4 Adhesives and Thermal Interface Materials

A thermal interface material is required at the package-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, the diagram in Figure 17-2 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. The bare joint results in a thermal resistance approximately six times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the PCB. Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

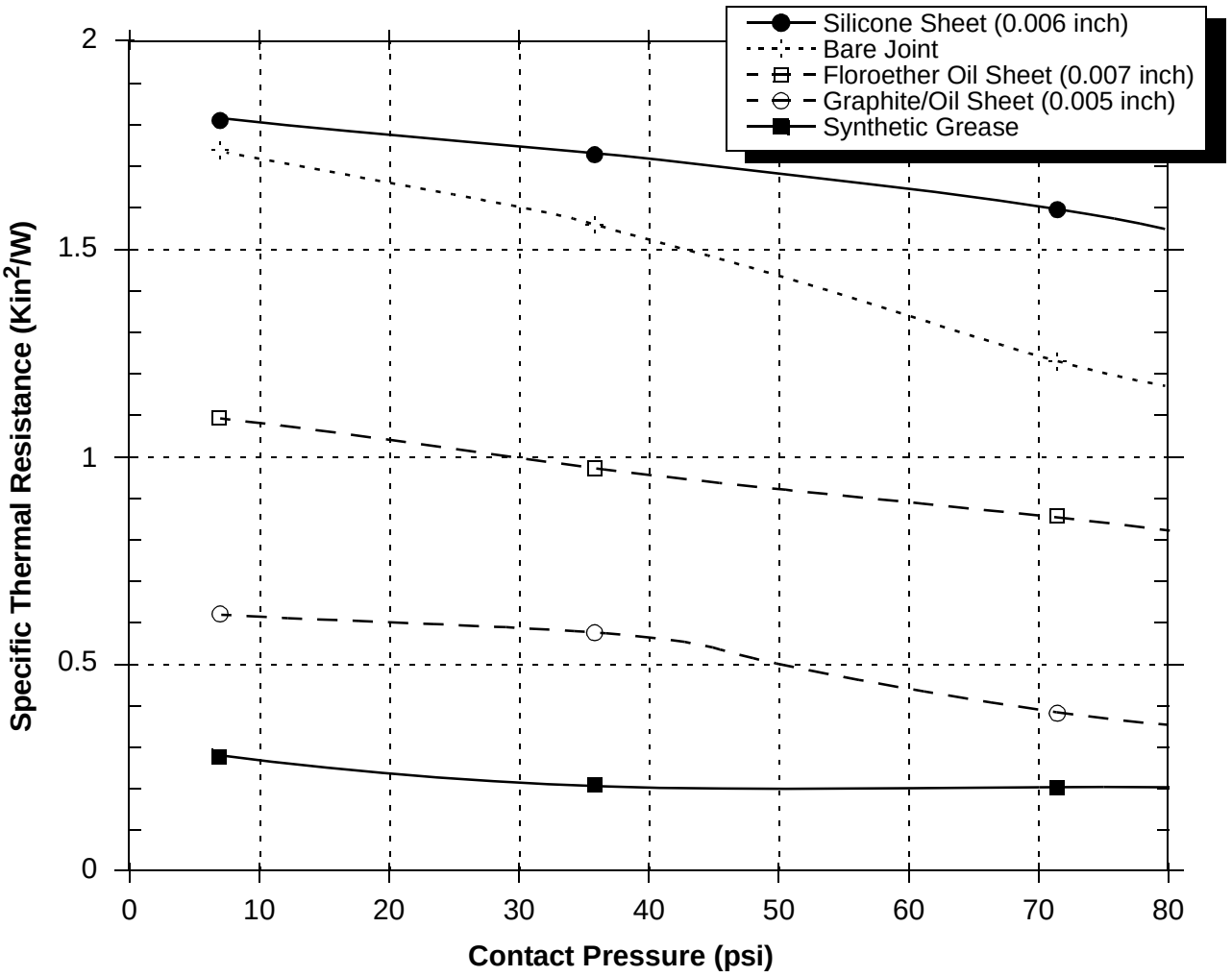


Figure 17-2. Thermal Performance of Interface Material

17.5 Heat Sink Selection

The choice of the heat sink is dependant on a number of factors such as the space available, the air flow across the heat sink and the availability of a fan. This will be ultimately be determined by the mechanical constraints of a system.

For preliminary heat sink sizing, the die junction temperature can be expressed as

$T_j = T_i + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) \times P_d$

Where:

T_j is the die-junction temperature
T_i is the inlet cabinet ambient temperature
T_r is the air temperature rise within the computer cabinet
θ_{jc} is the junction-to-case thermal resistance
θ_{int} is the adhesive or interface material thermal resistance
θ_{sa} is the heat sink base-to-ambient thermal resistance
P_d is the power dissipated by the device

During operation the die-junction temperatures (T_j) should be maintained within the specified range of 0 - 105°C.

The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30° to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5° to 10°C. The thermal resistance of some thermal interface material (θ_{int}) may be about 1°C/W. Assuming a T_i of 30°C, a T_r of 5°C, a FC-PBGA package θ_{jc} = 0.3, and a power consumption (P_d) of 7.0 W, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.3°C/W + 1.0°C/W + \theta_{sa}) * 7.0\ W$

The heat sink-to-ambient thermal resistance (θ_{sa}) versus airflow velocity for a Aavid Thermalloy heat sink 10-THMA-01 is shown in the diagram in Figure 17-3.

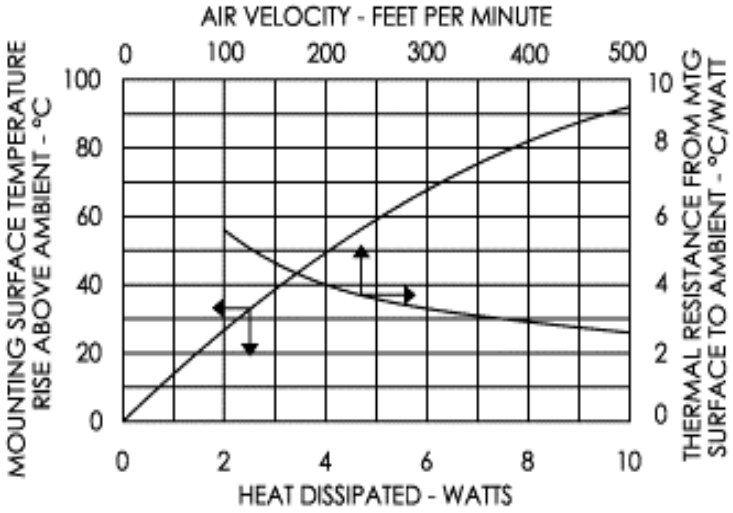


Figure 17-3. Aavid Thermalloy 10-THMA-01 Thermal Characteristics

Assuming an air velocity of 1m/s.

1m/s is equal to 200 LFM. (Linear Feet per minute)

From the graph above, this will equate to an effective θ_{sa} of about 4°C/W, thus

T_j = 30°C + 5°C + (0.3°C/W +1.0°C/W + 4°C/W) x 7.0 W,

resulting in a die-junction temperature of approximately 72.1°C which is well within the maximum operating temperature of the component.

The diagram in Figure 17-4 shows the physical dimensions of the Aavid Thermalloy 10-THMA-01.

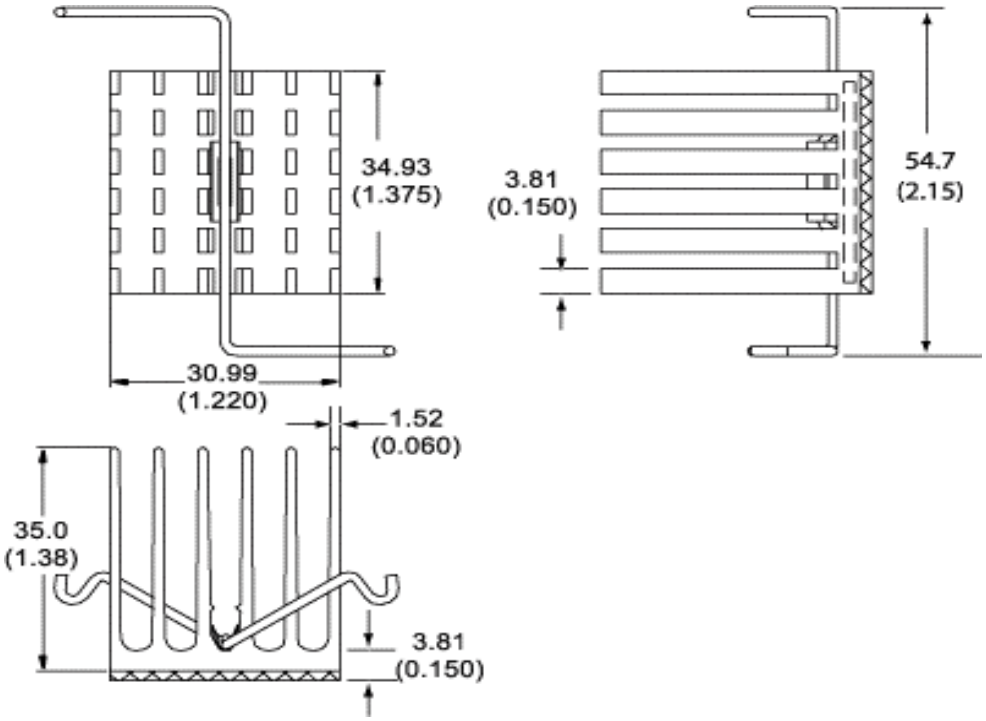


Figure 17-4. Aavid Thermalloy 10-THMA-01 Dimensions

17.6 Fans

To aid in thermal dissipation, each heat sink is fitted with a fan. Running off a 12V supply, the 25mm x 25mm x 10mm fan is capable of providing an air flow of 1m/s.

17.7 Heat Sinks On Torridon

The photo in Figure 17-5 shows a heat sink on Torridon fitted with a fan.

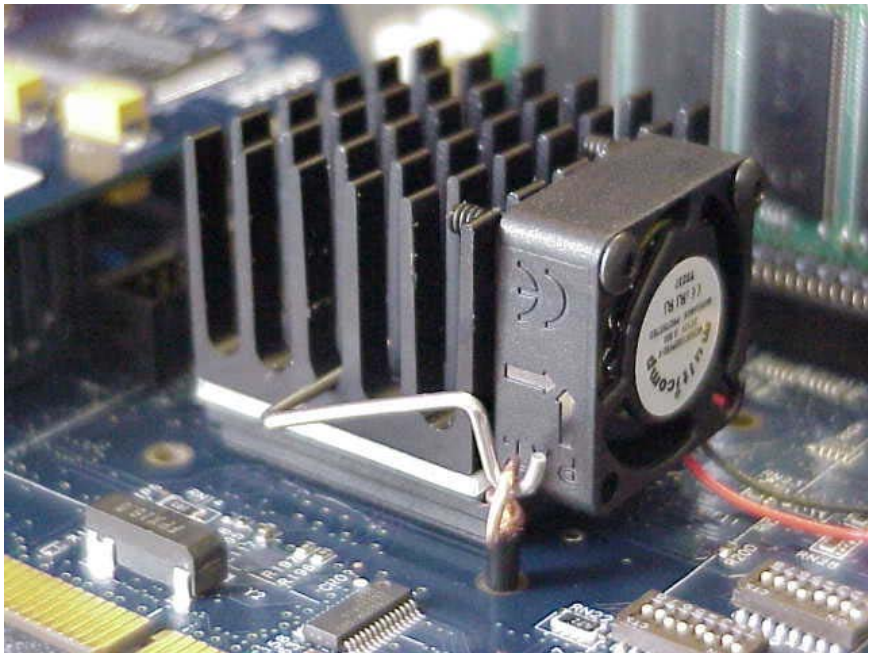


Figure 17-5. Heat Sink on Torridon

Appendix A
Schematics

The schematics for Torridon are shown on the following pages.

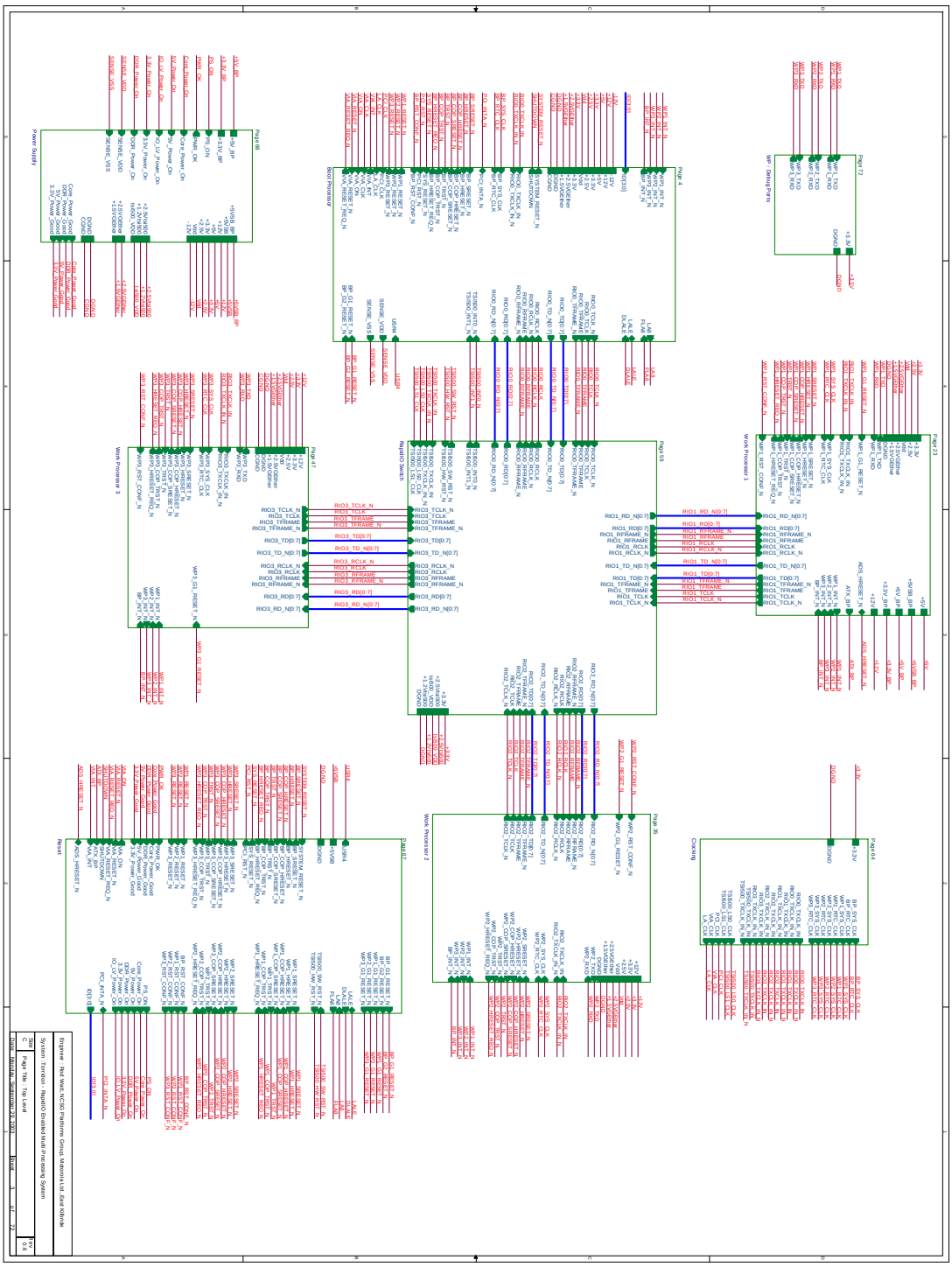


Figure A-1. Top Level

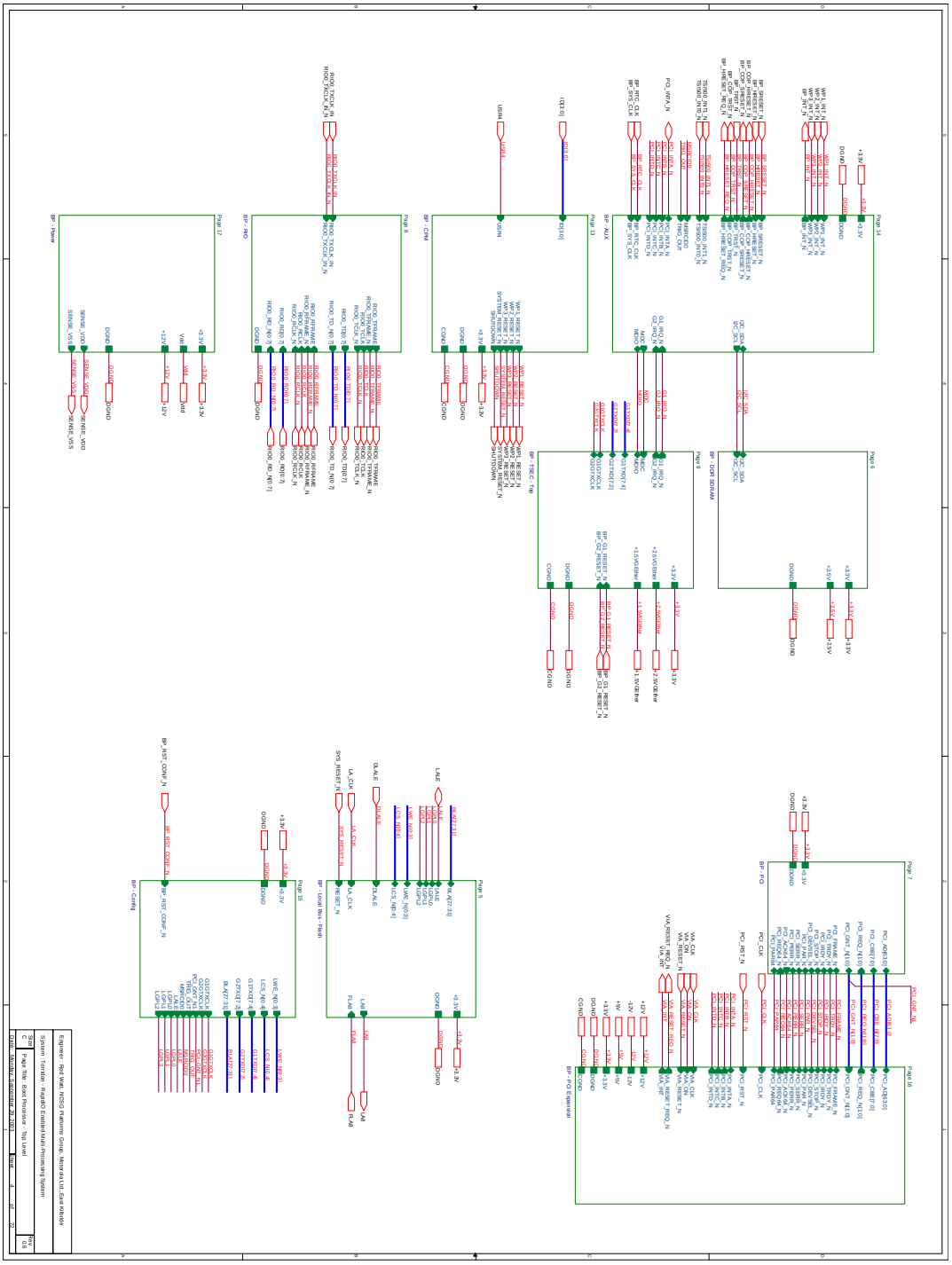


Figure A-2. Boot Processor—Top Level

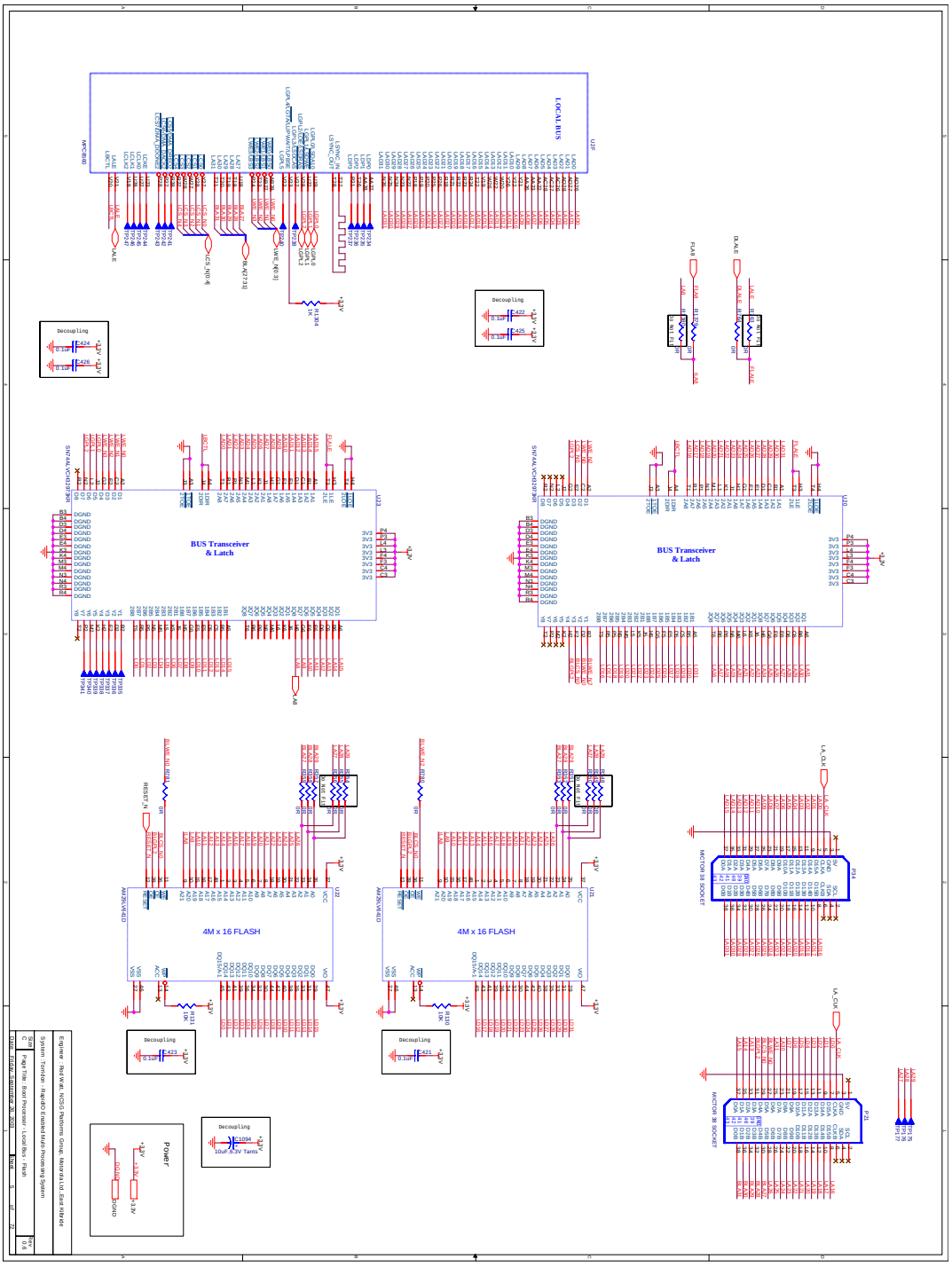


Figure A-3. Boot Processor—Local Bus—Flash

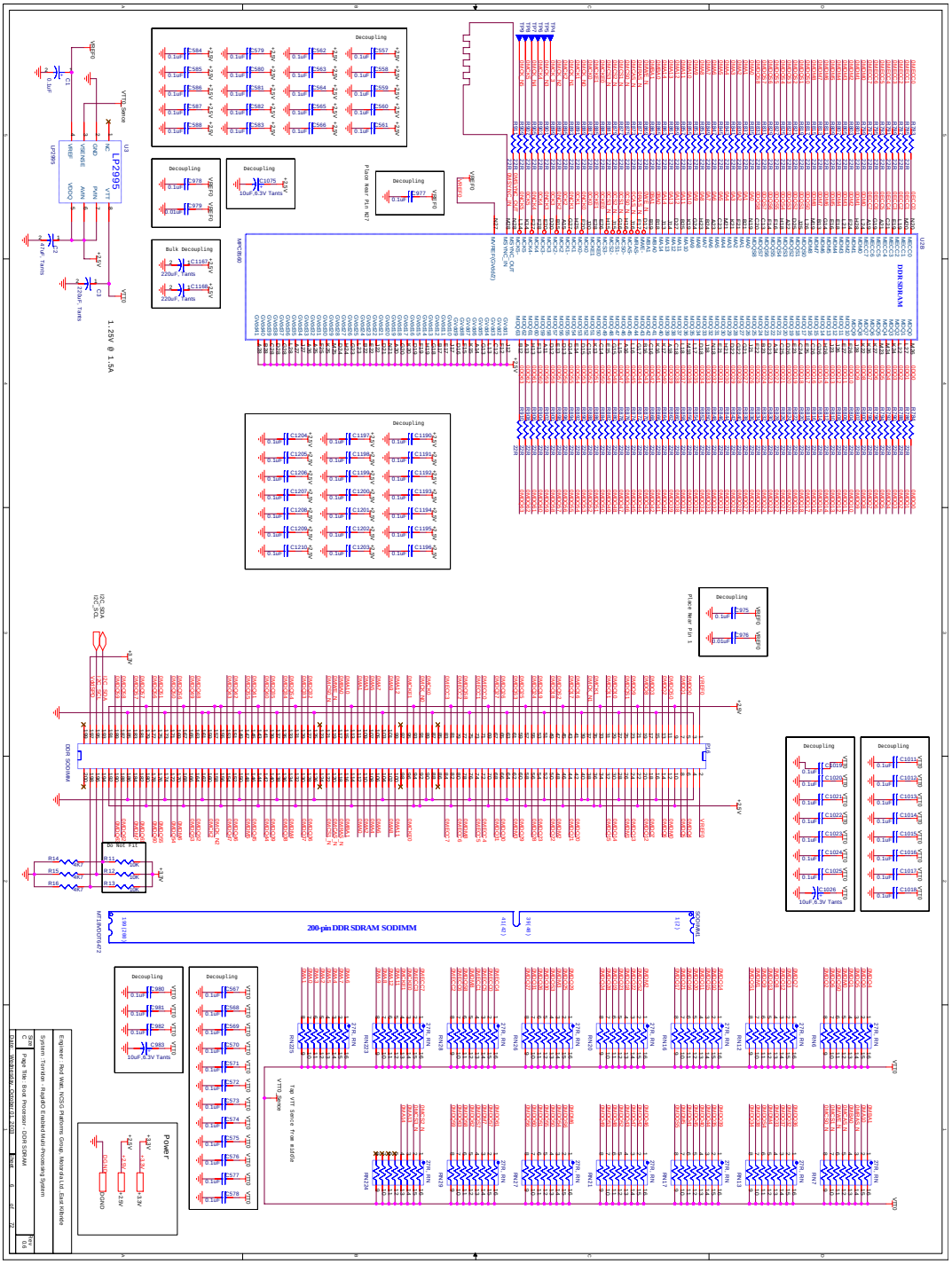


Figure A-4. Boot Processor—DDR SDRAM

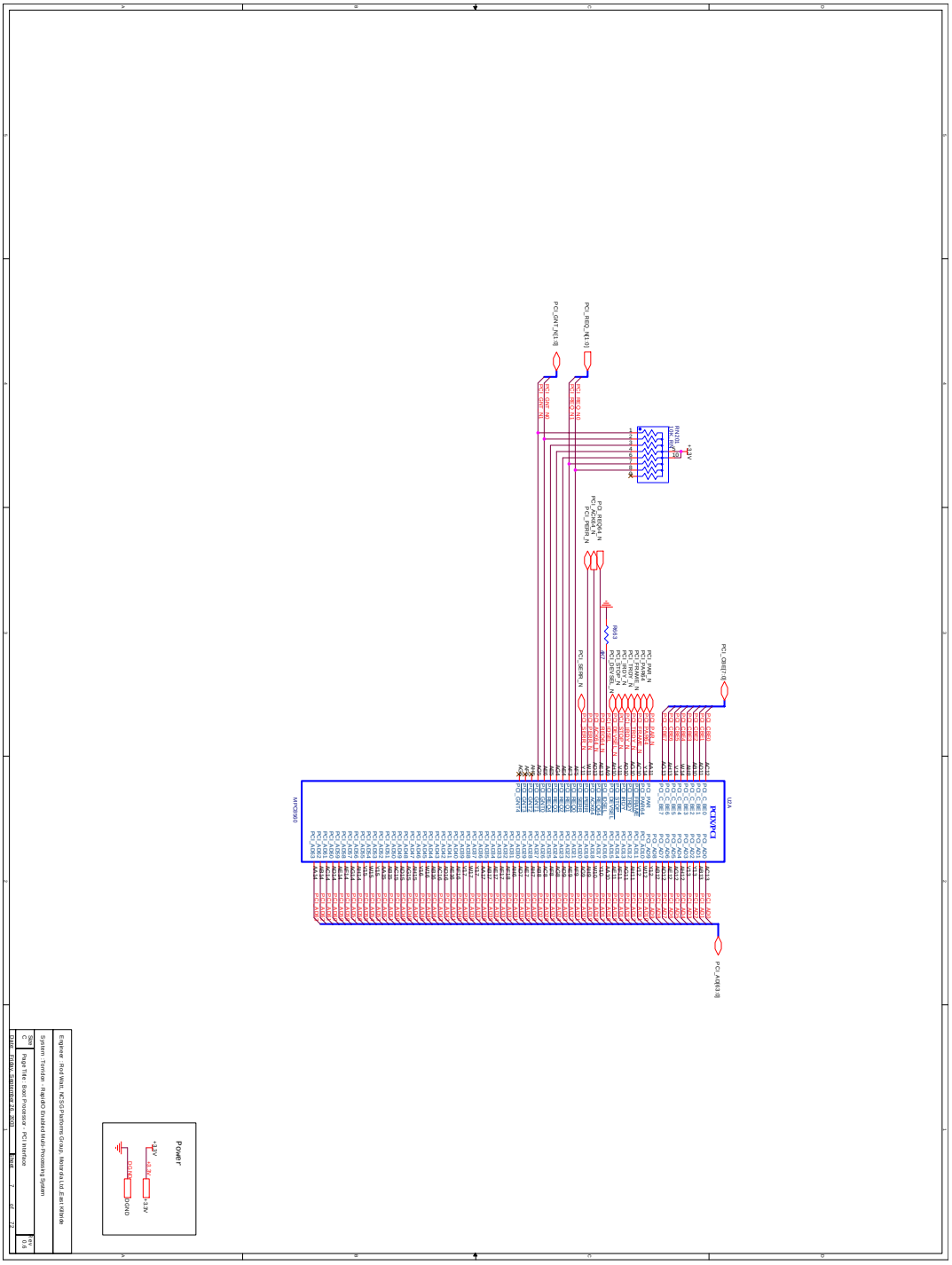


Figure A-5. Boot Processor—PCI Interface

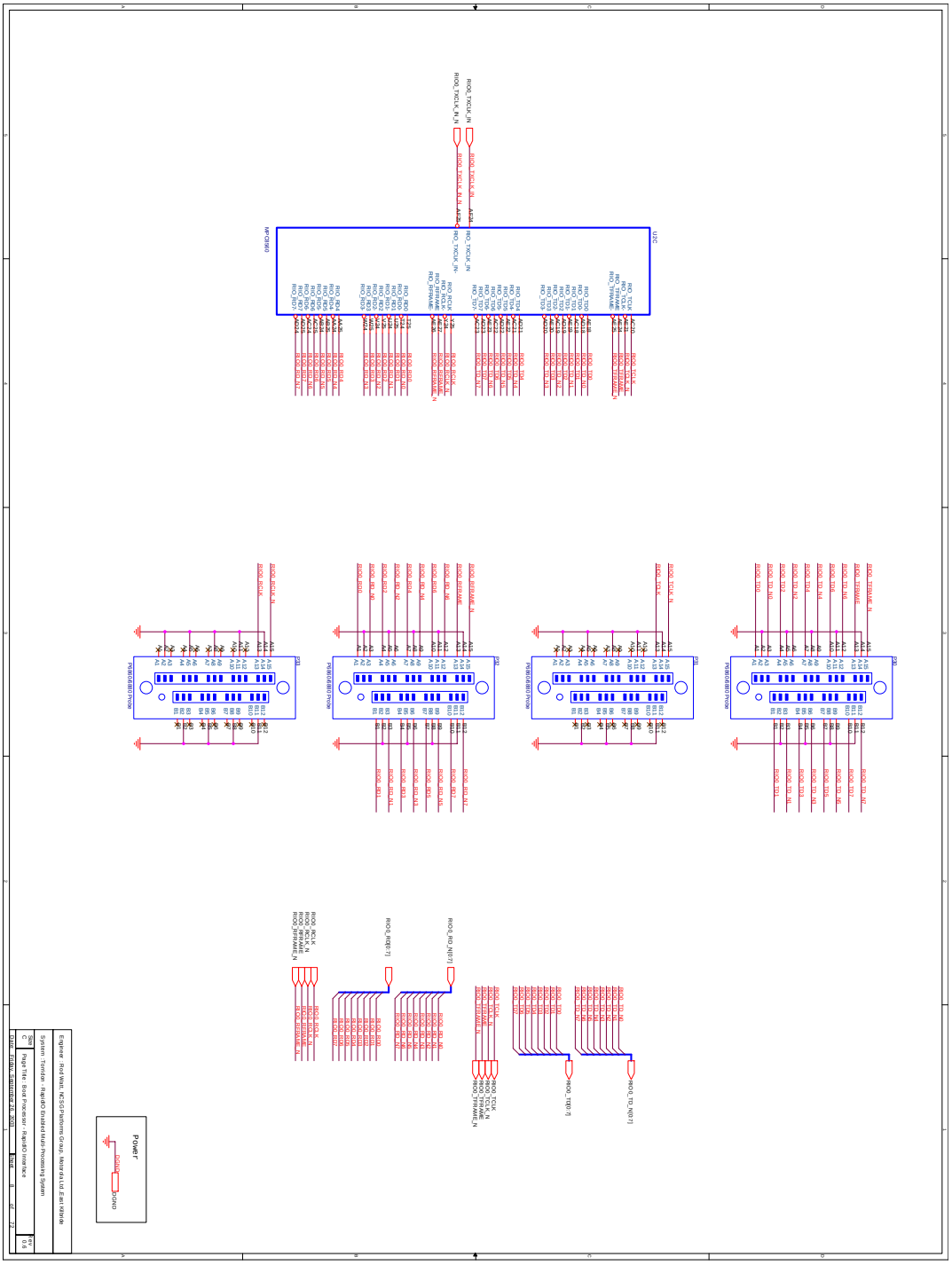


Figure A-6. Boot Processor—RapidIO Interface

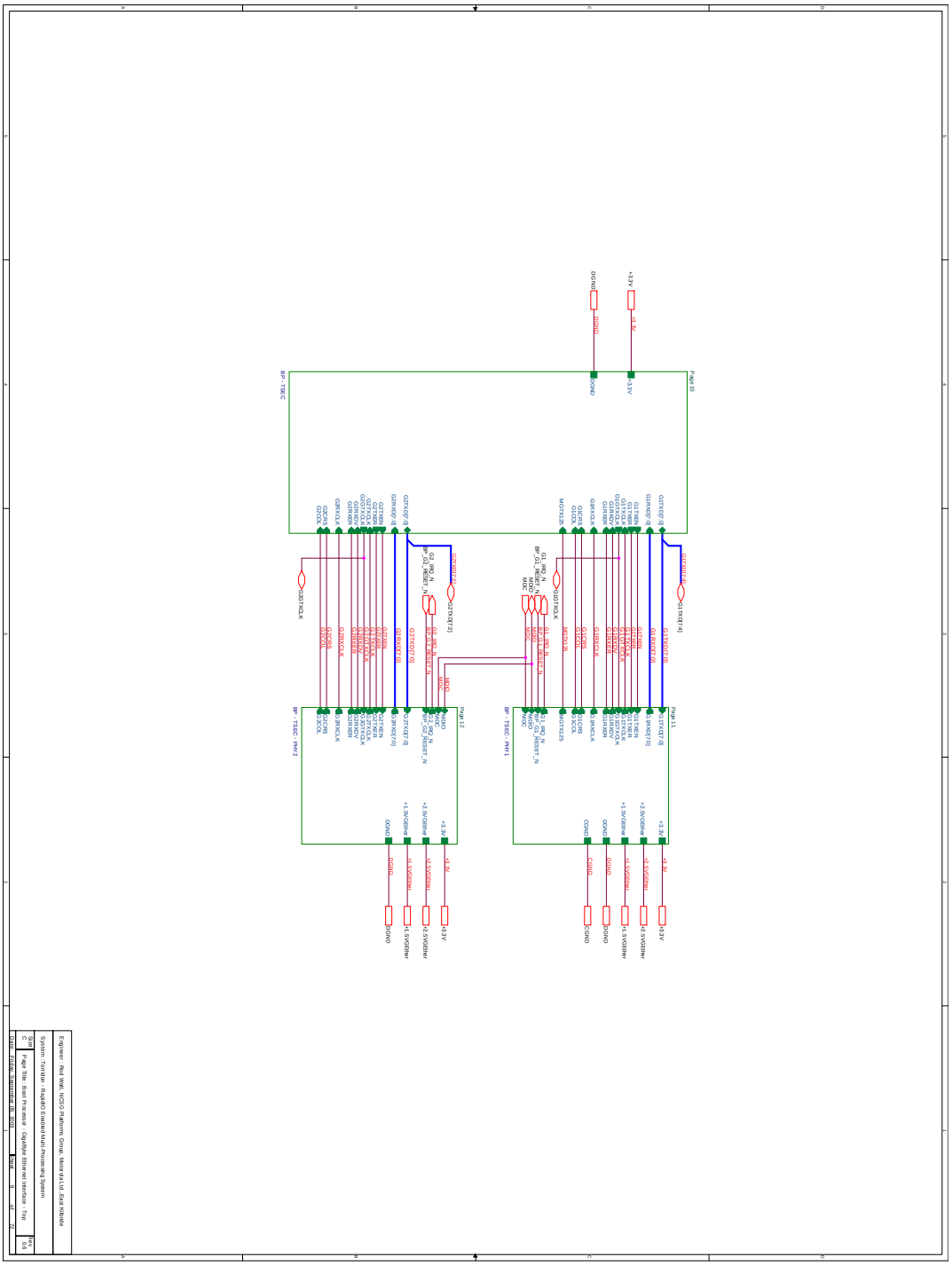


Figure A-7. Boot Processor—GigaByte Ethernet Interface—Top

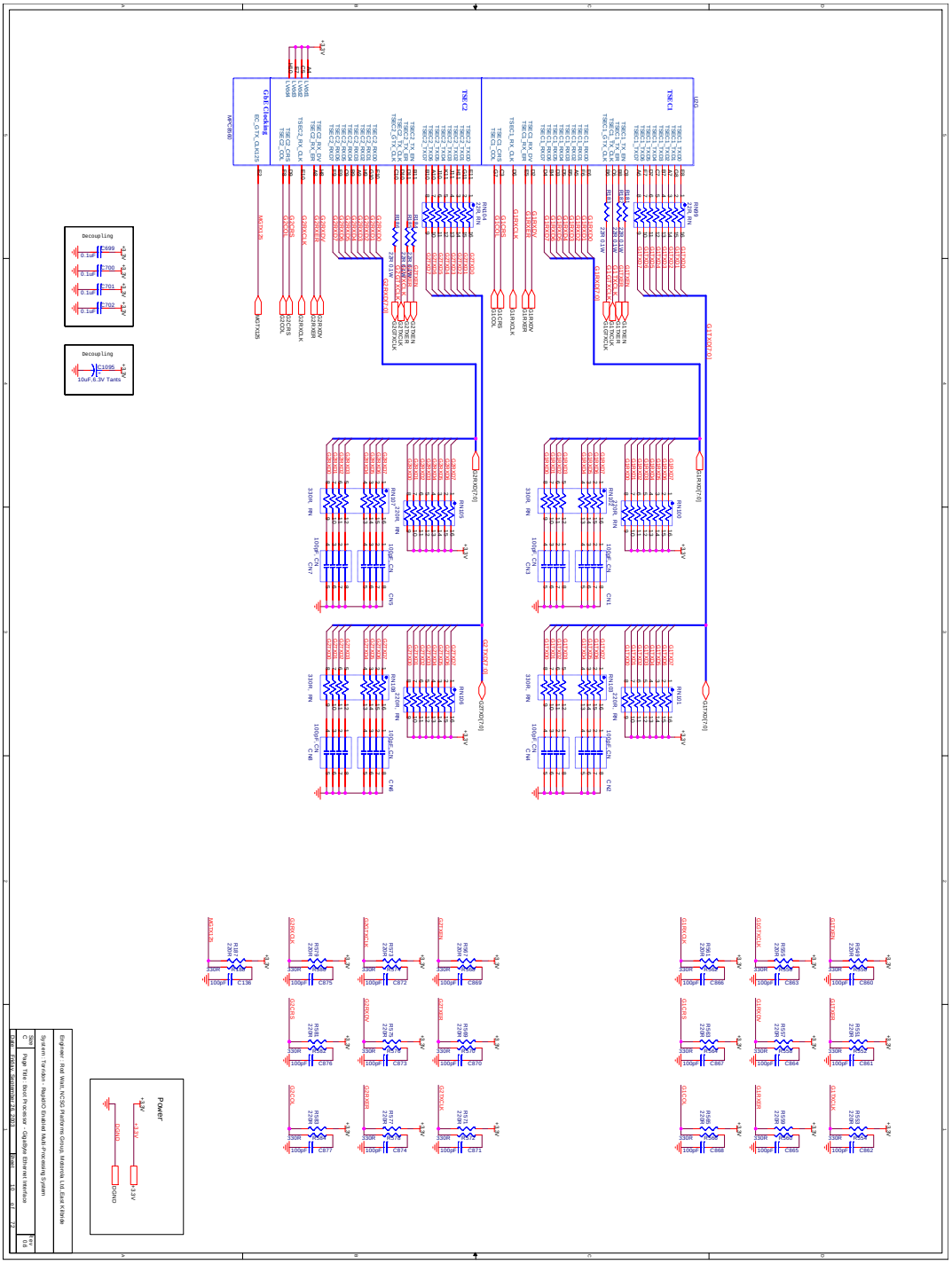


Figure A-8. Boot Processor—GigaByte Ethernet Interface

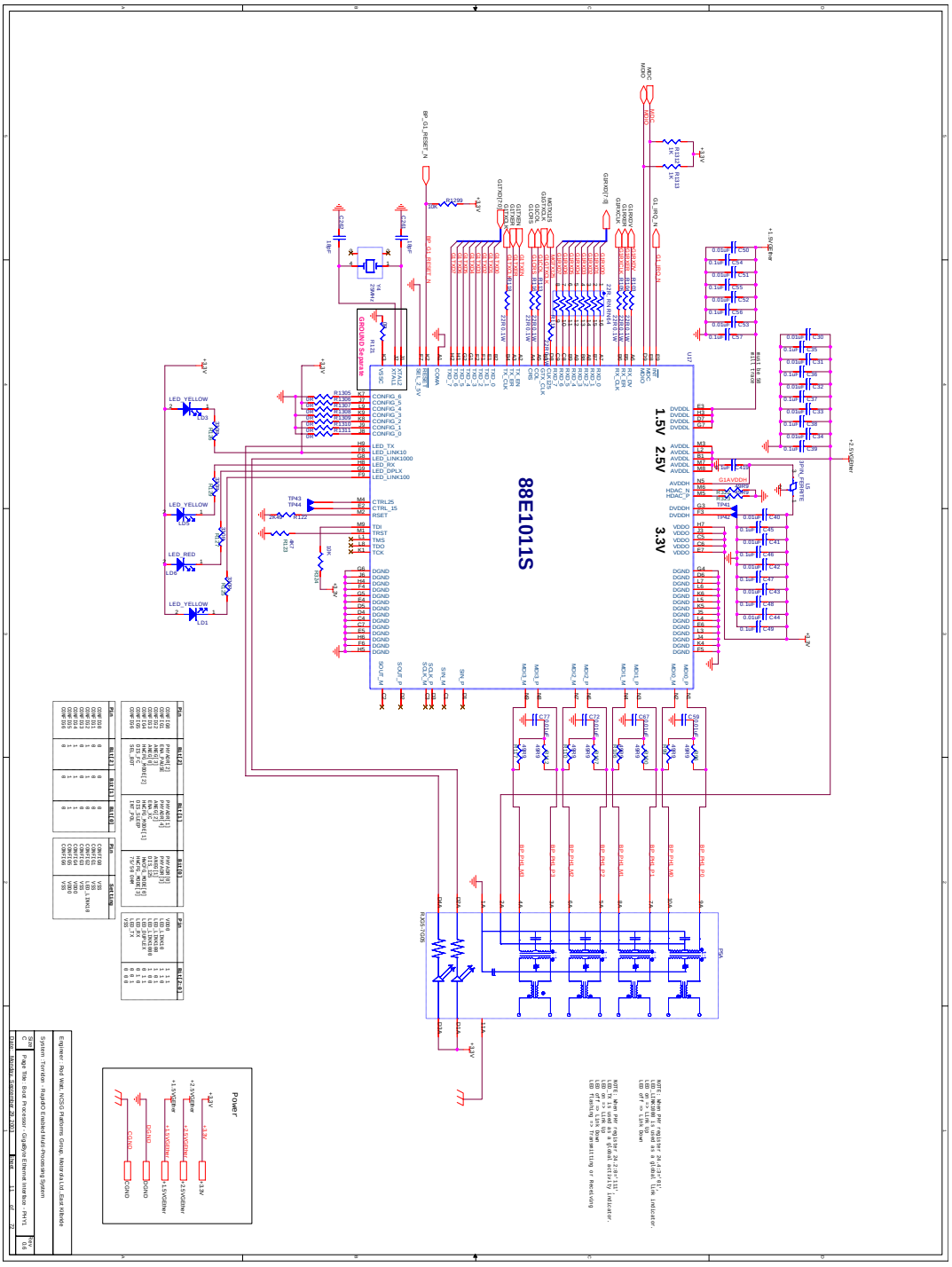


Figure A-9. Boot Processor—GigaByte Ethernet Interface—PHY1

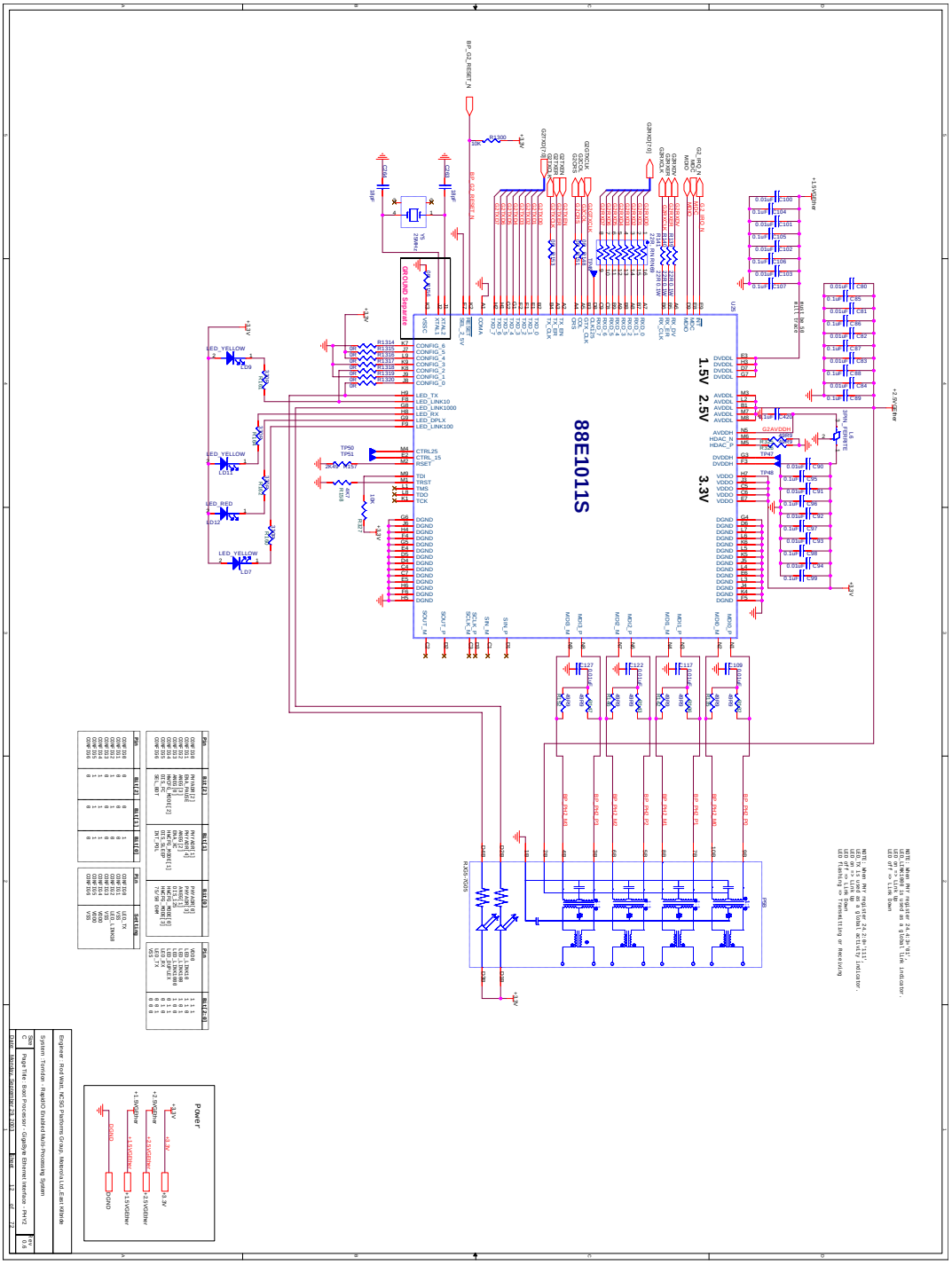


Figure A-10. Boot Processor—GigaByte Ethernet Interface—PHY2

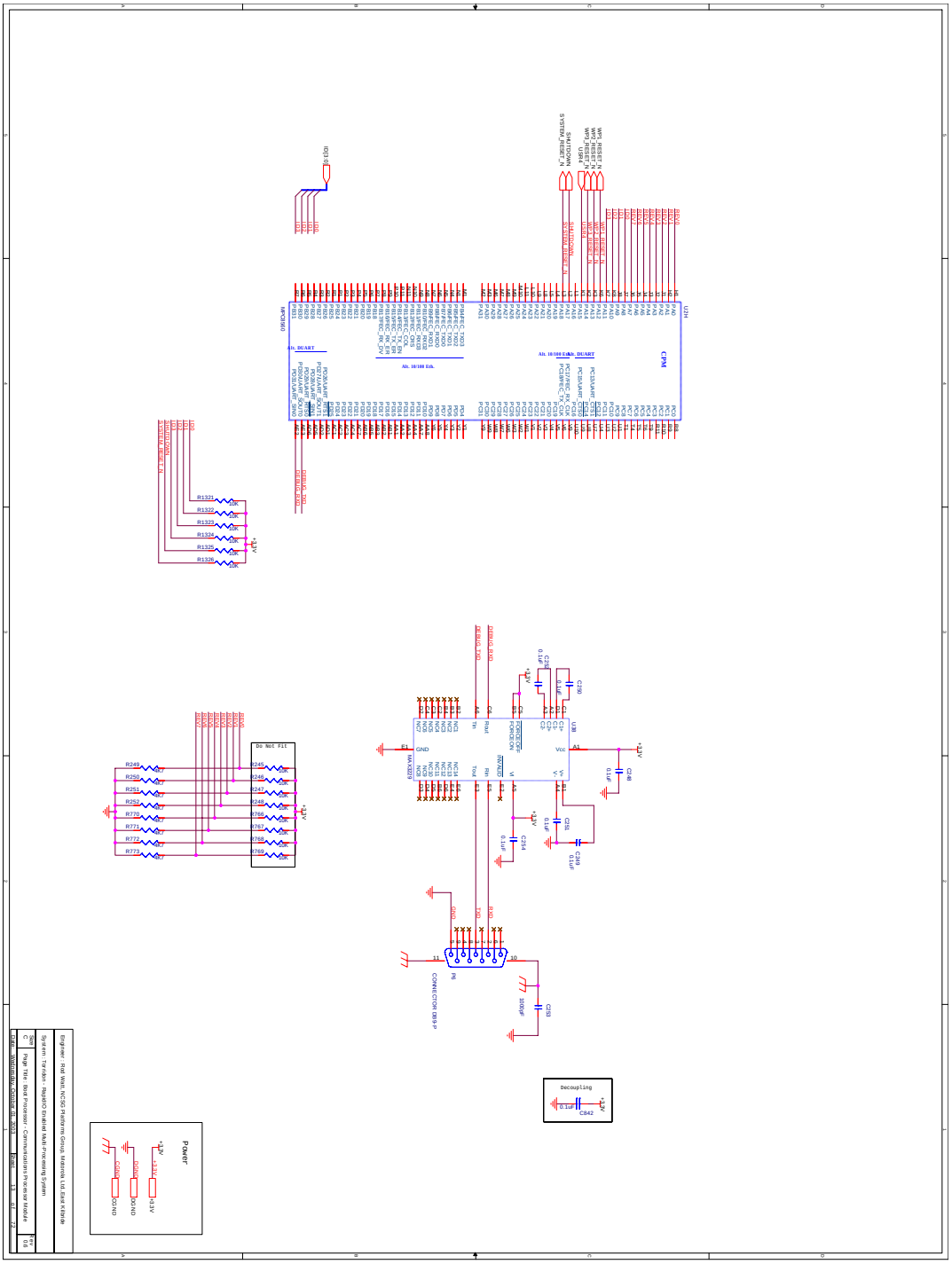


Figure A-11. Boot Processor—Communications Processor Module

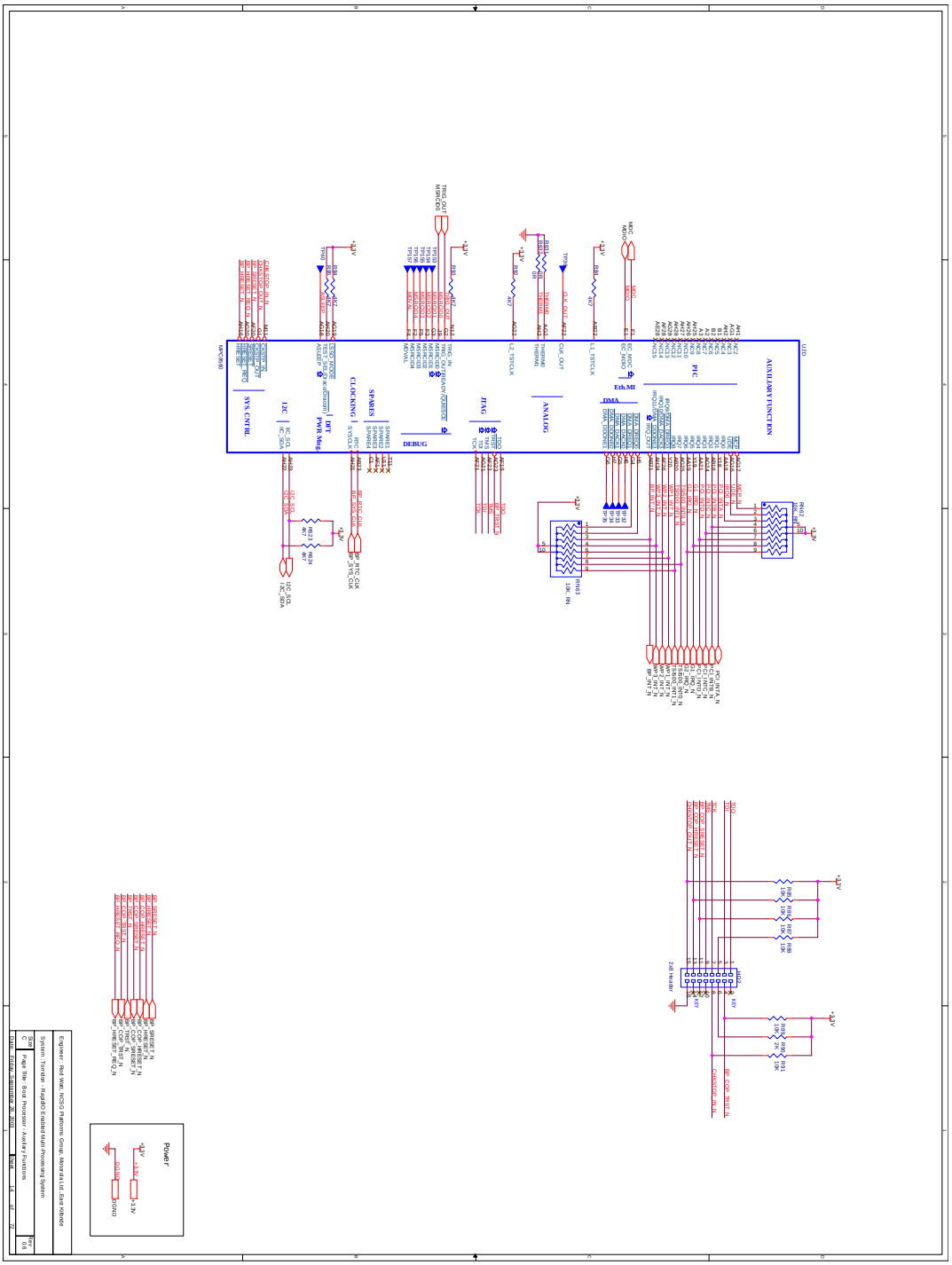


Figure A-12. Boot Processor—Auxiliary Functions

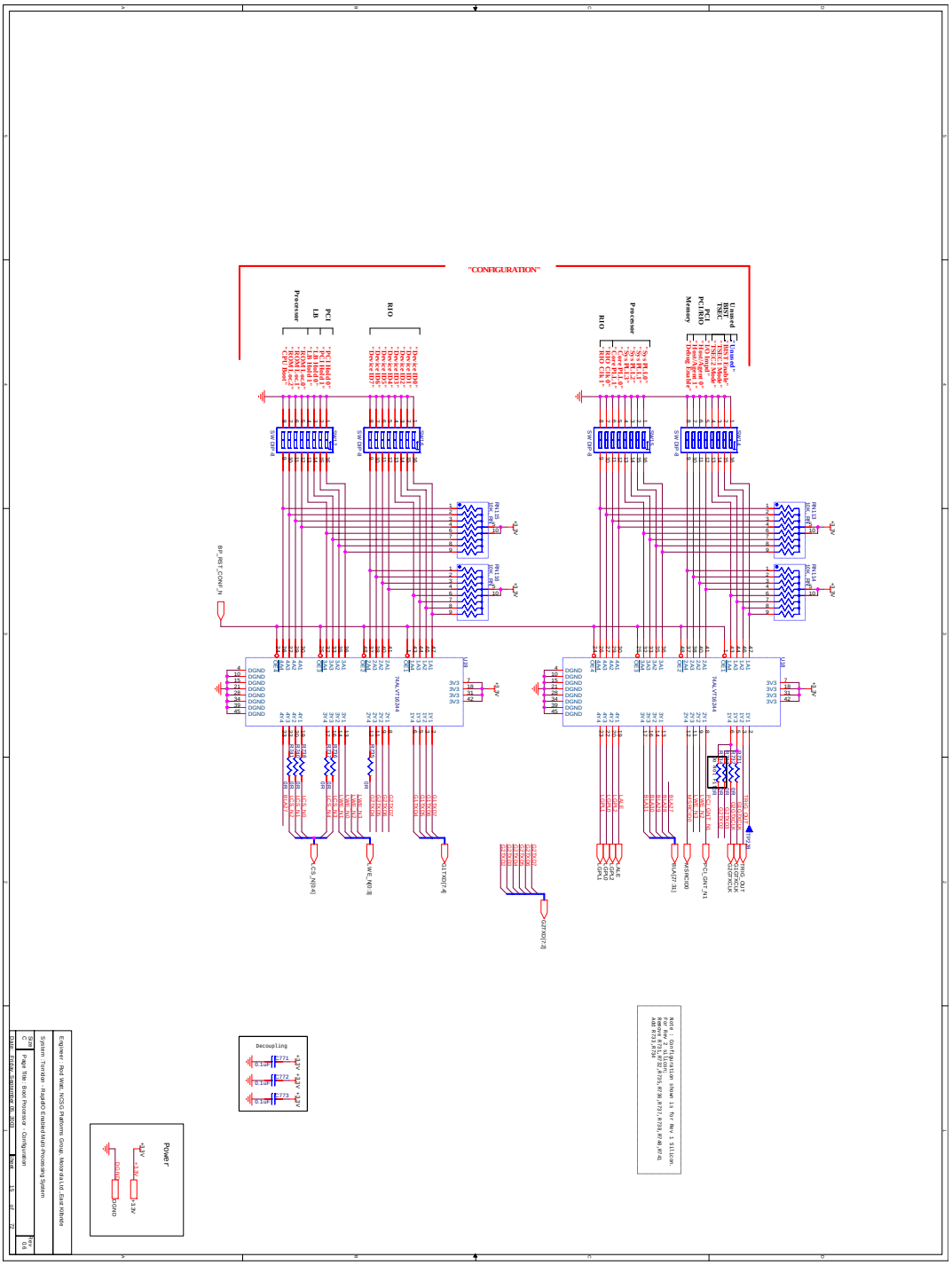


Figure A-13. Boot Processor—Power On Configuration

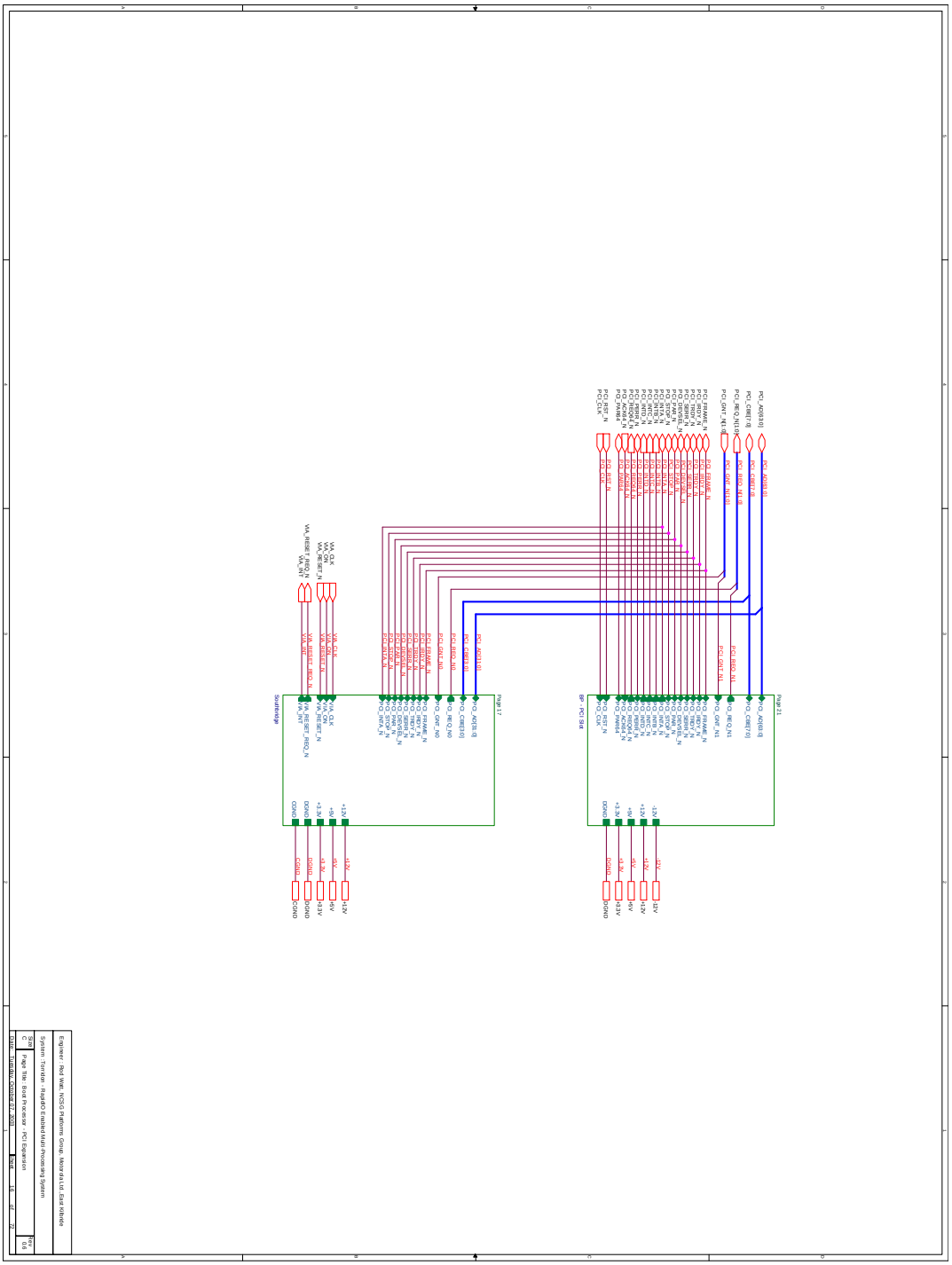


Figure A-14. Boot Processor—PCI Expansion

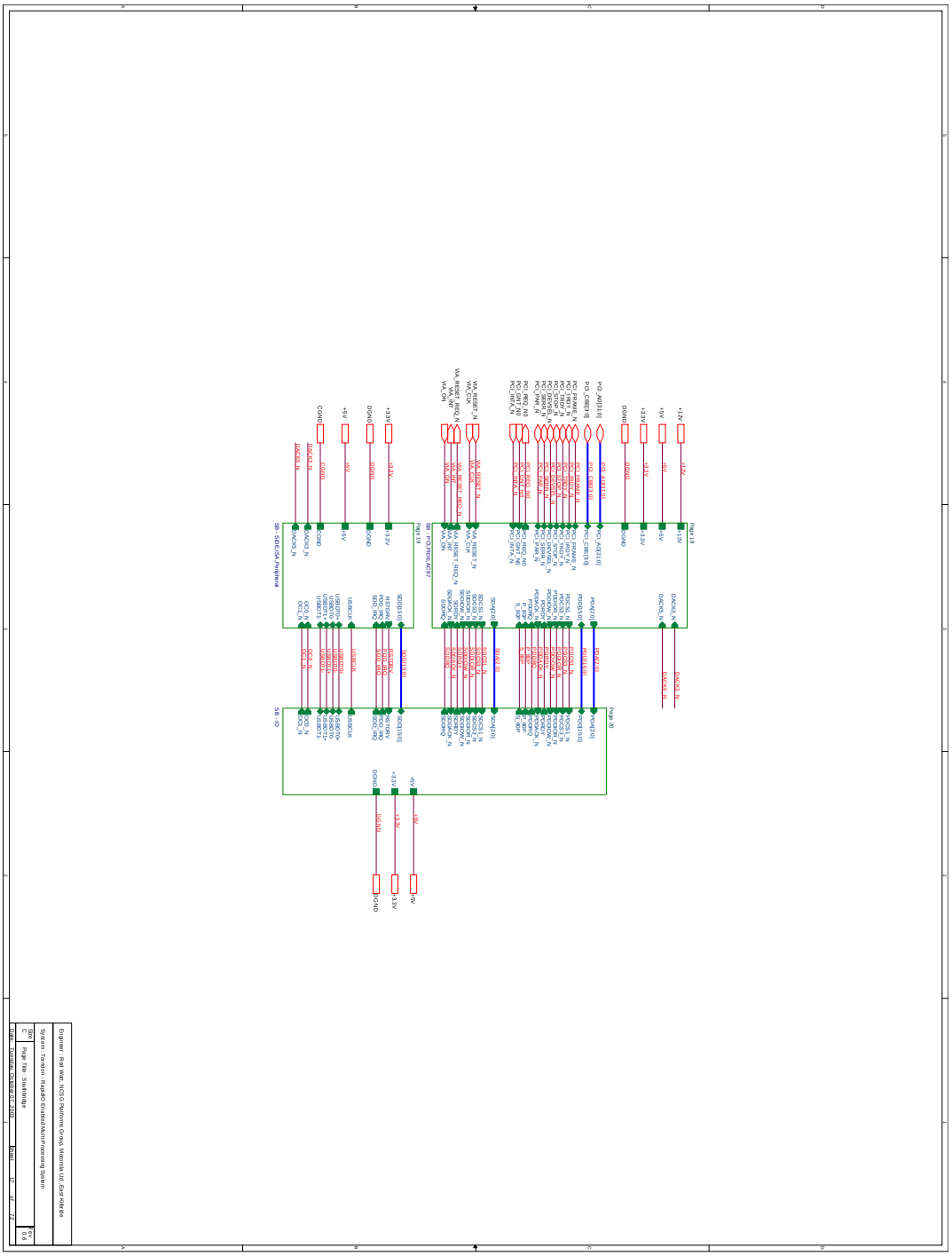


Figure A-15. Southbridge—Top Level

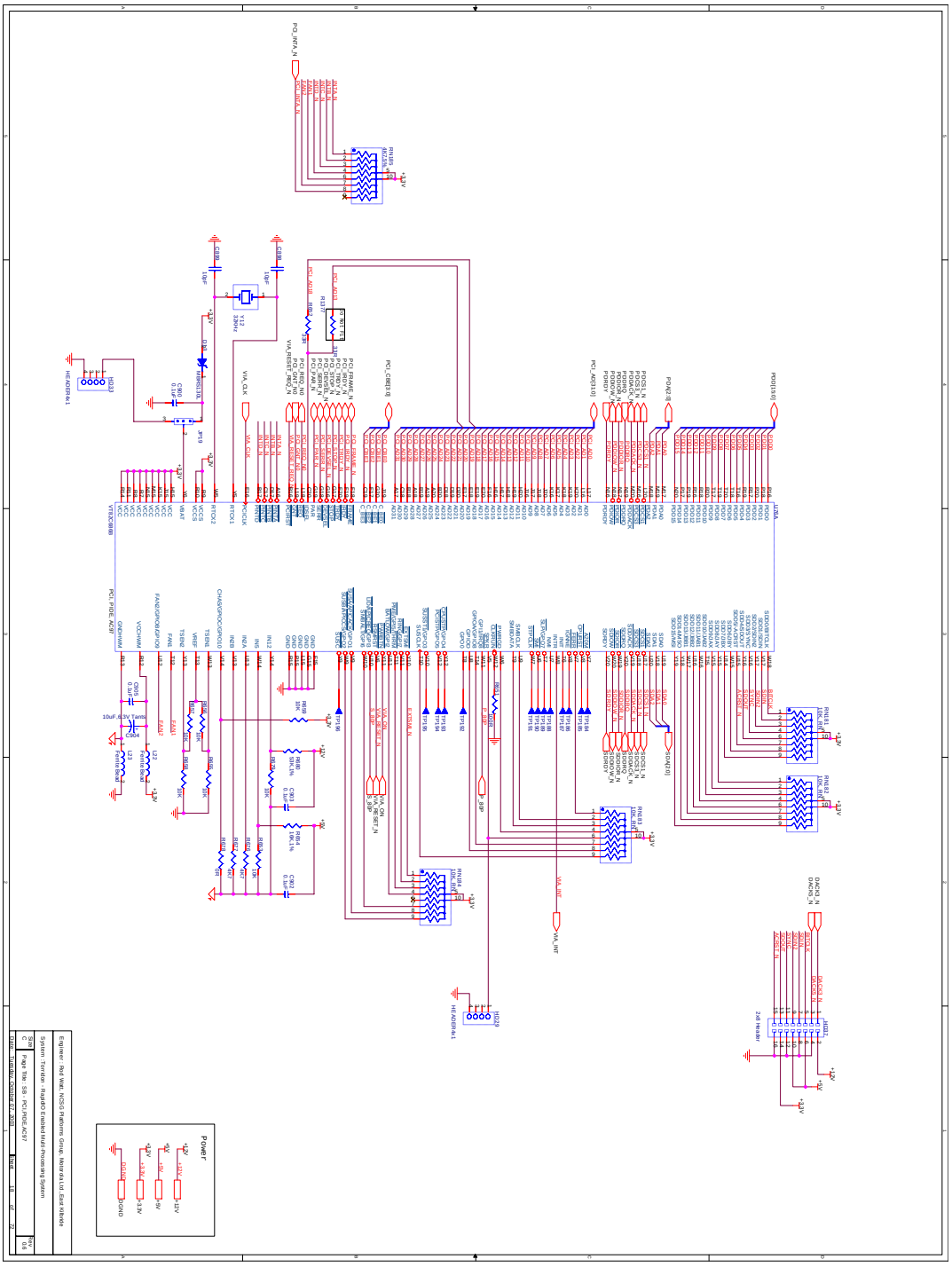


Figure A-16. Southbridge—PCI, PIDE, AC97

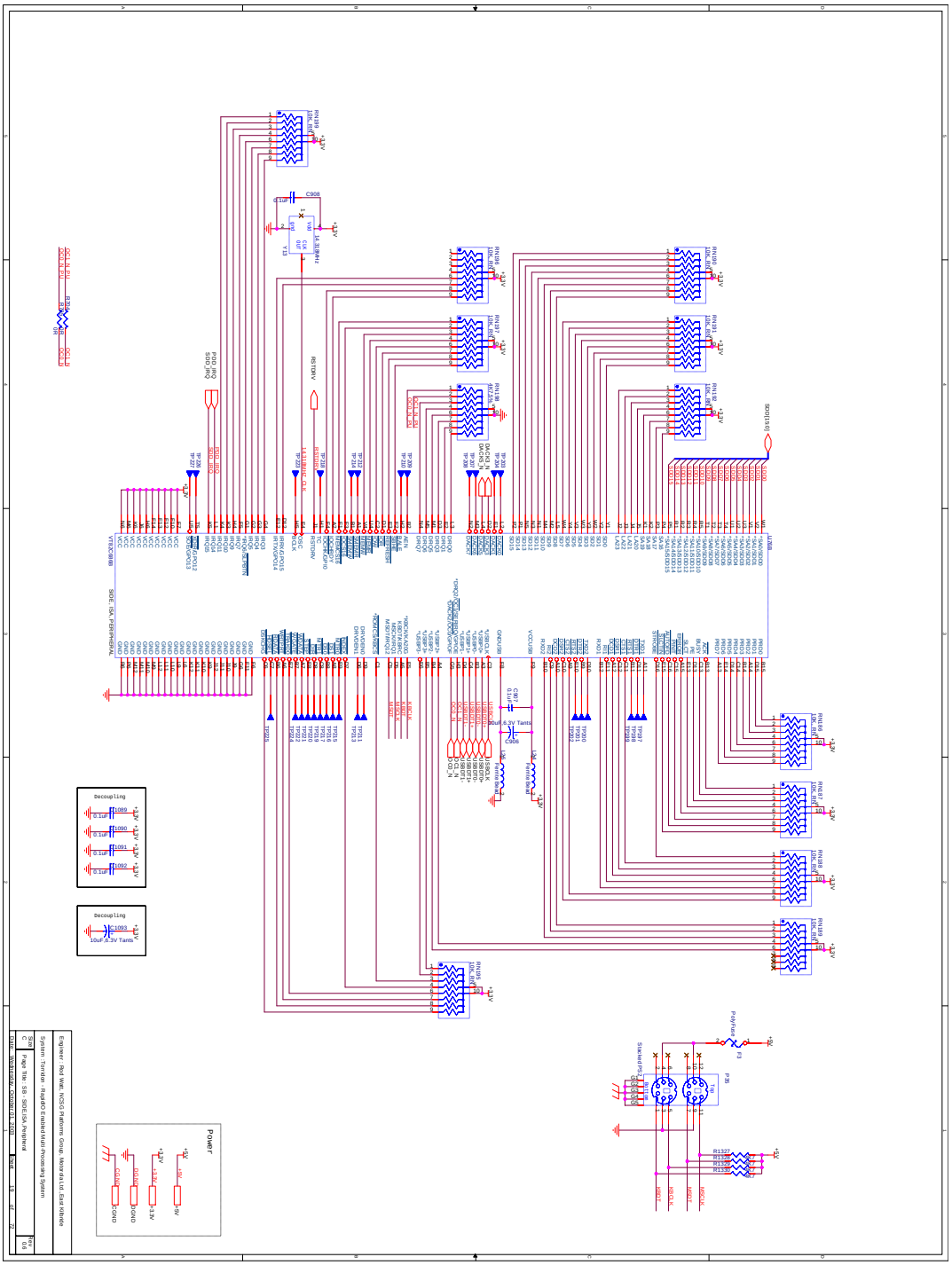


Figure A-17. Southbridge—Side, ISA, Peripheral

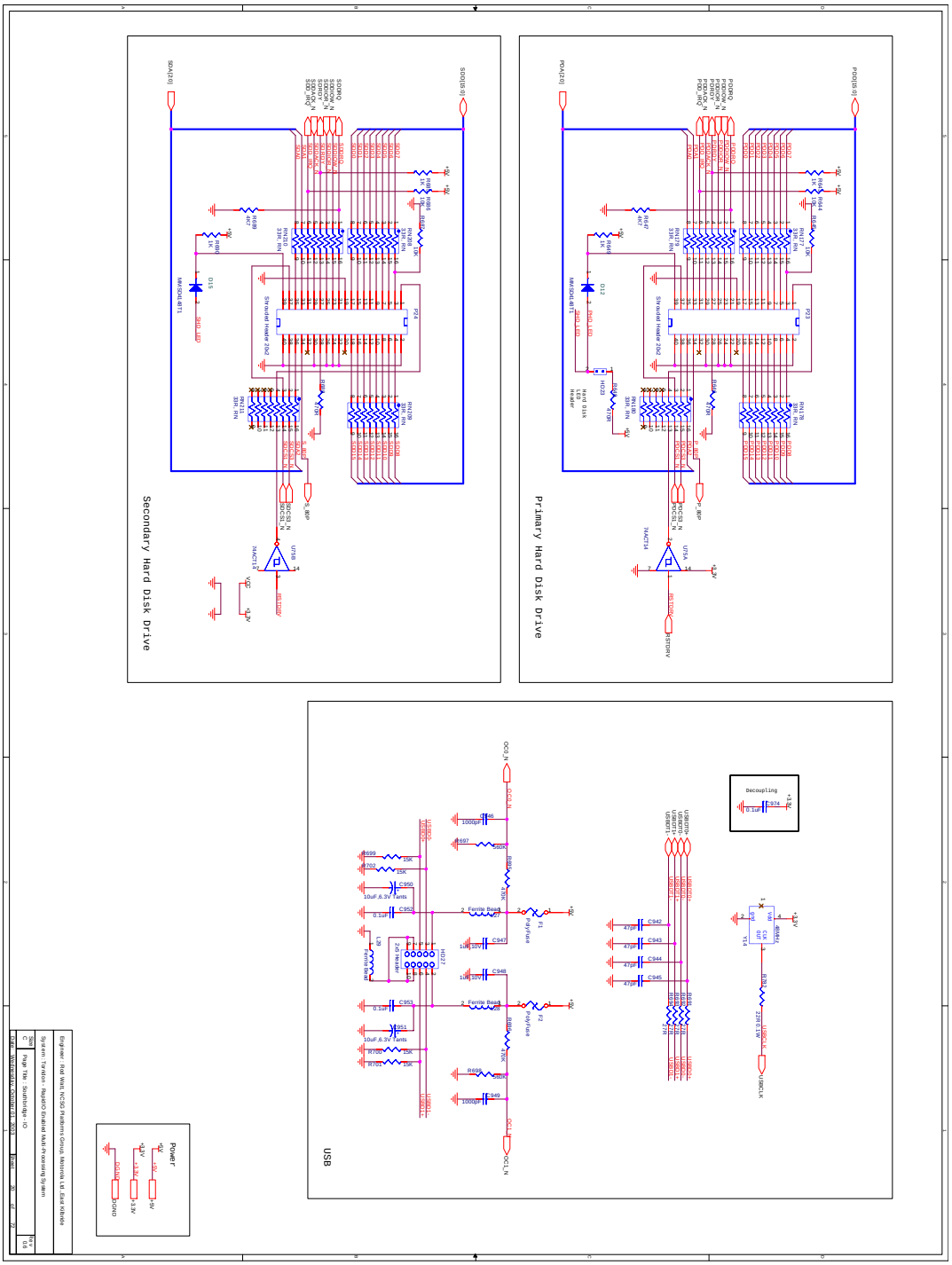


Figure A-18. Southbridge—IO

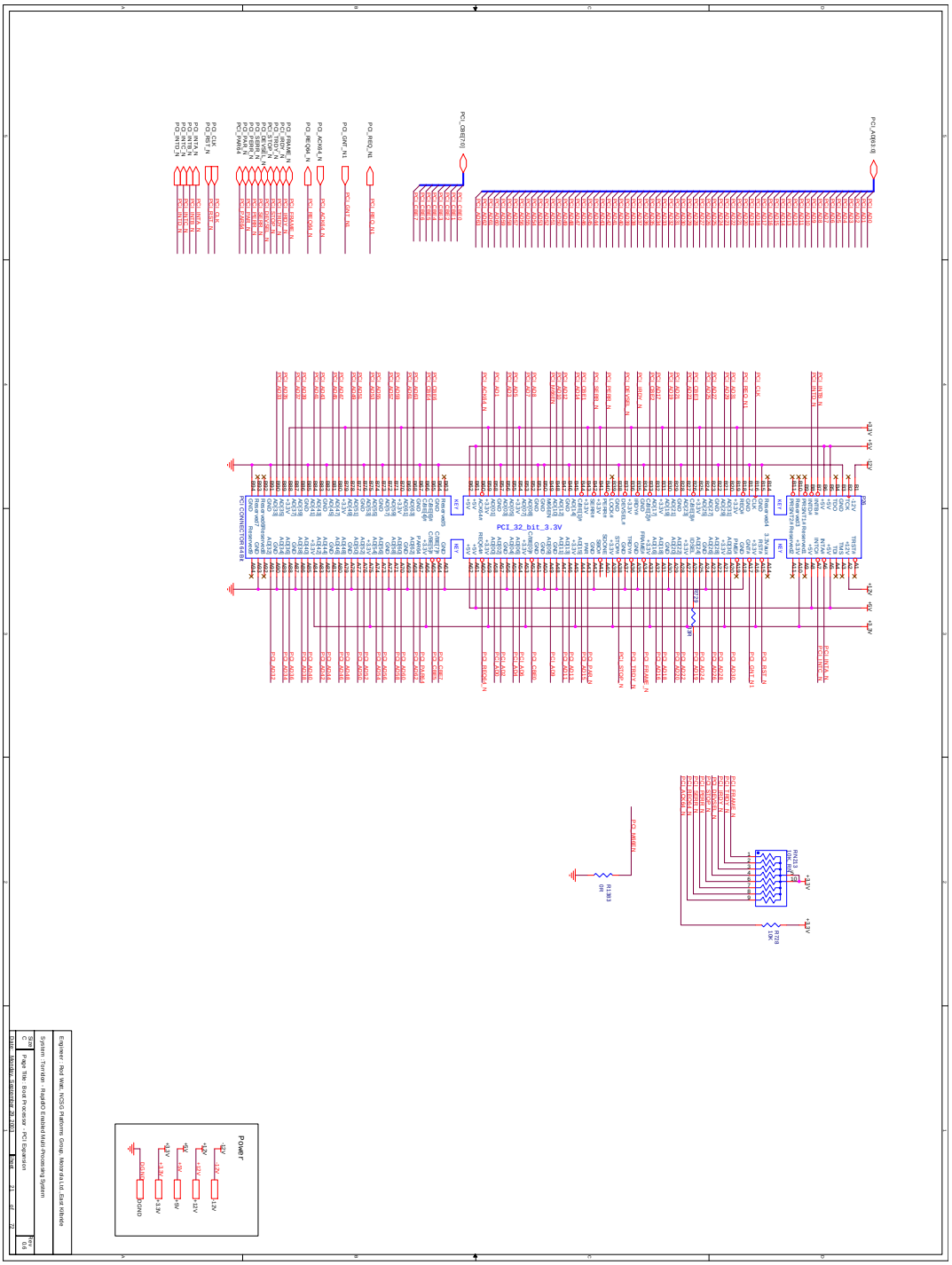


Figure A-19. Boot Processor—PCI Slot

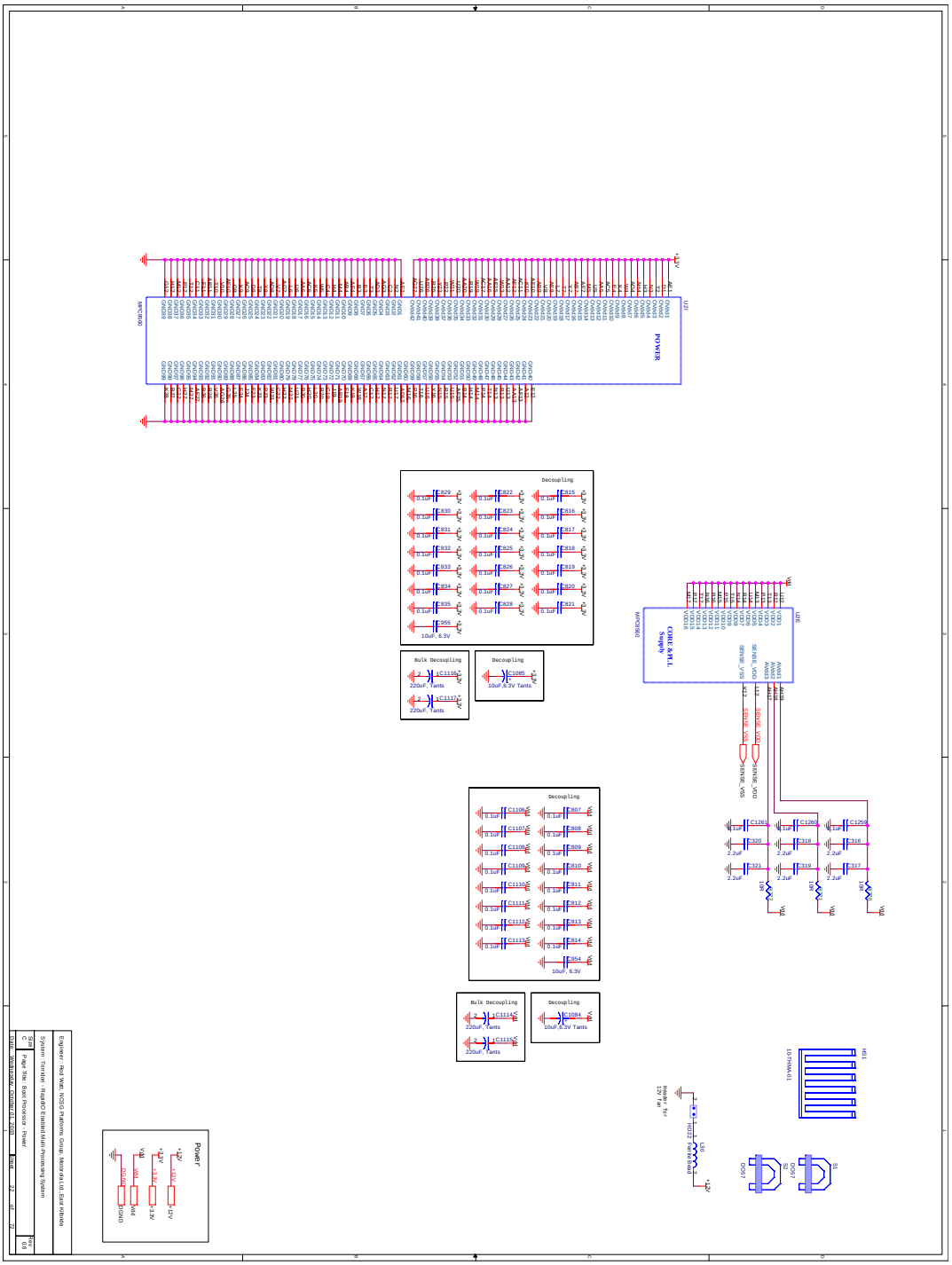


Figure A-20. Boot Processor—Power

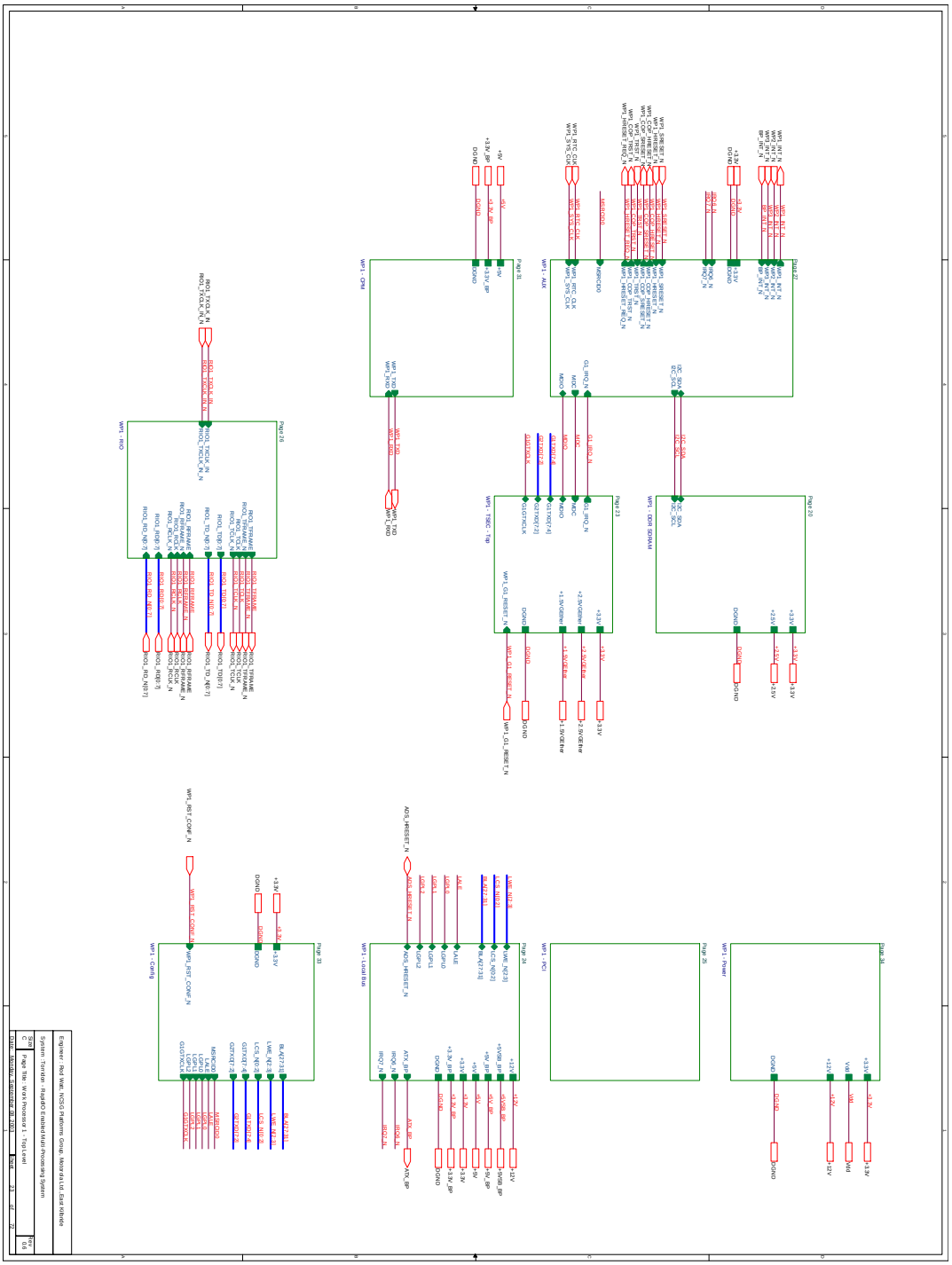


Figure A-21. Work Processor 1—Top Level

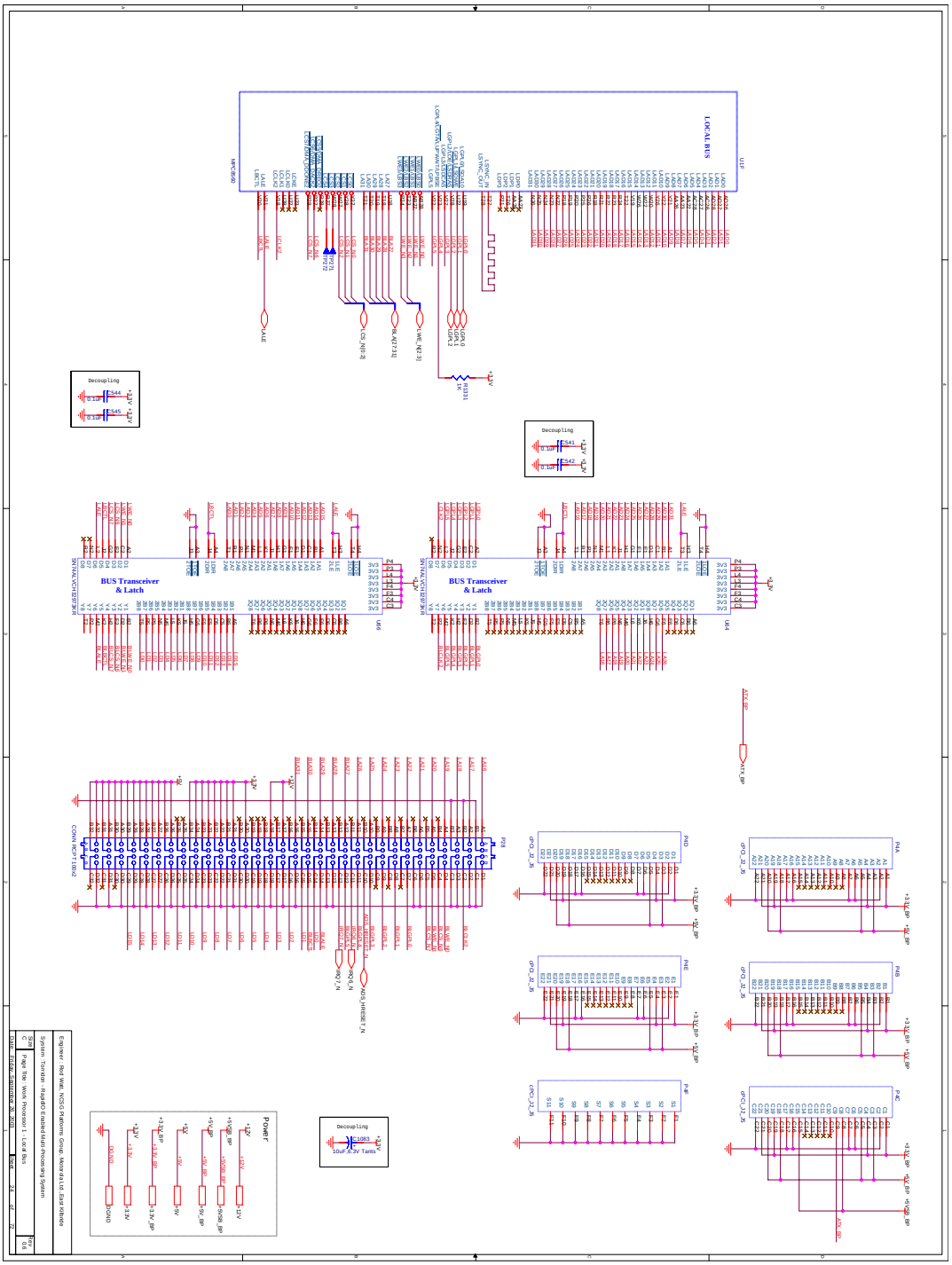


Figure A-22. Work Processor 1—Local Bus

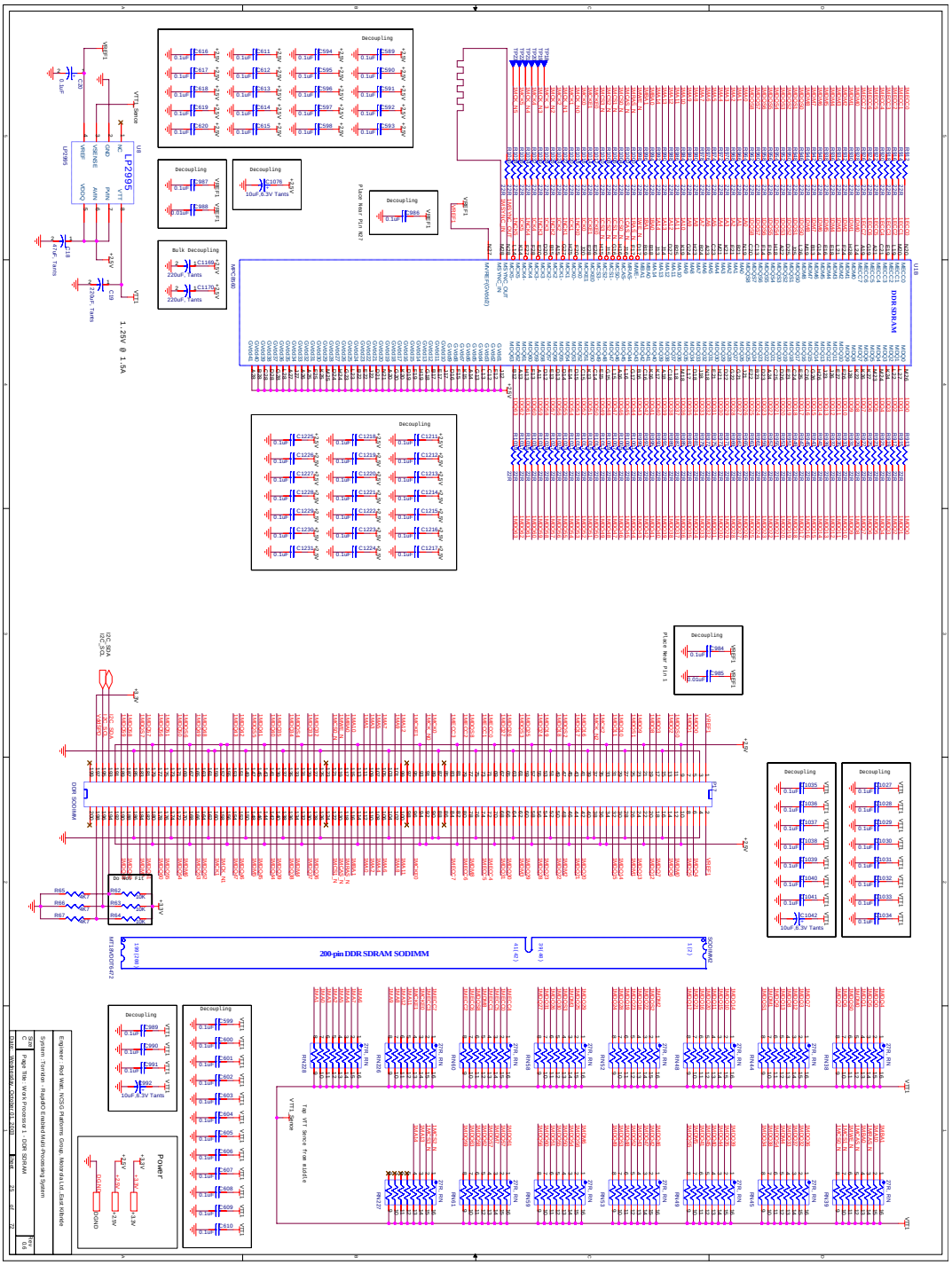


Figure A-23. Work Processor 1—DDR SDRAM

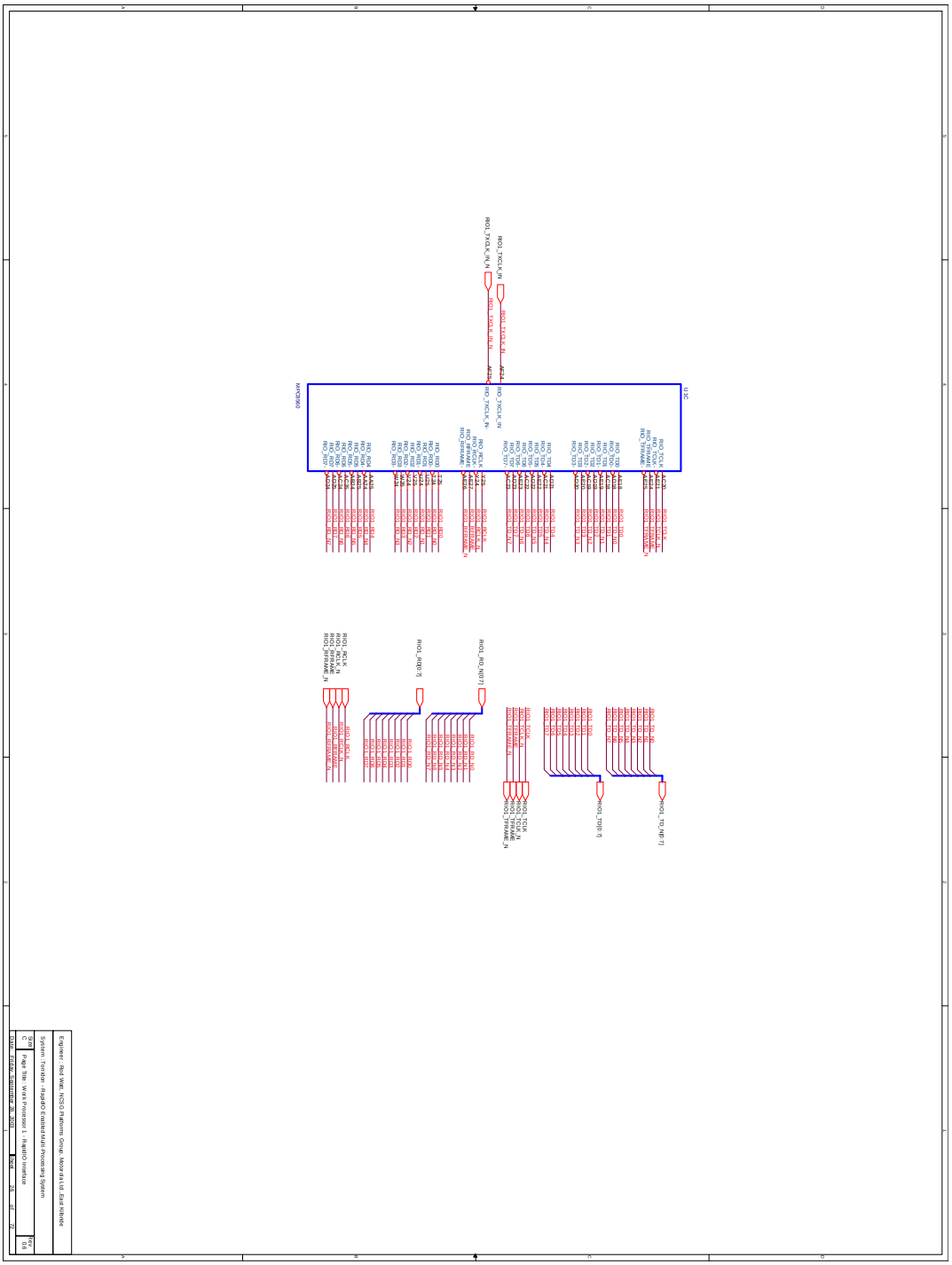


Figure A-24. Work Processor 1—RapidIO Interface

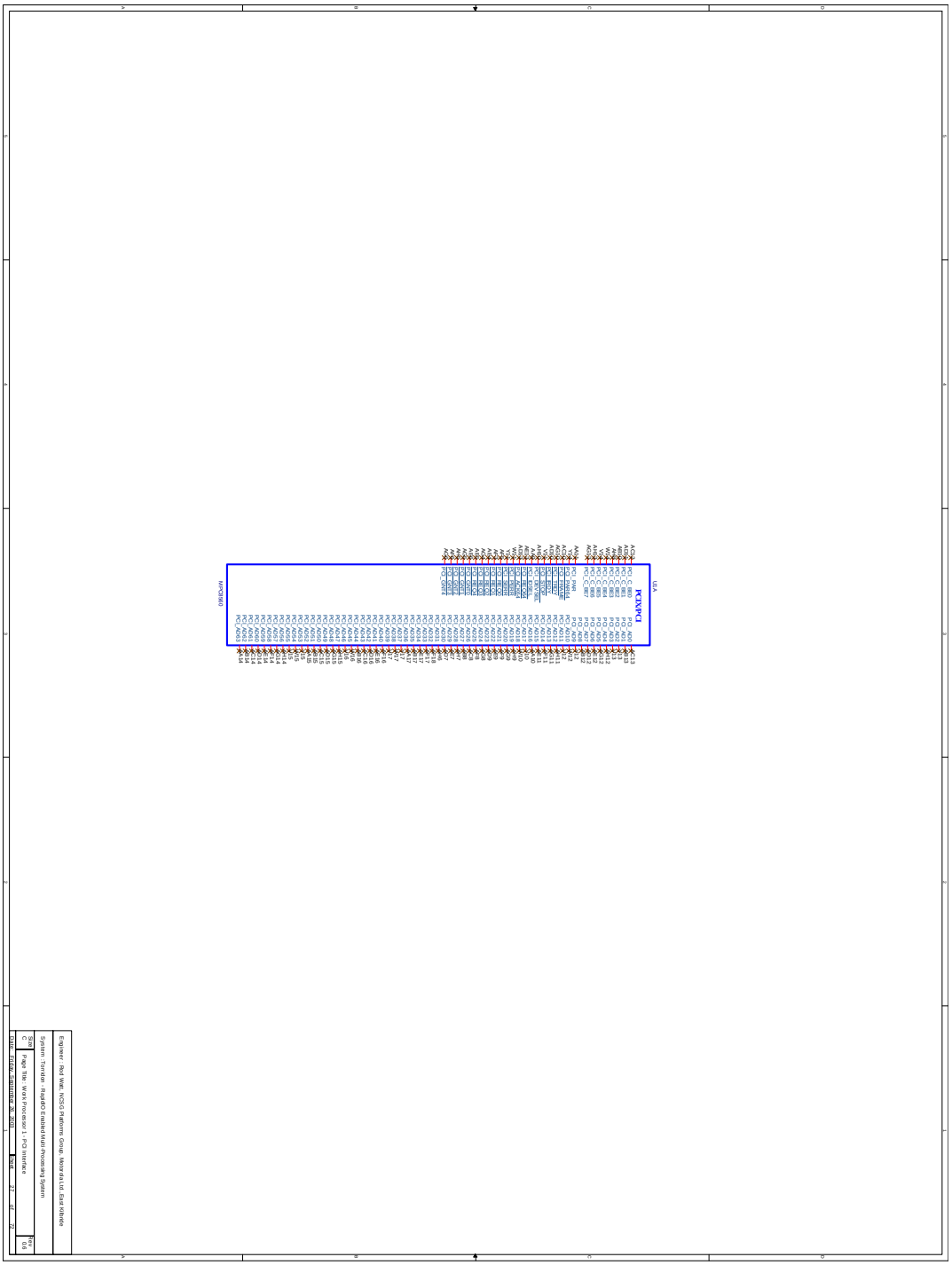


Figure A-25. Work Processor 1—PCI Interface

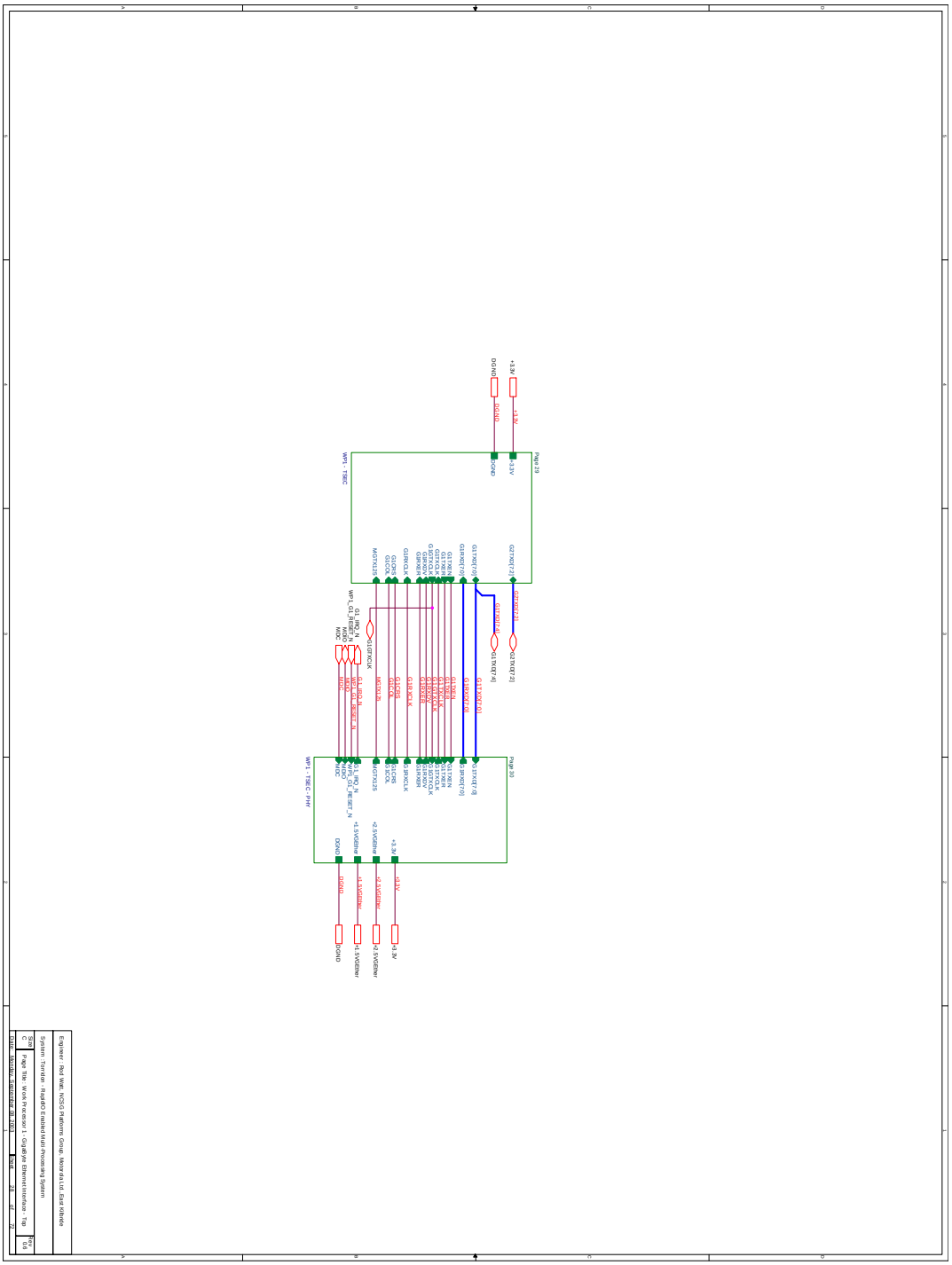


Figure A-26. Work Processor 1—GigaByte Ethernet Interface—Top

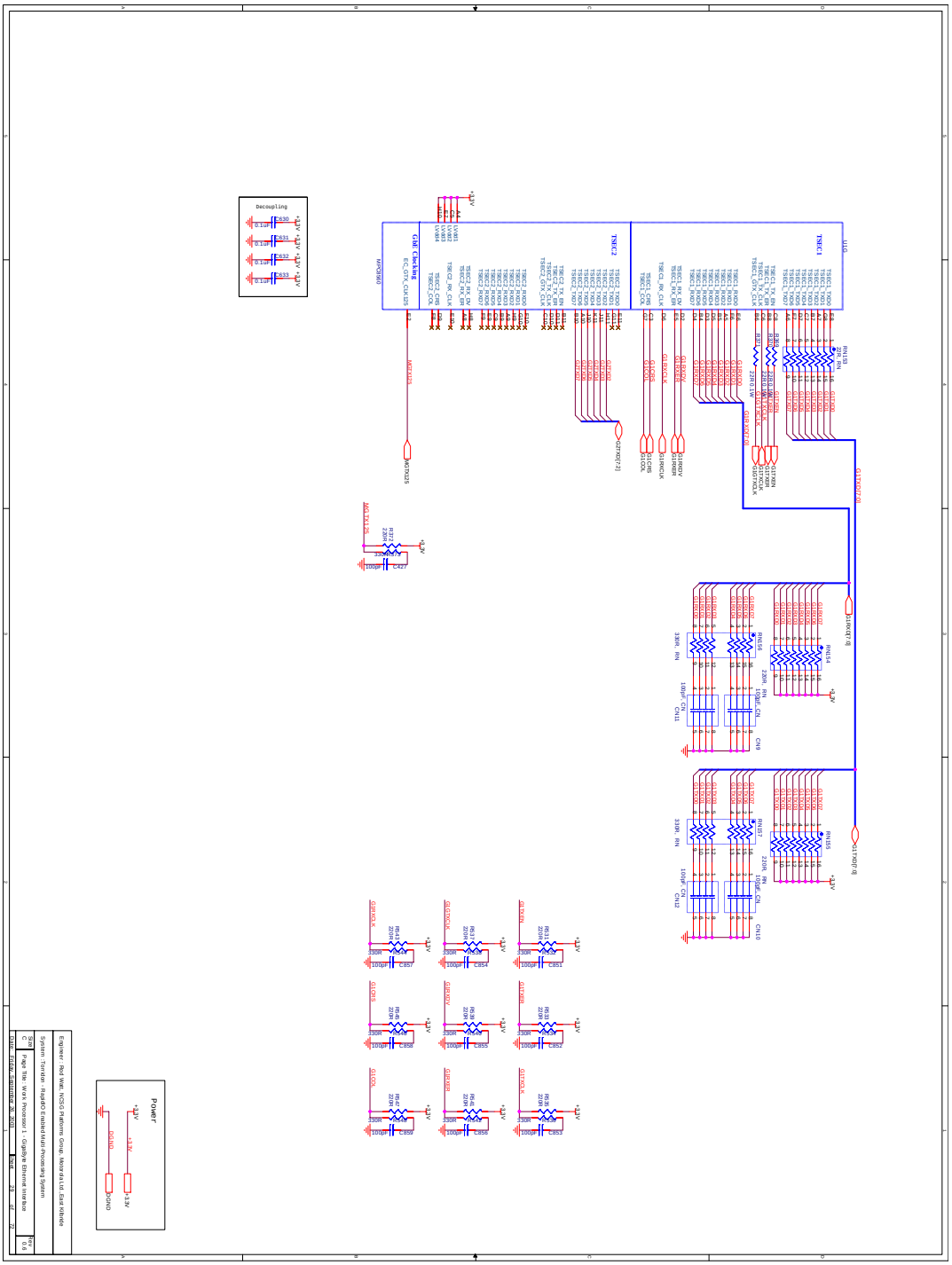


Figure A-27. Work Processor 1—GigaByte Ethernet Interface

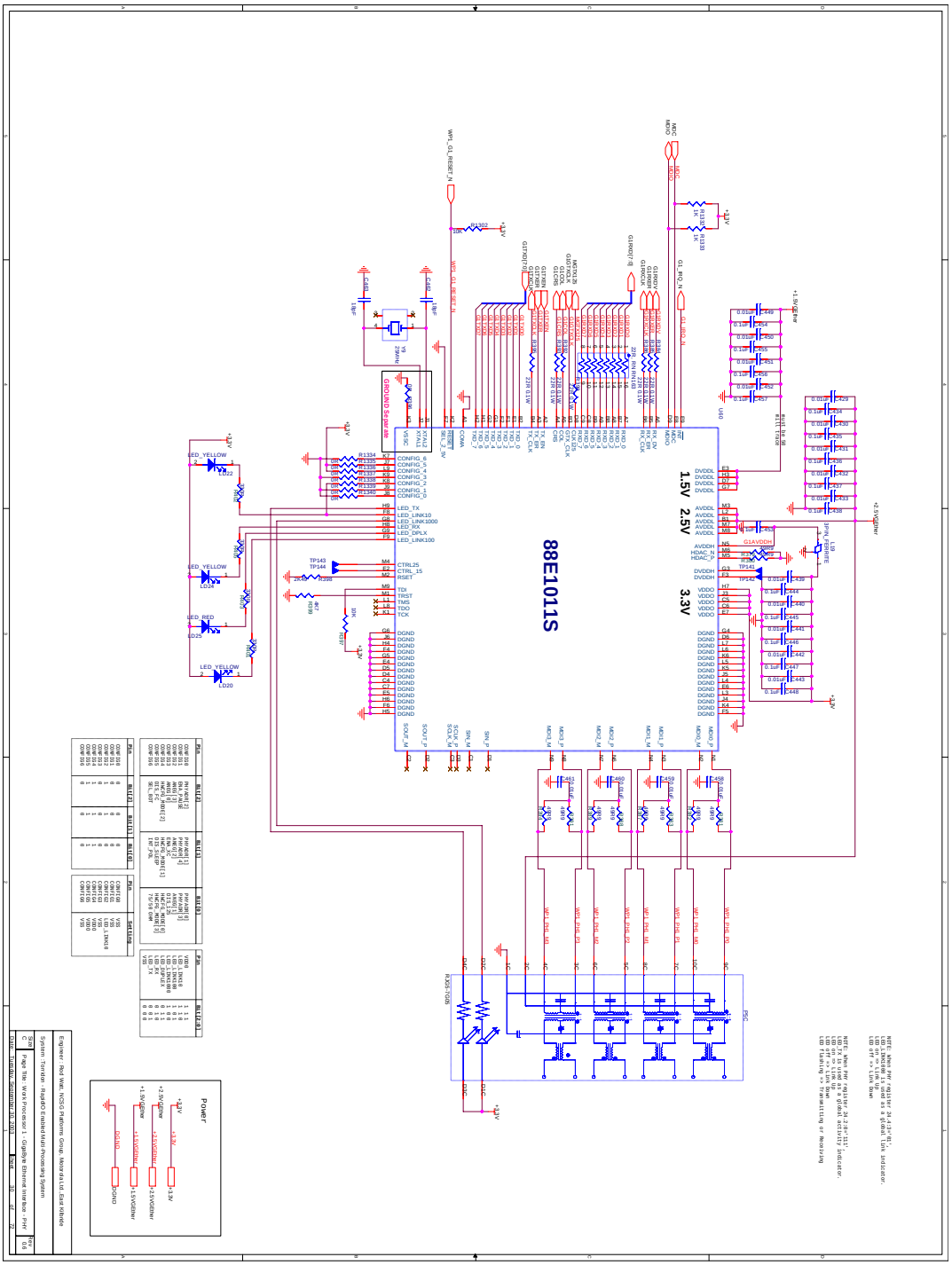


Figure A-28. Work Processor 1—GigaByte Ethernet Interface—PHY

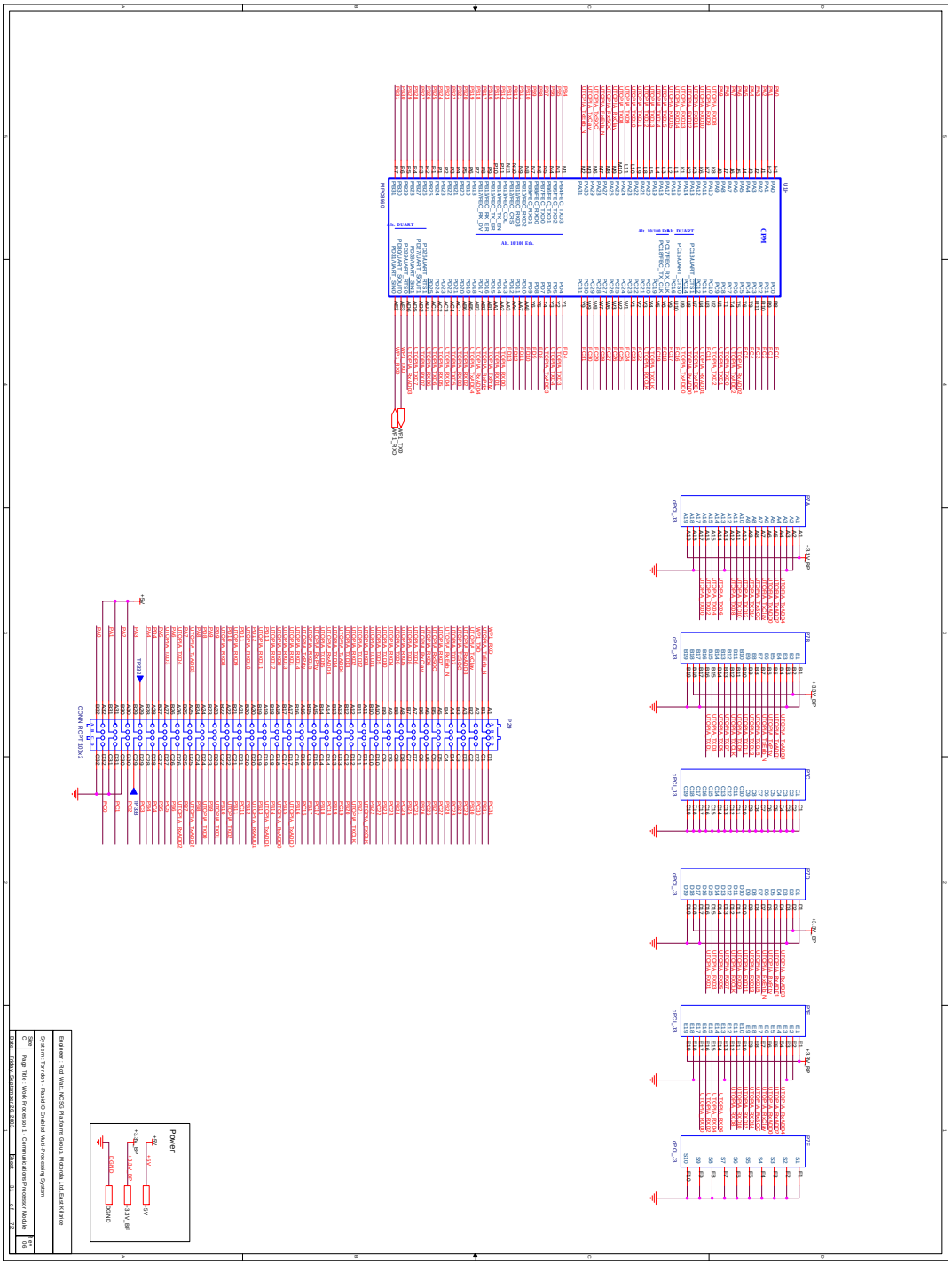


Figure A-29. Work Processor 1—Communications Processor Module

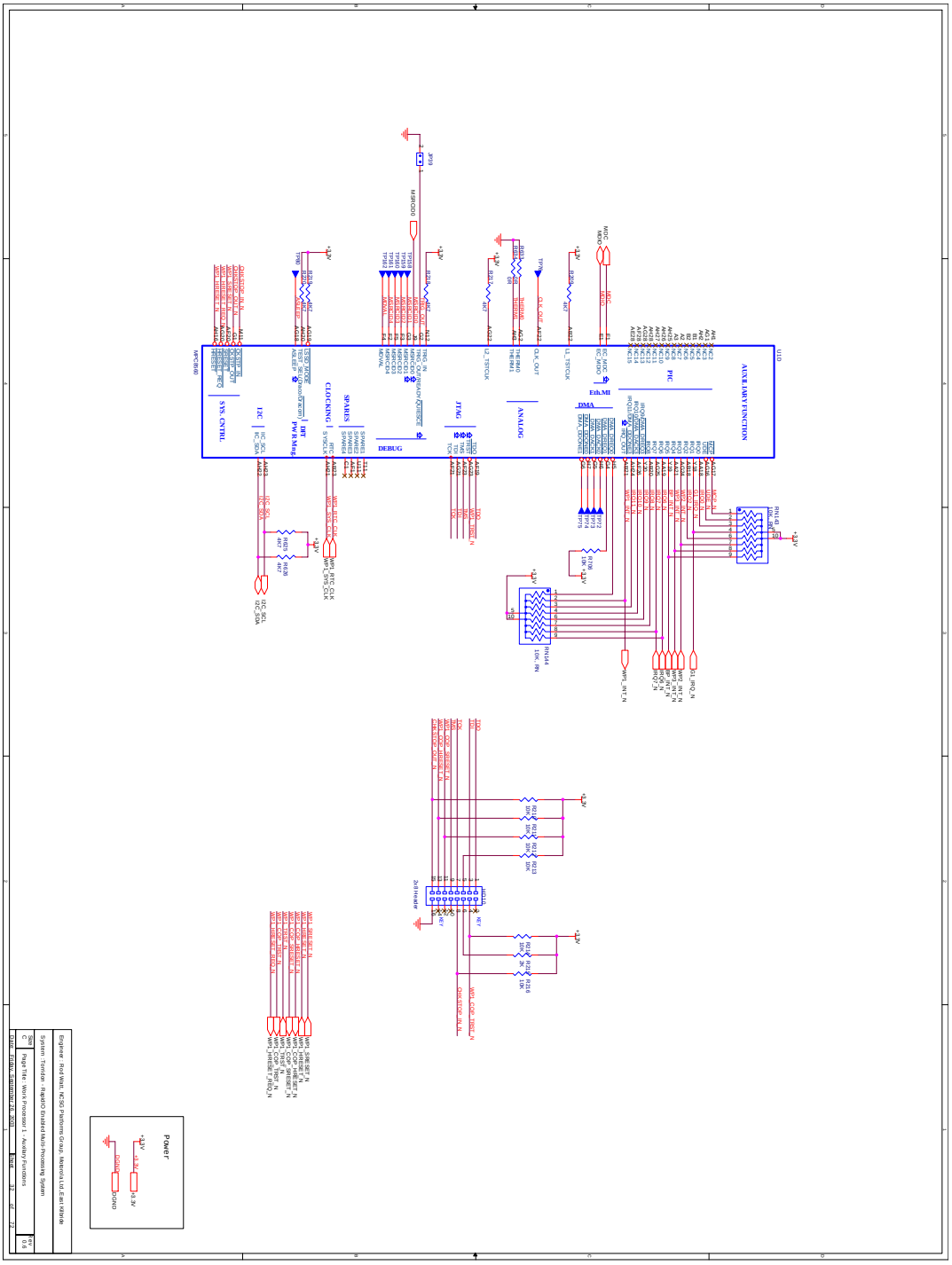


Figure A-30. Work Processor 1—Auxiliary Functions

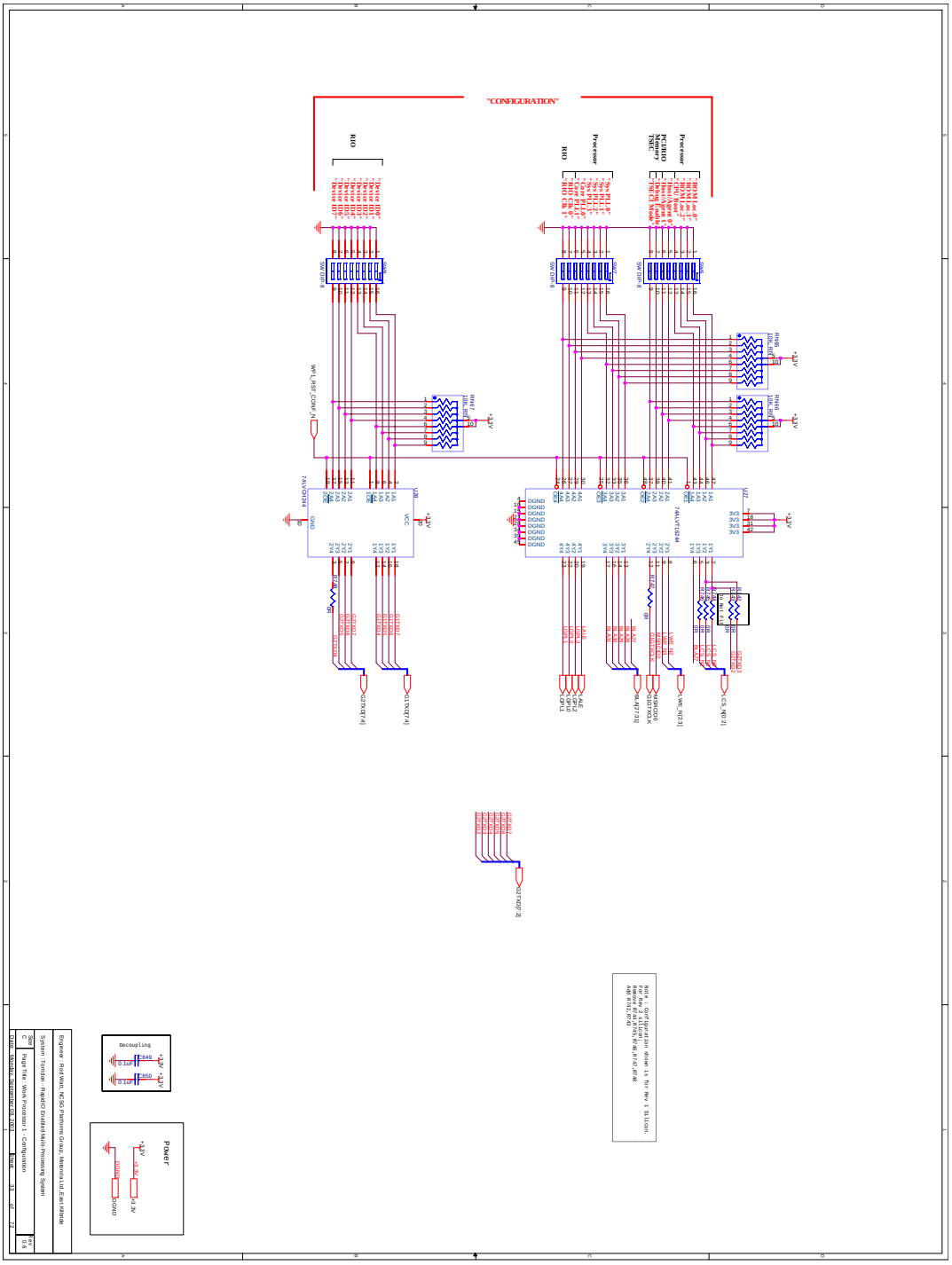


Figure A-31. Work Processor 1—Power On Configuration

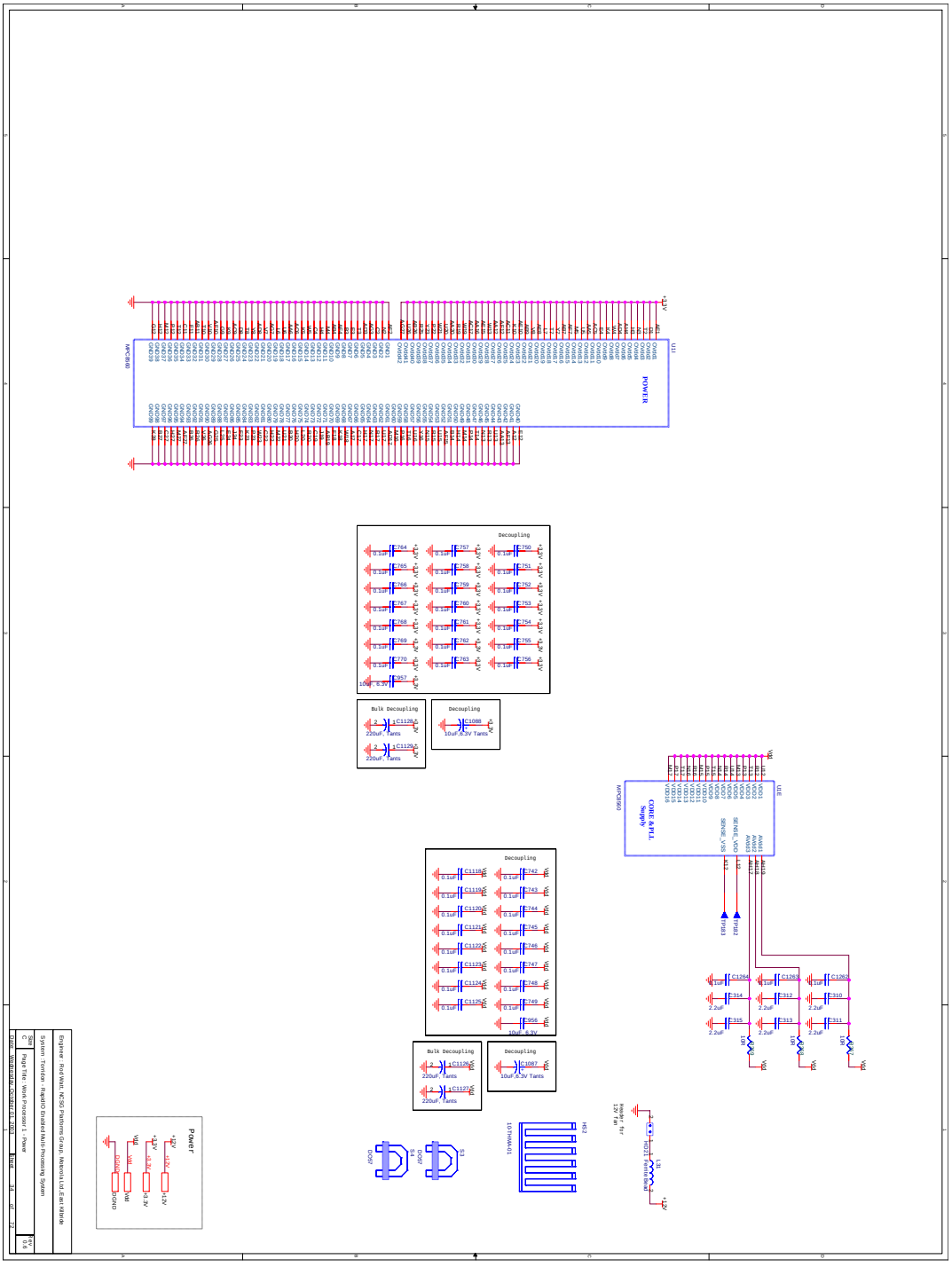


Figure A-32. Work Processor 1—Power

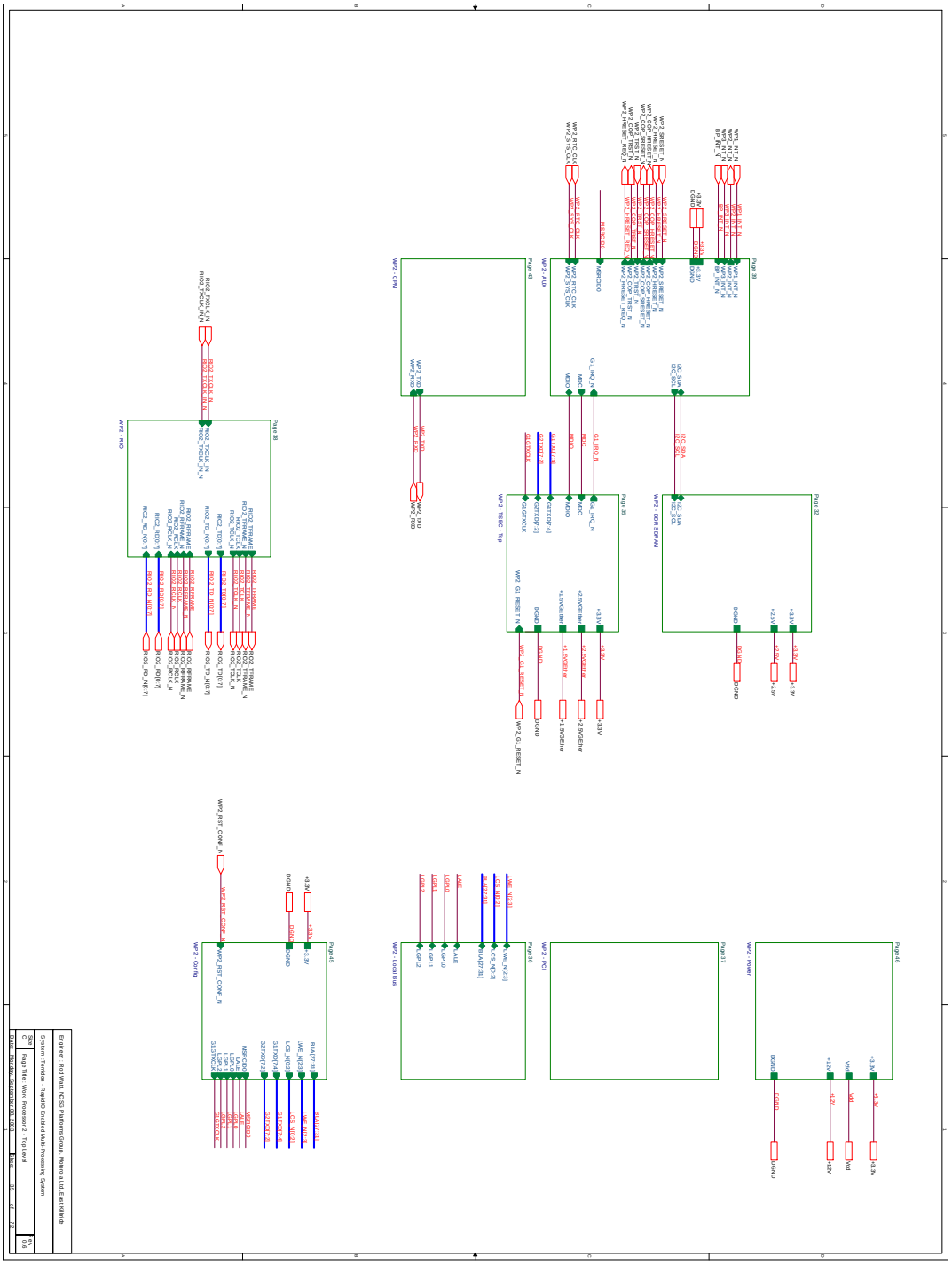


Figure A-33. Work Processor 2—Top Level

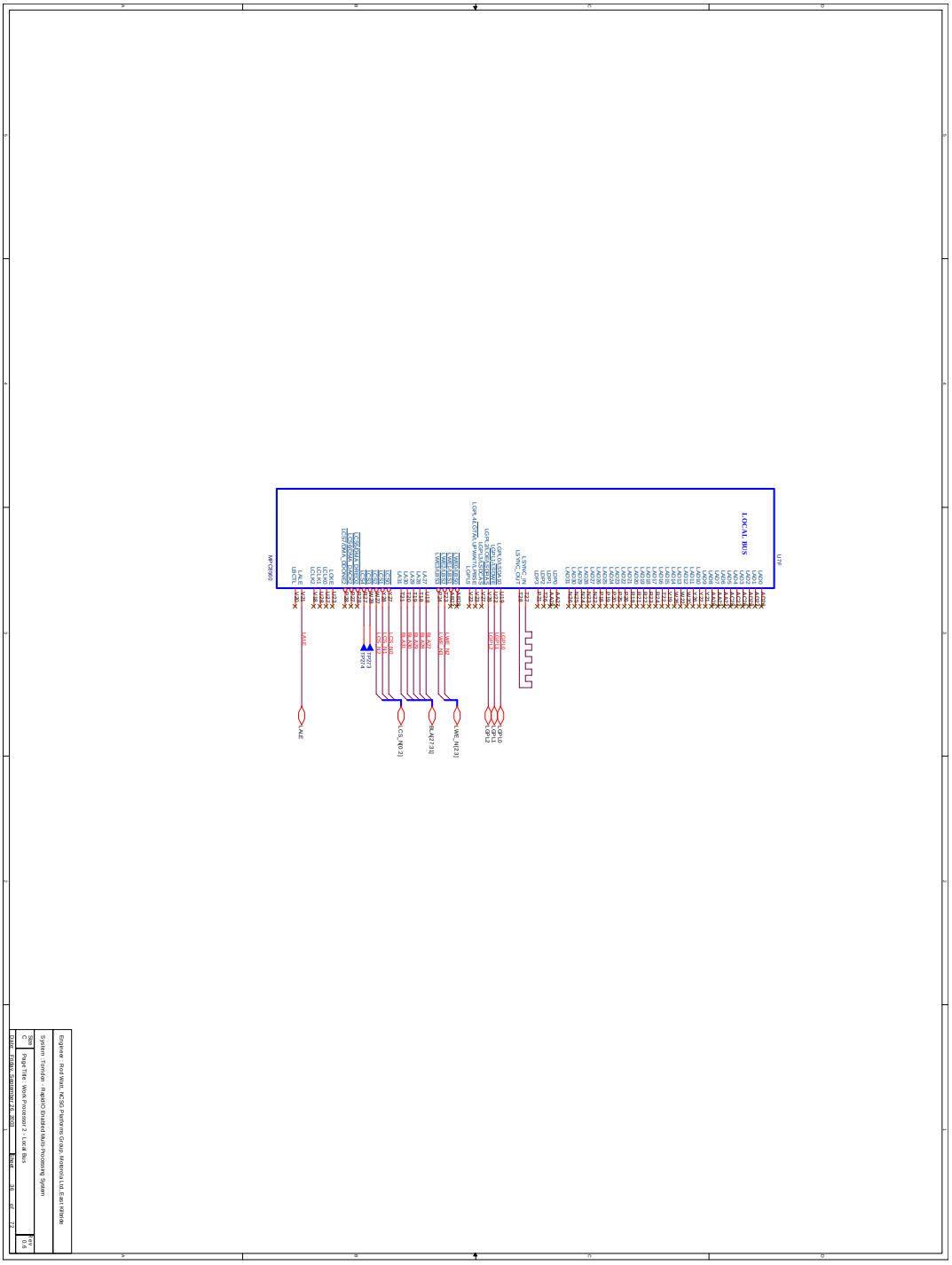


Figure A-34. Work Processor 2—Local Bus

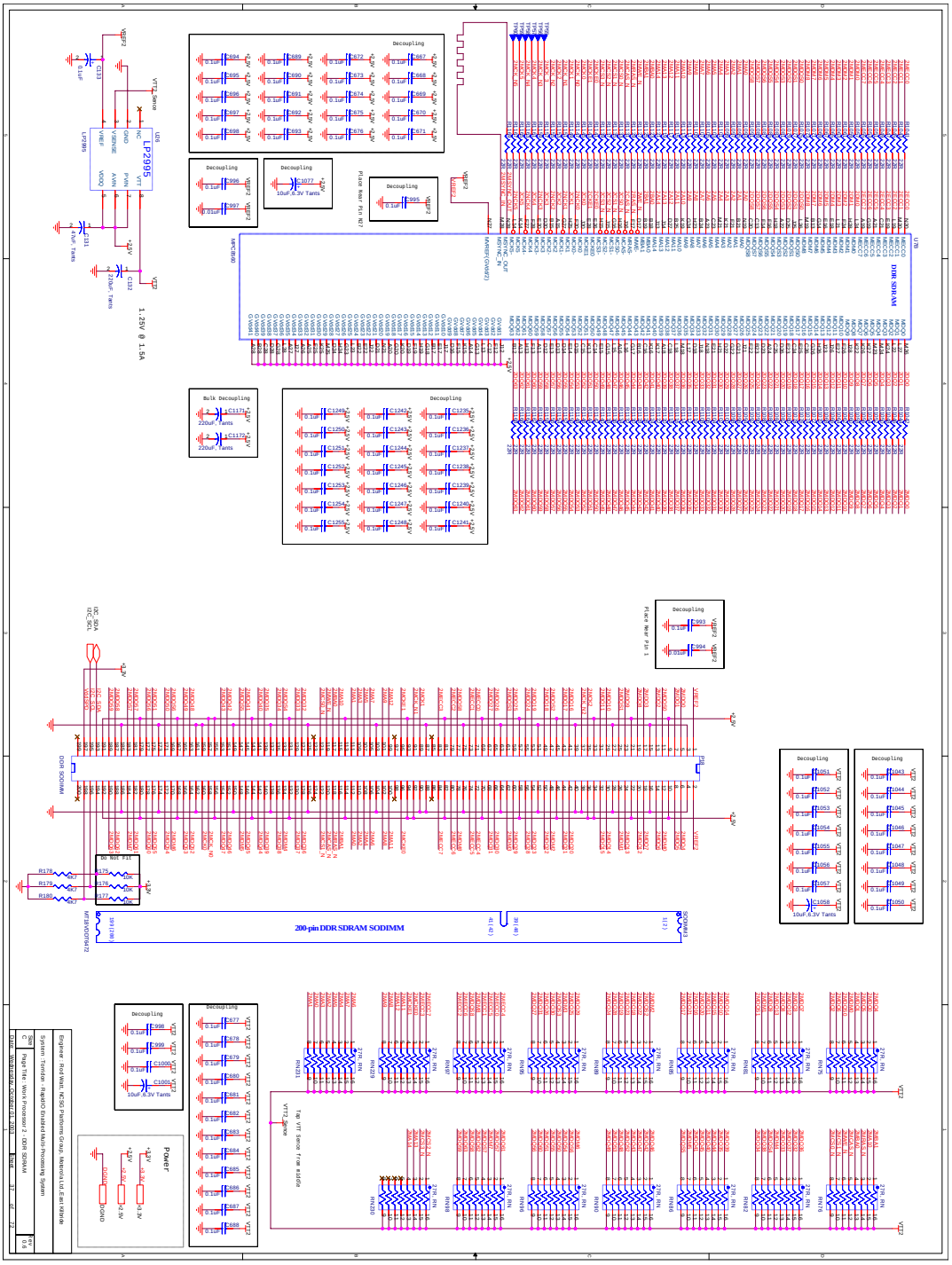


Figure A-35. Work Processor 2—DDR SDRAM

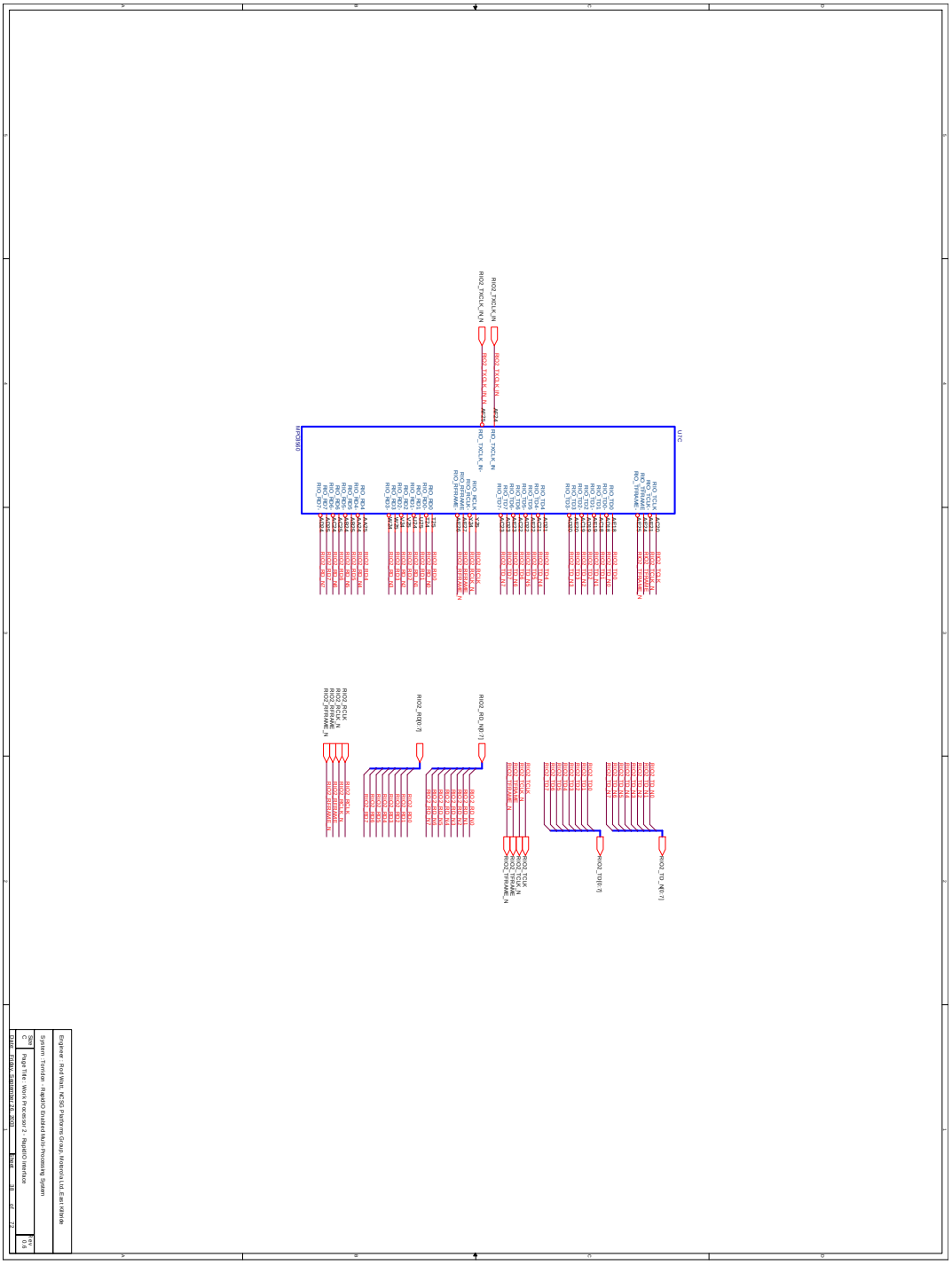


Figure A-36. Work Processor 2—RapidIO Interface

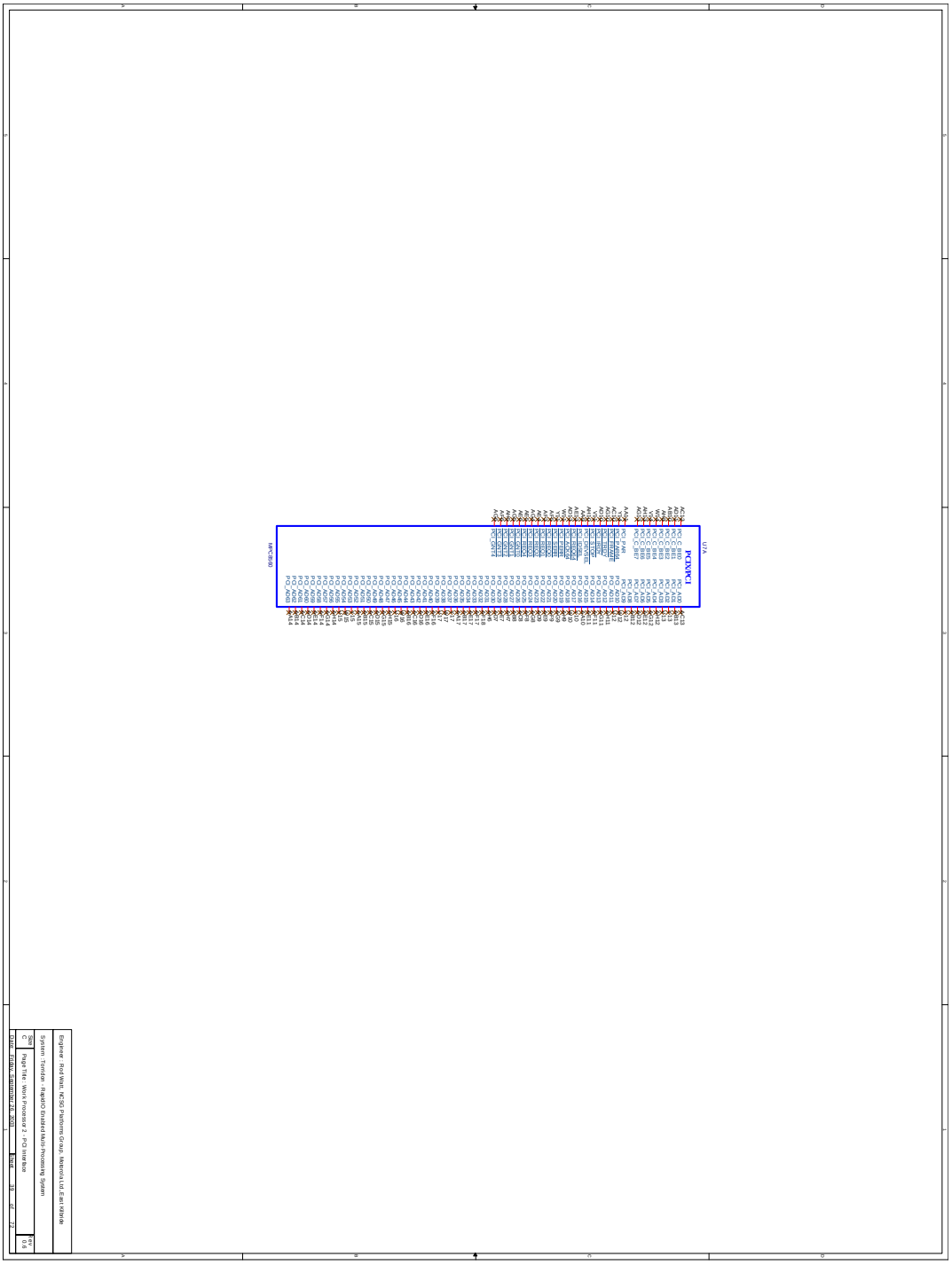


Figure A-37. Work Processor 2—PCI Interface

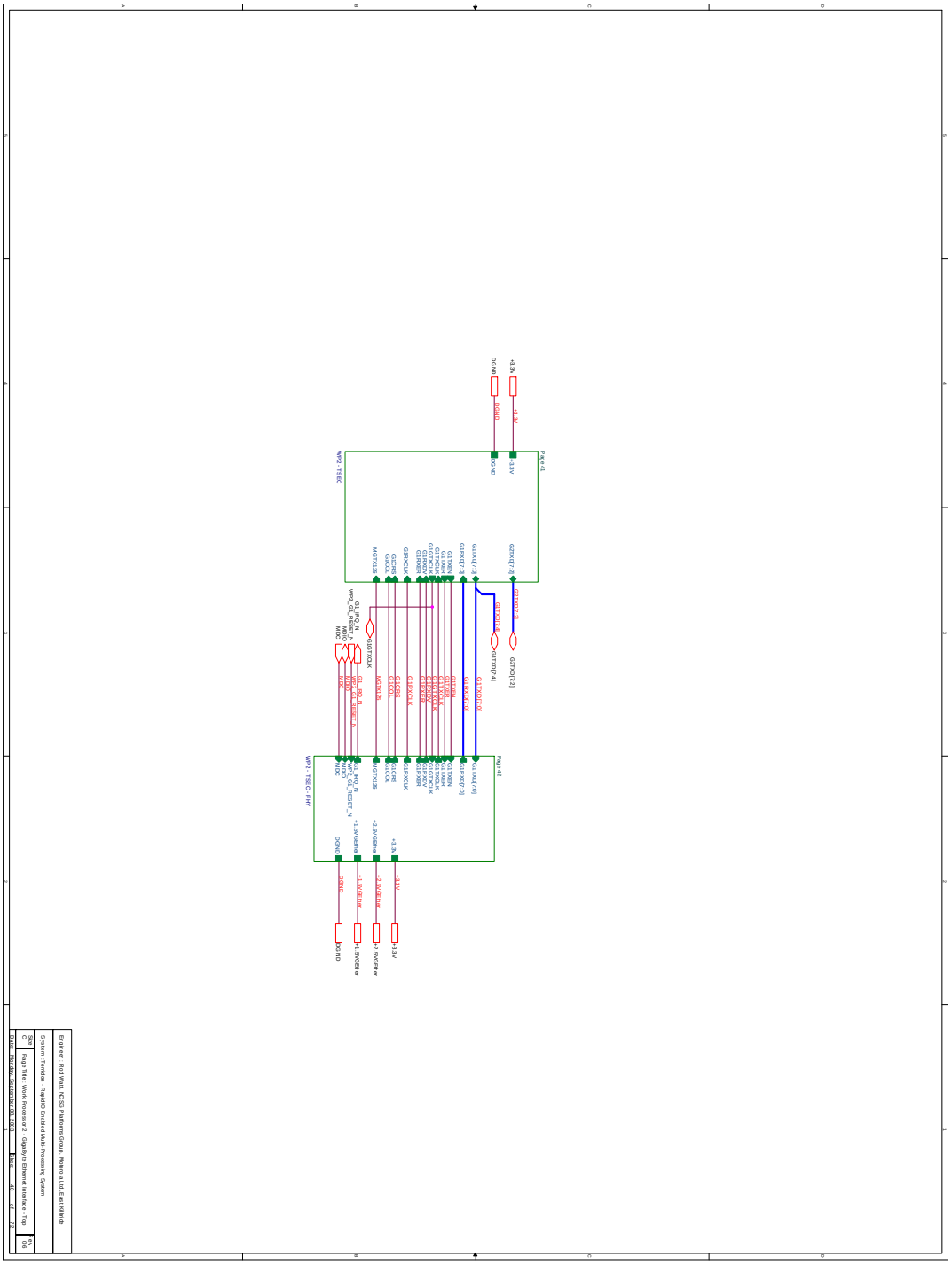


Figure A-38. Work Processor 2—GigaByte Ethernet Interface—Top

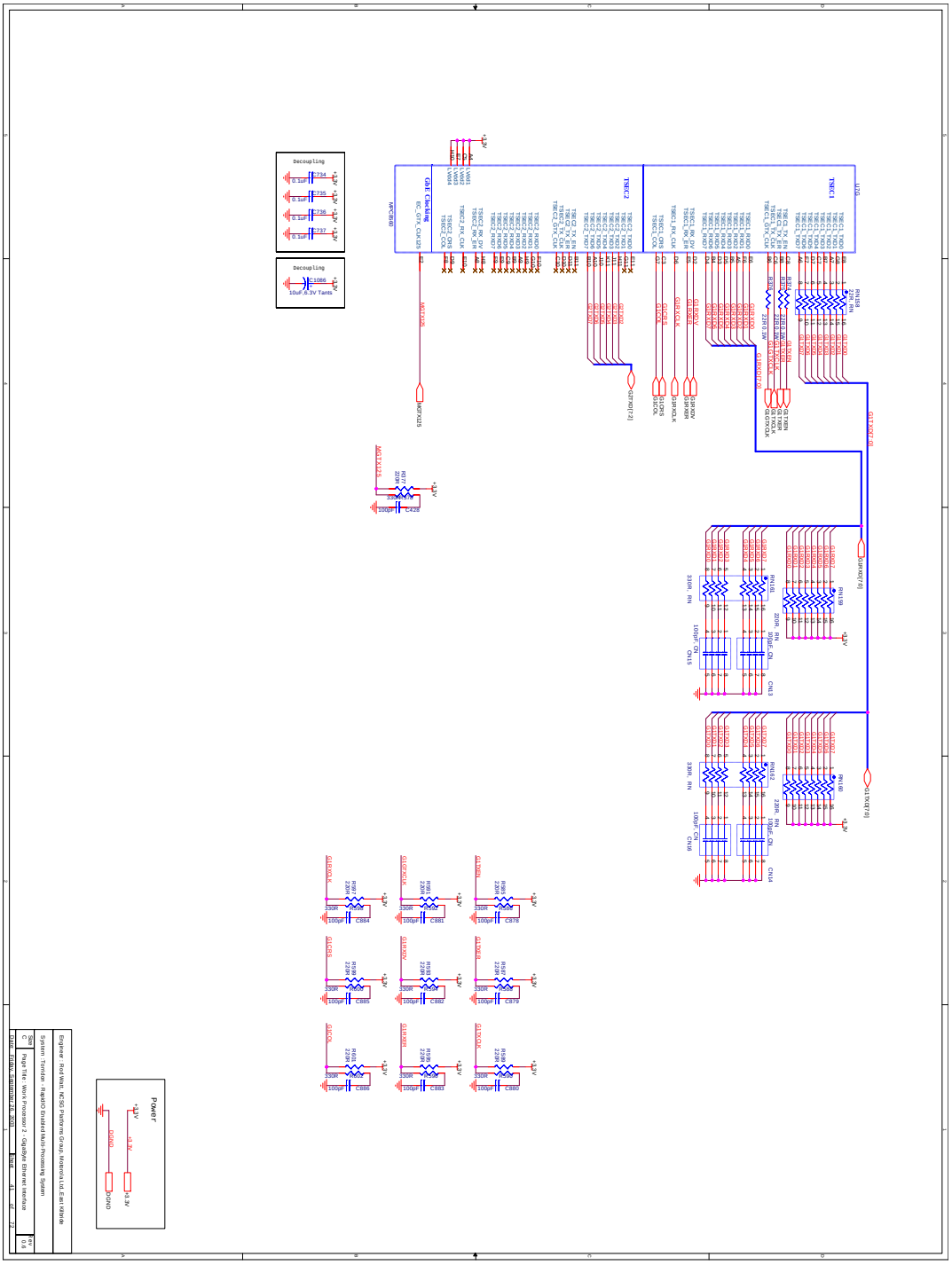


Figure A-39. Work Processor 2—GigaByte Ethernet Interface

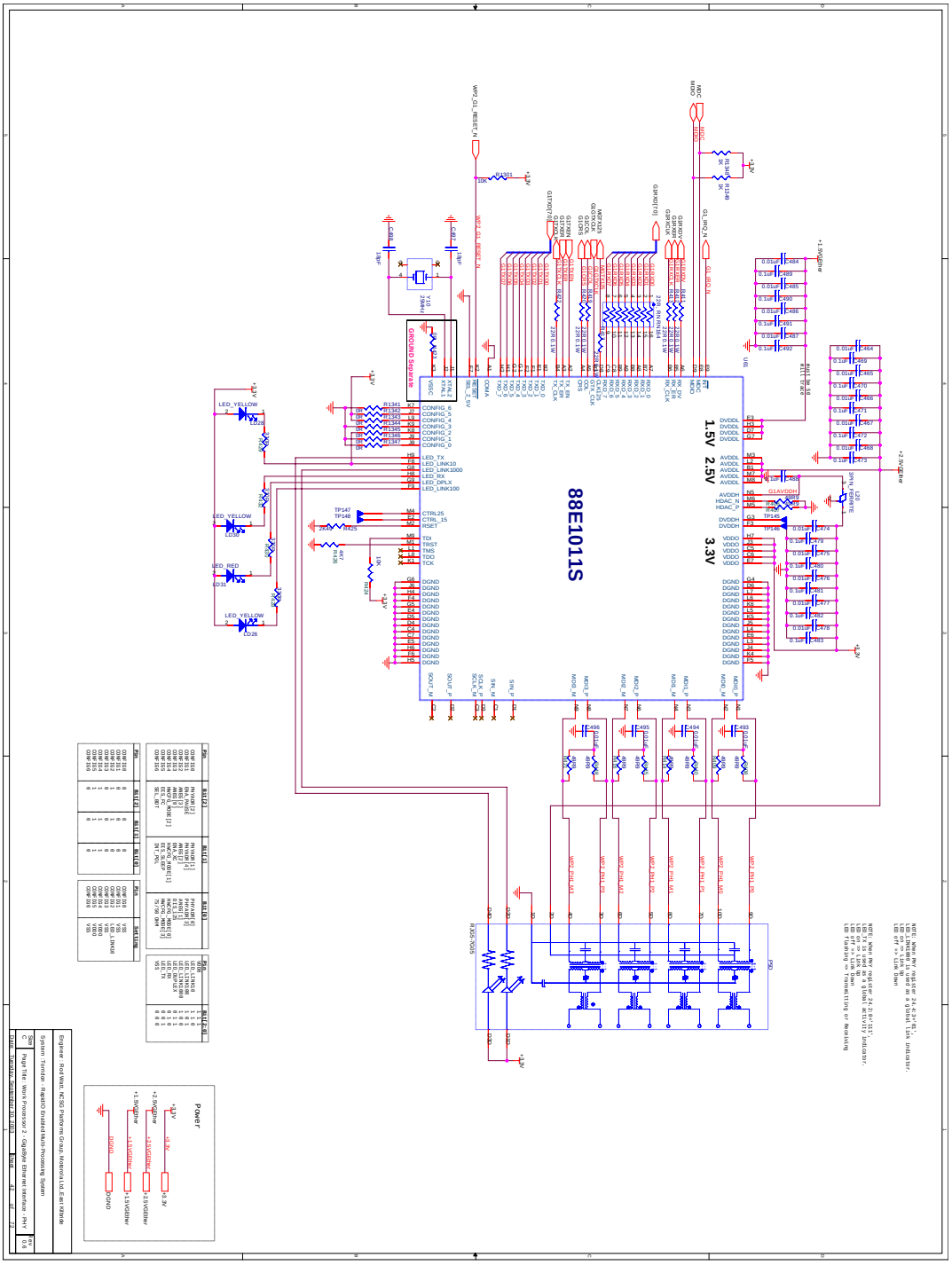


Figure A-40. GigaByte Ethernet Interface—PHY

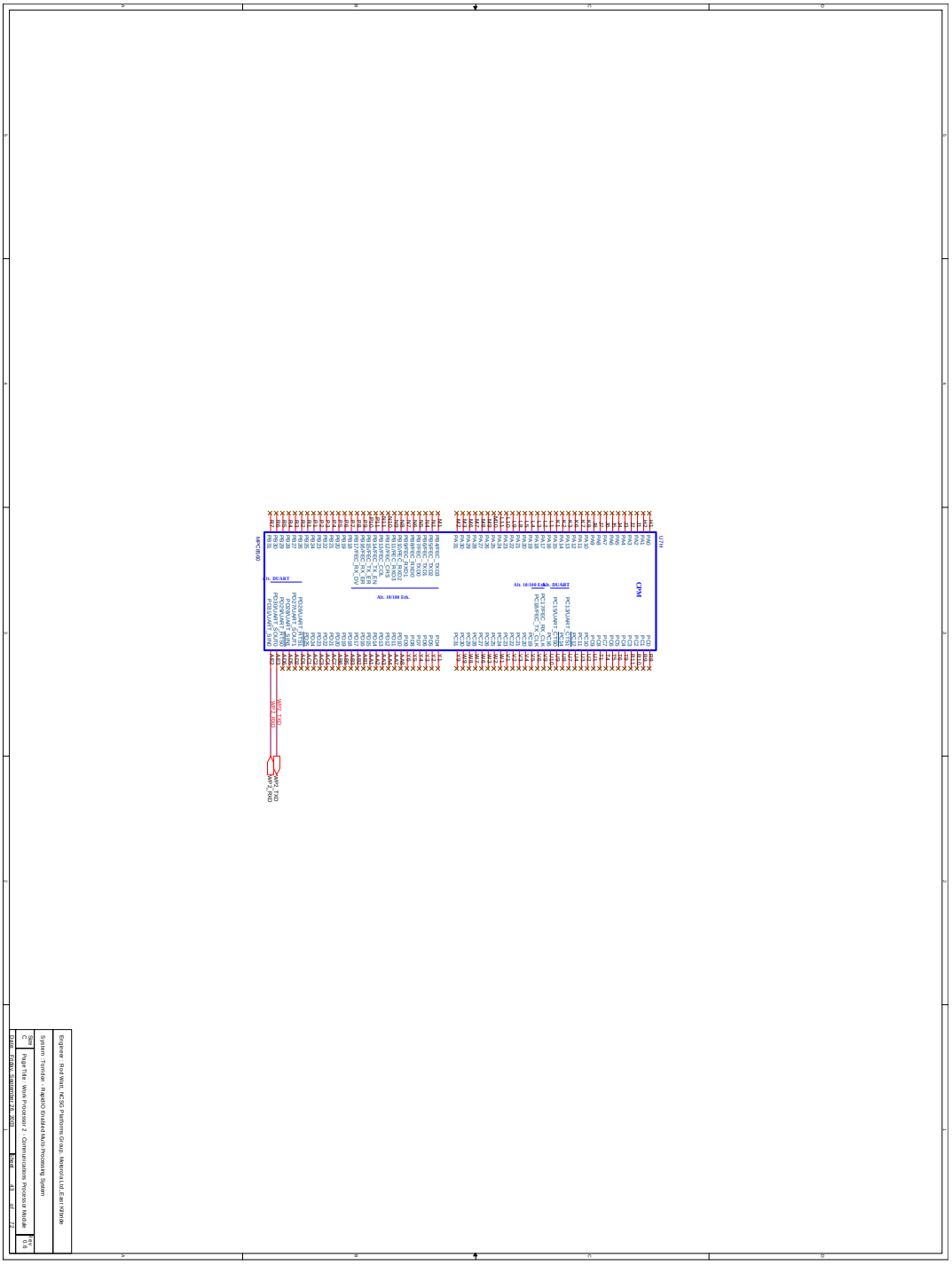


Figure A-41. Work Processor 2—Communications Processor Module

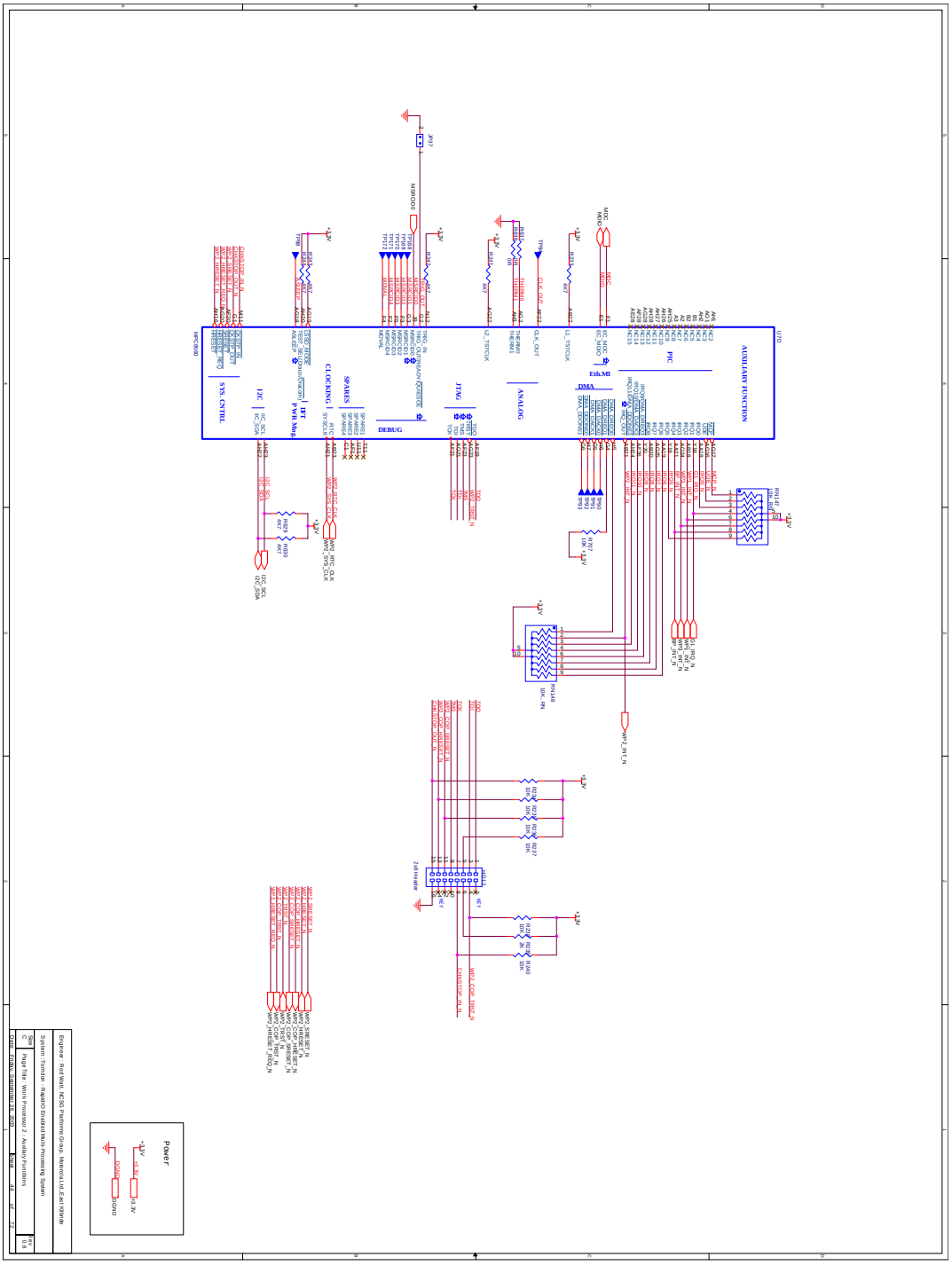


Figure A-42. Work Processor 2—Auxiliary Functions

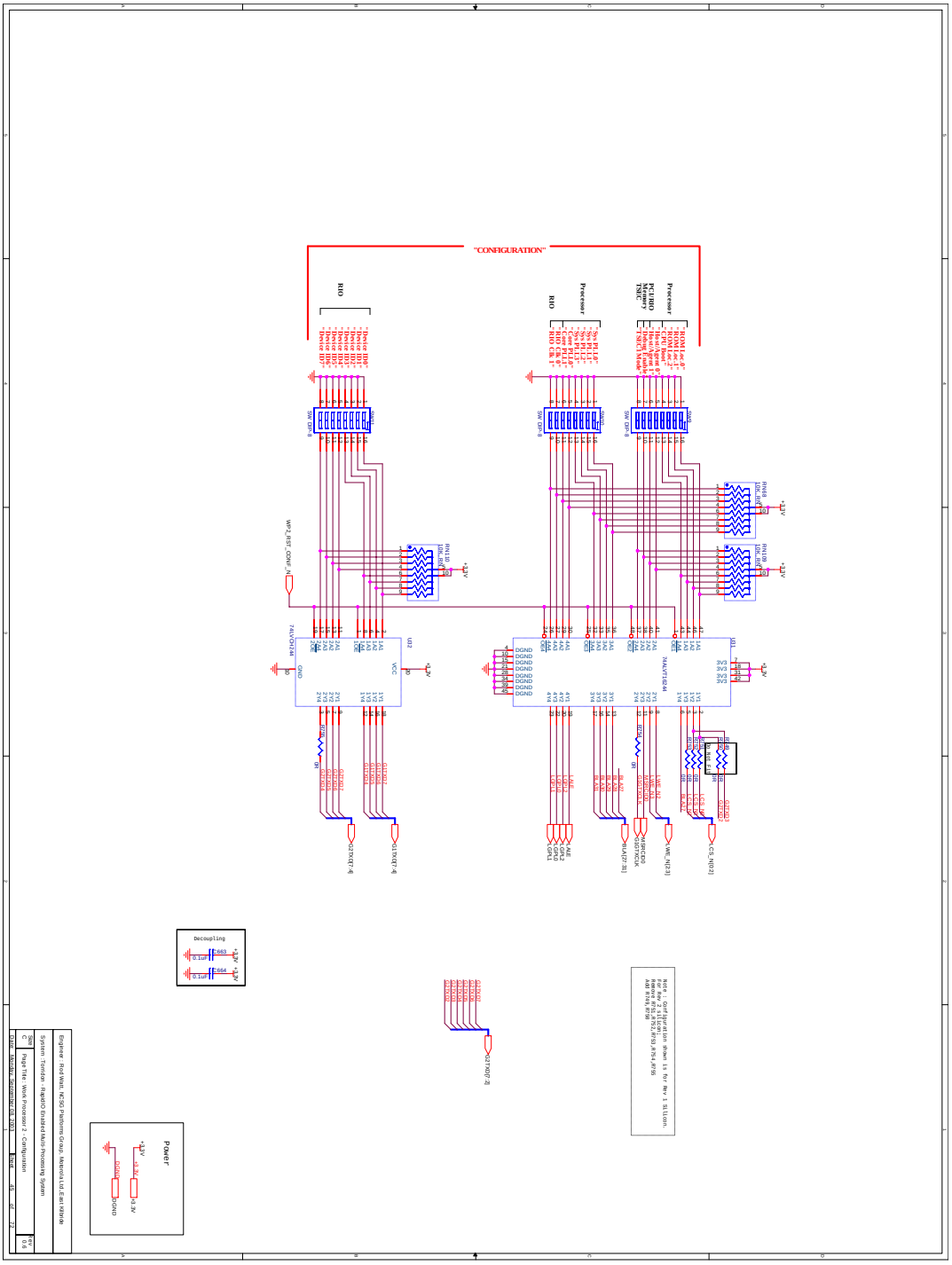


Figure A-43. Work Processor 2—Power On Configuration

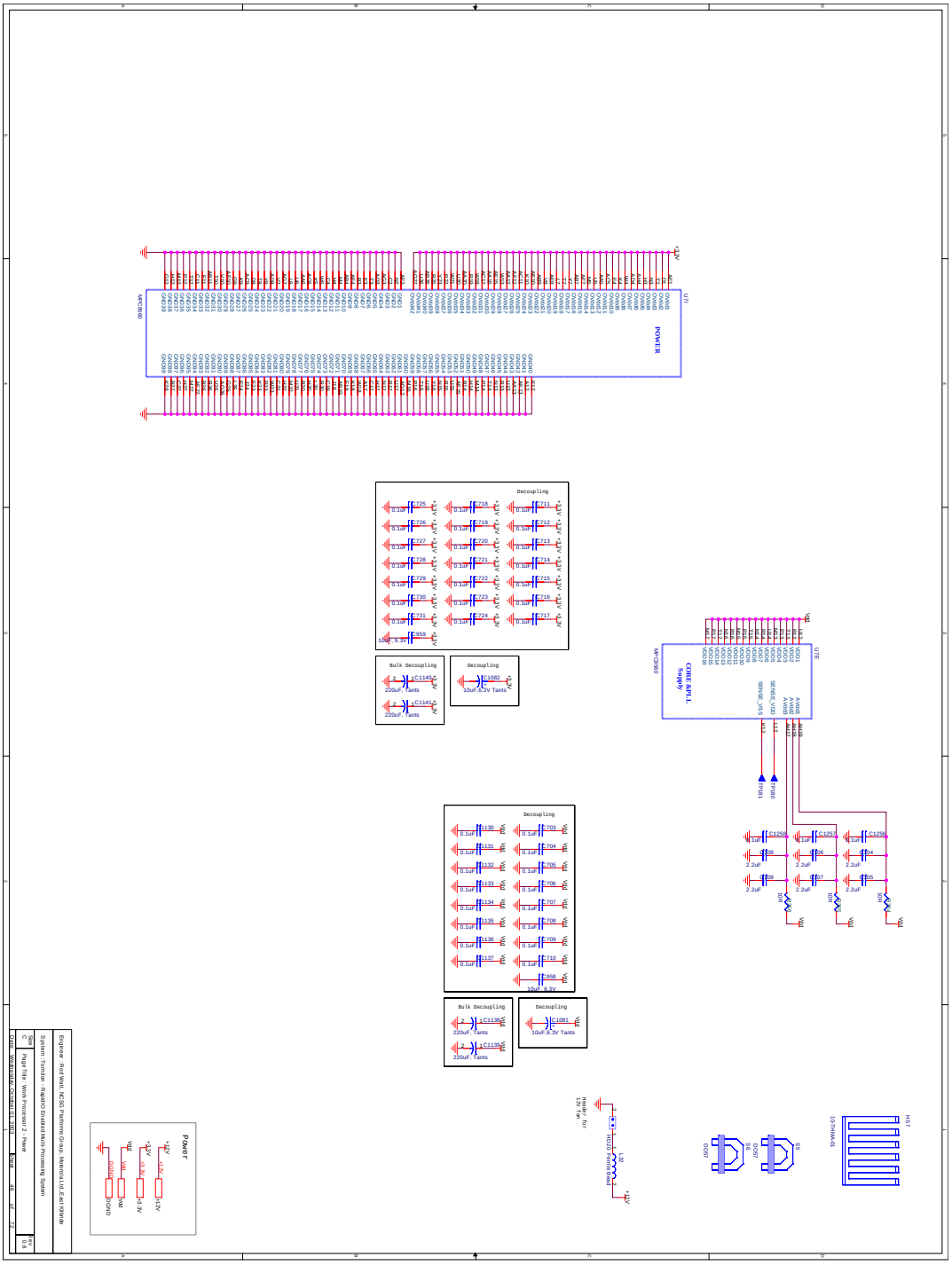


Figure A-44. Work Processor 2—Power

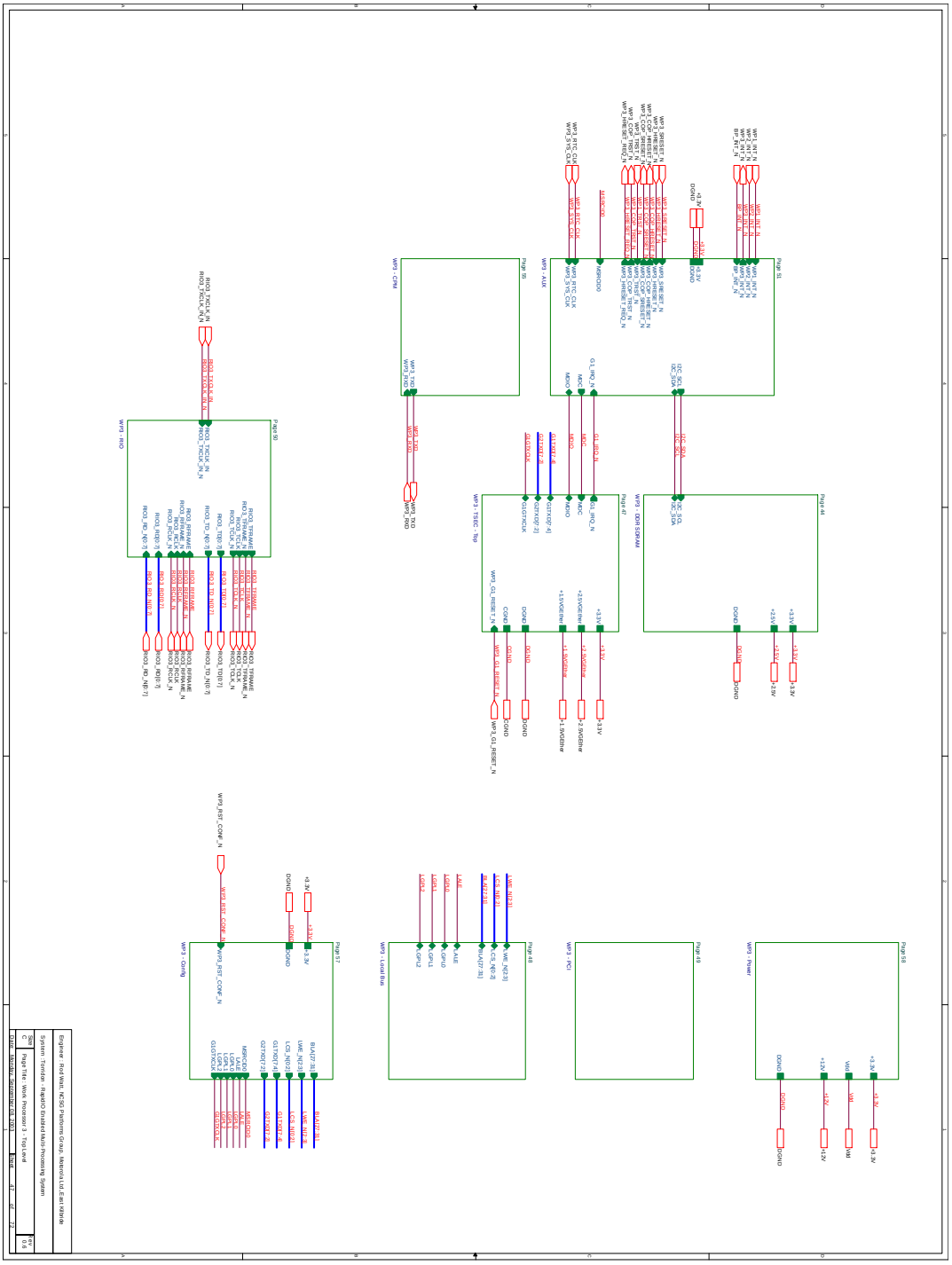


Figure A-45. Work Processor 3—Top Level

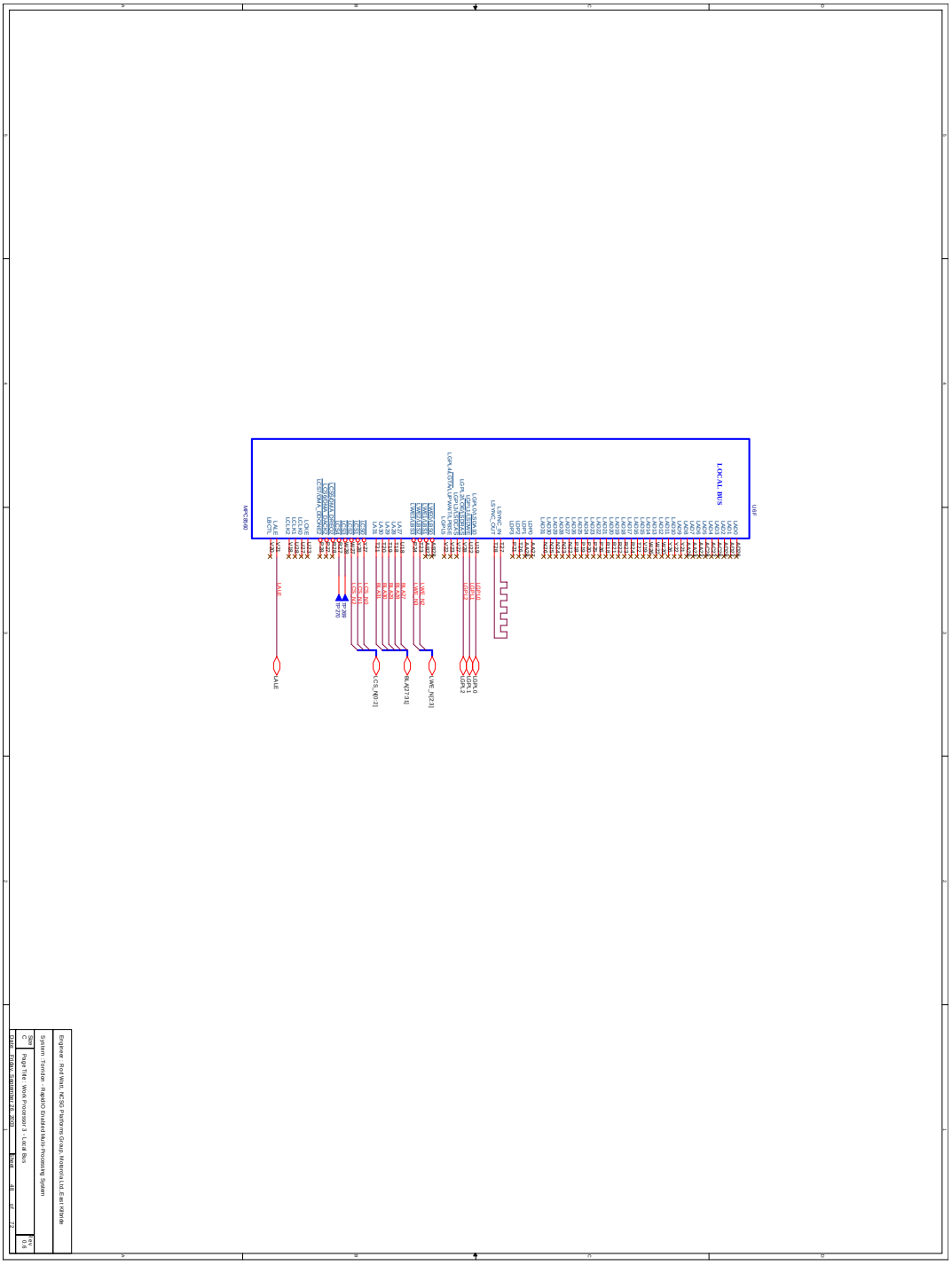


Figure A-46. Work Processor 3—Local Bus

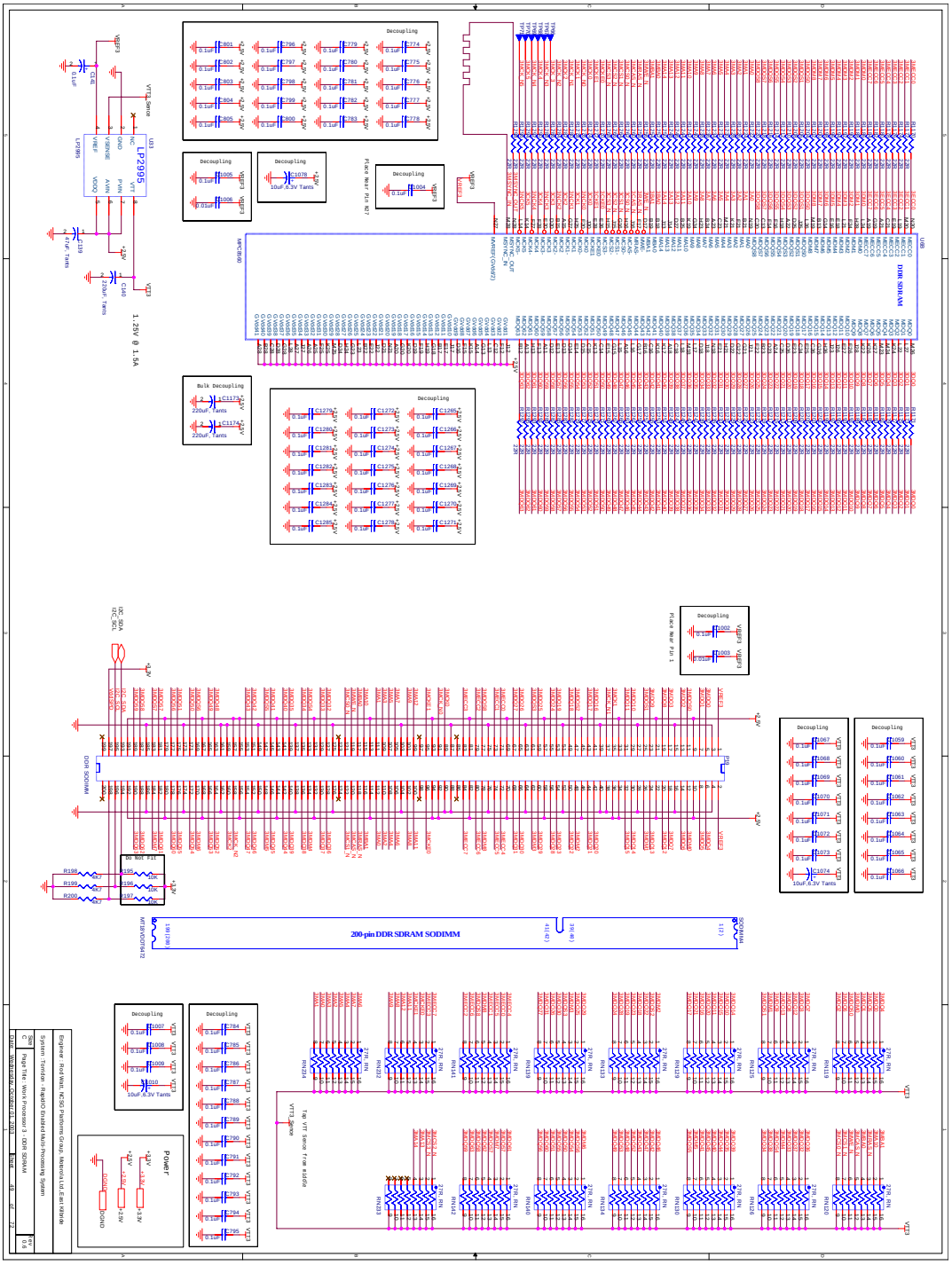


Figure A-47. Work Processor 3—DDR SDRAM

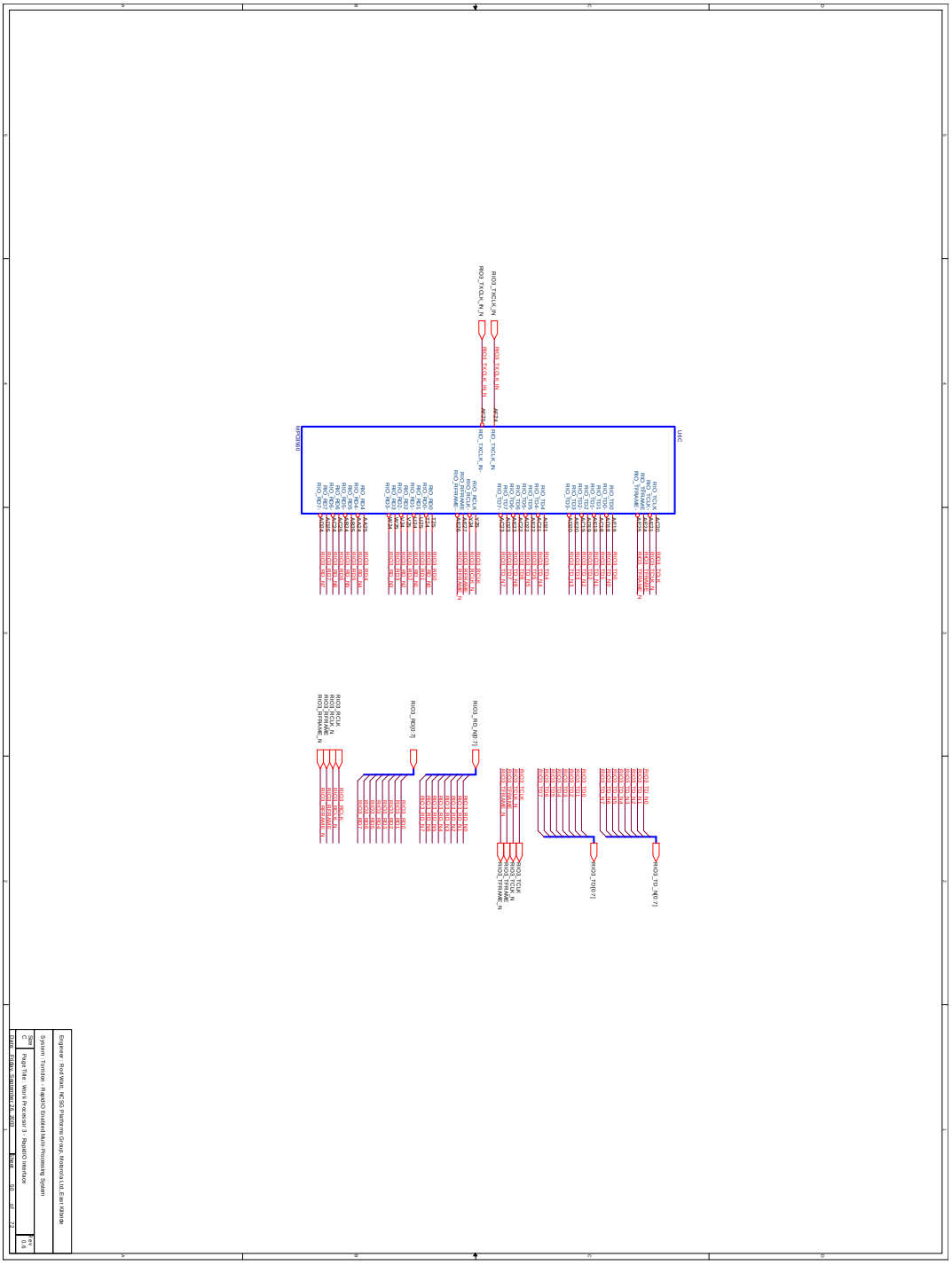


Figure A-48. Work Processor 3—RapidIO Interface

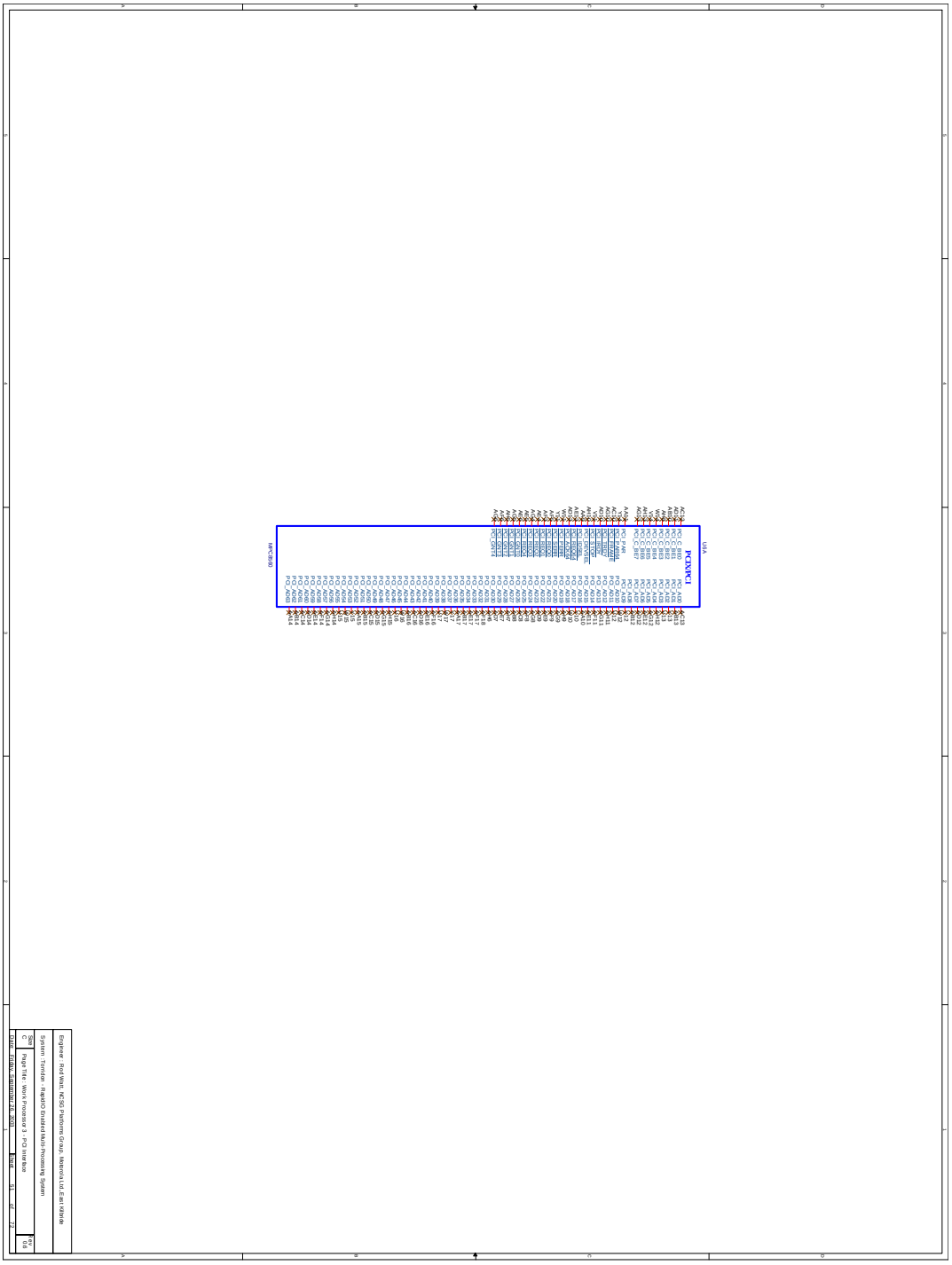


Figure A-49. Work Processor 3—PCI Interface

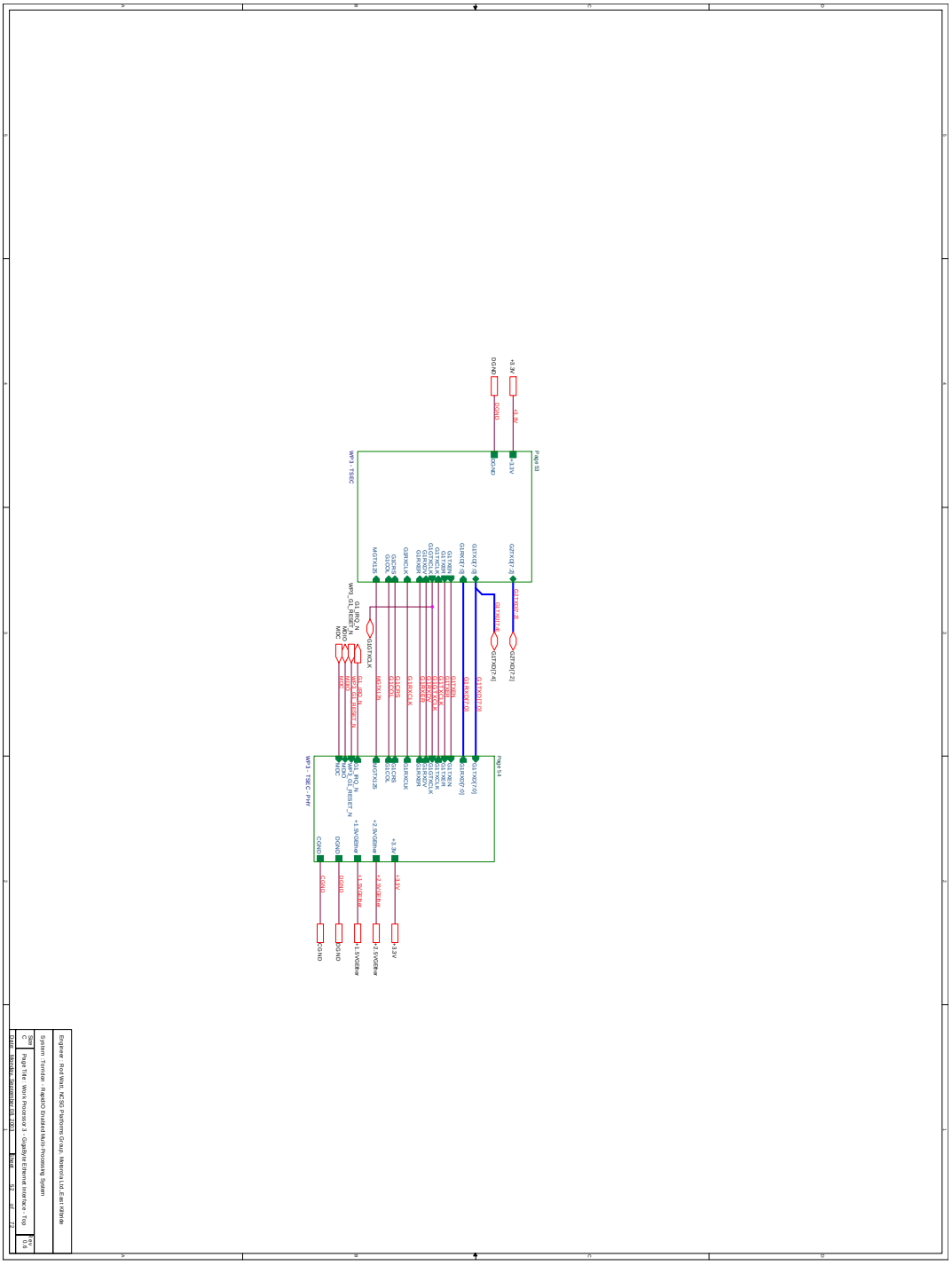


Figure A-50. Work Processor 3—GigaByte Ethernet Interface—Top

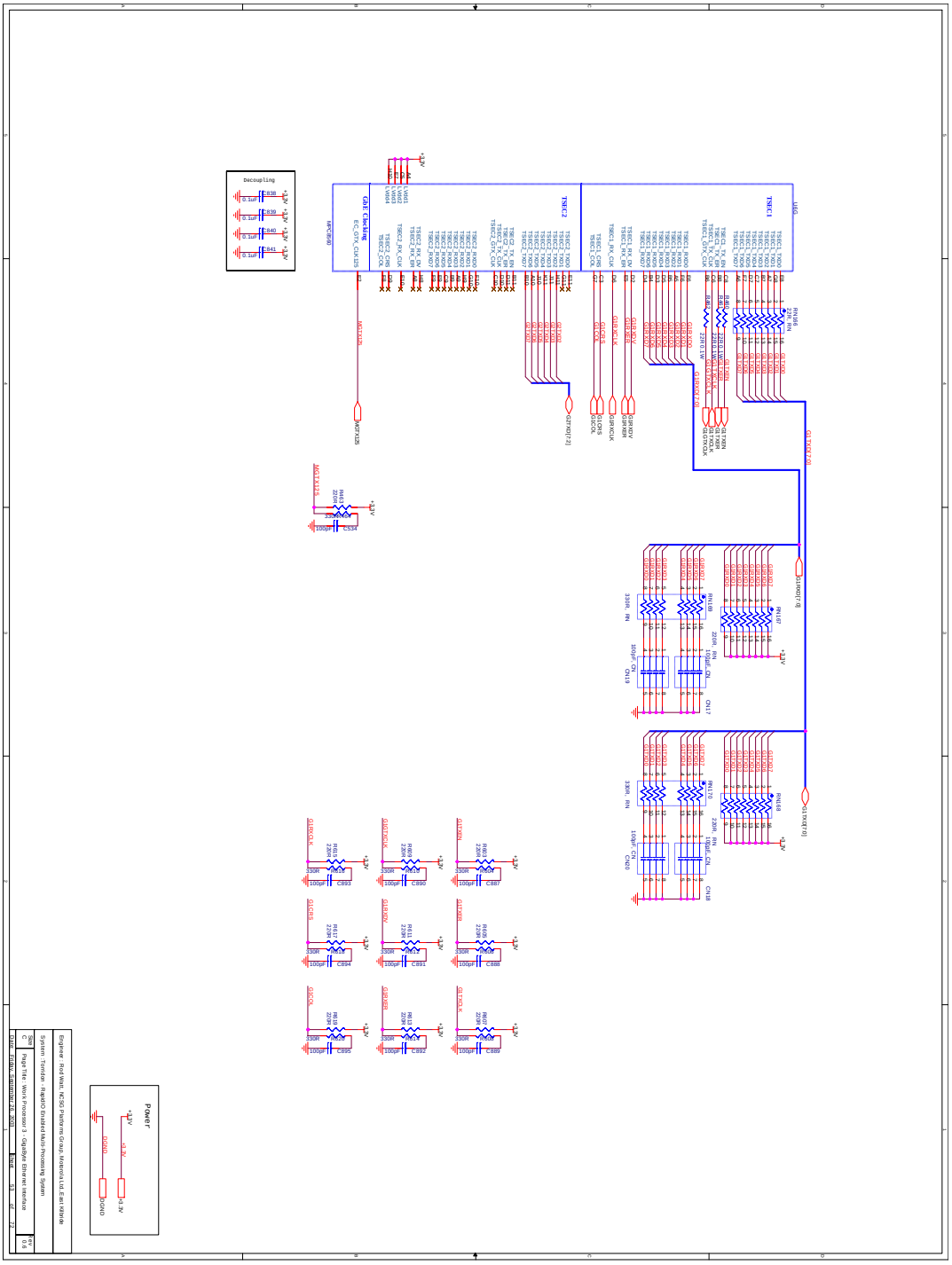


Figure A-51. Work Processor 3—GigaByte Ethernet Interface

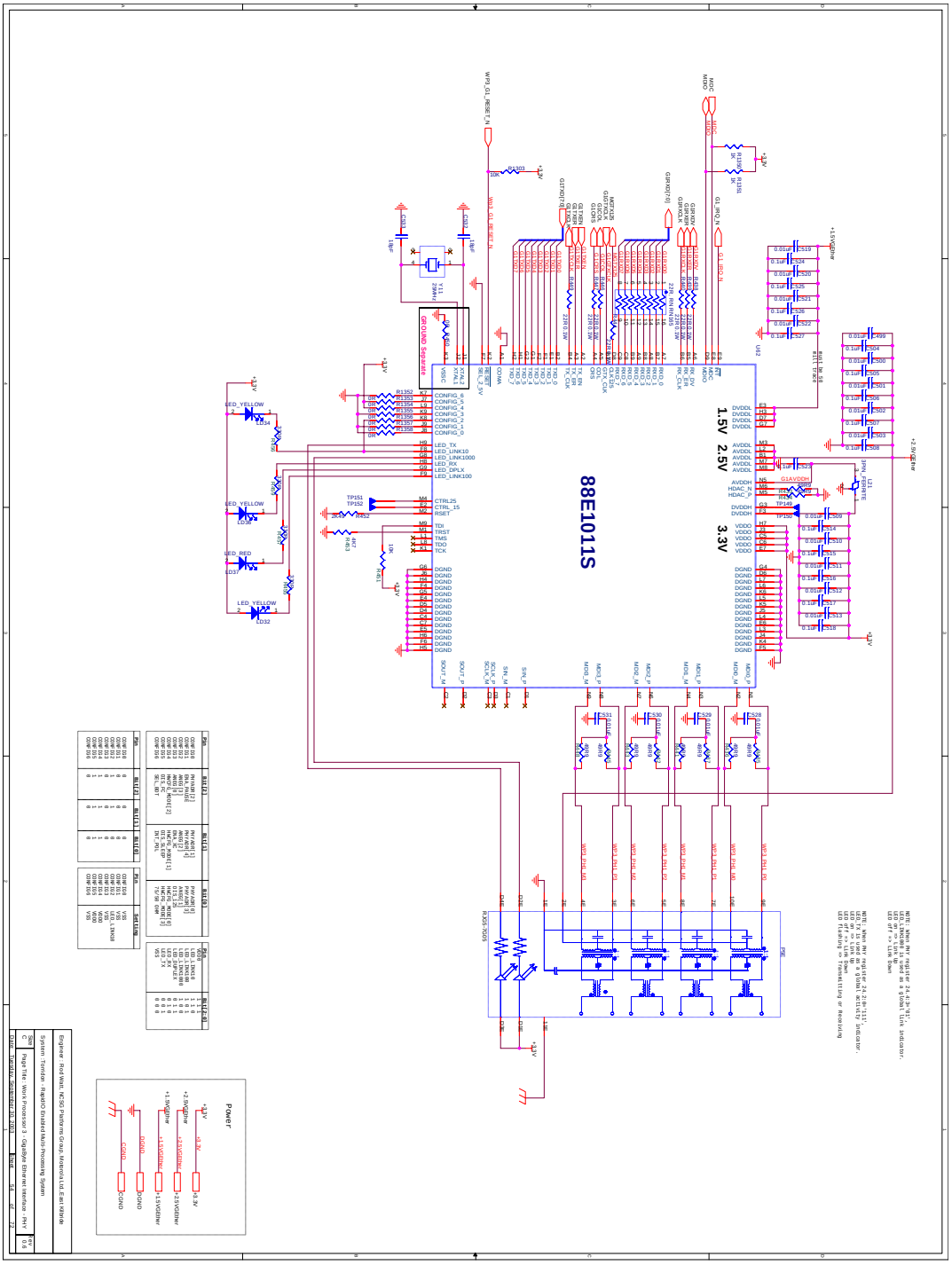


Figure A-52. Work Processor 3—GigaByte Ethernet Interface—PHY

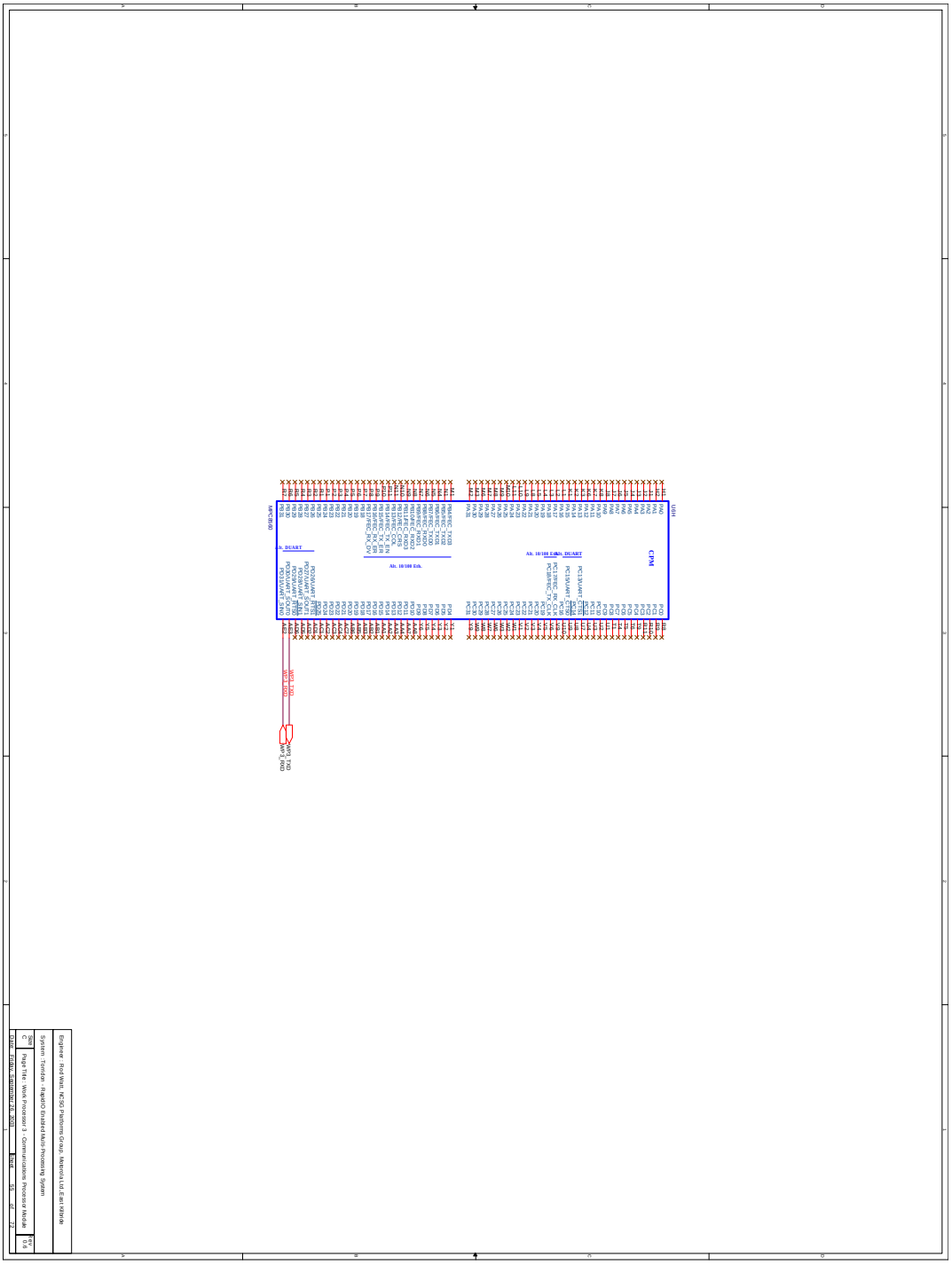


Figure A-53. Work Processor 3—Communications Processor Module

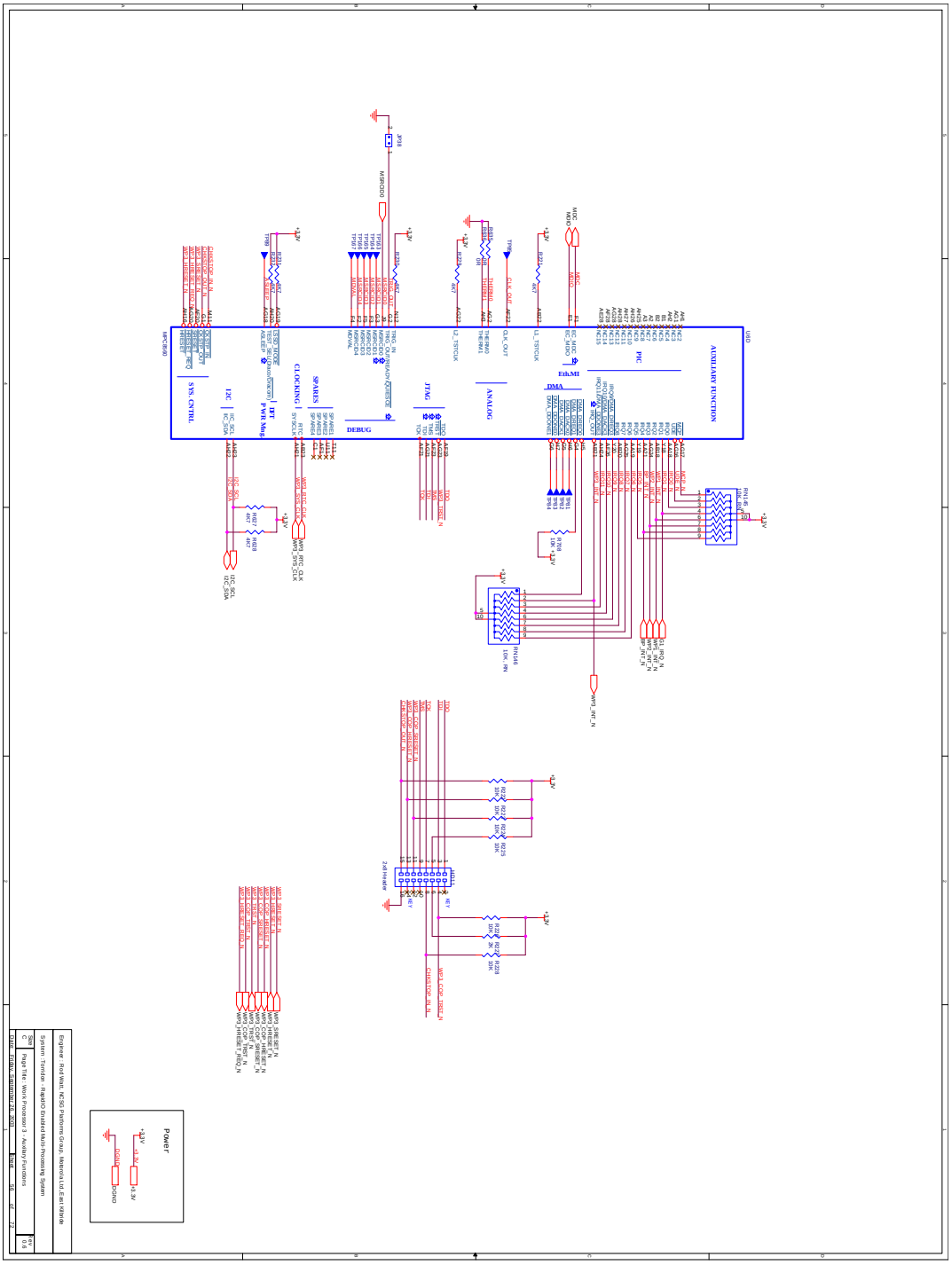


Figure A-54. Work Processor 3—Auxiliary Functions

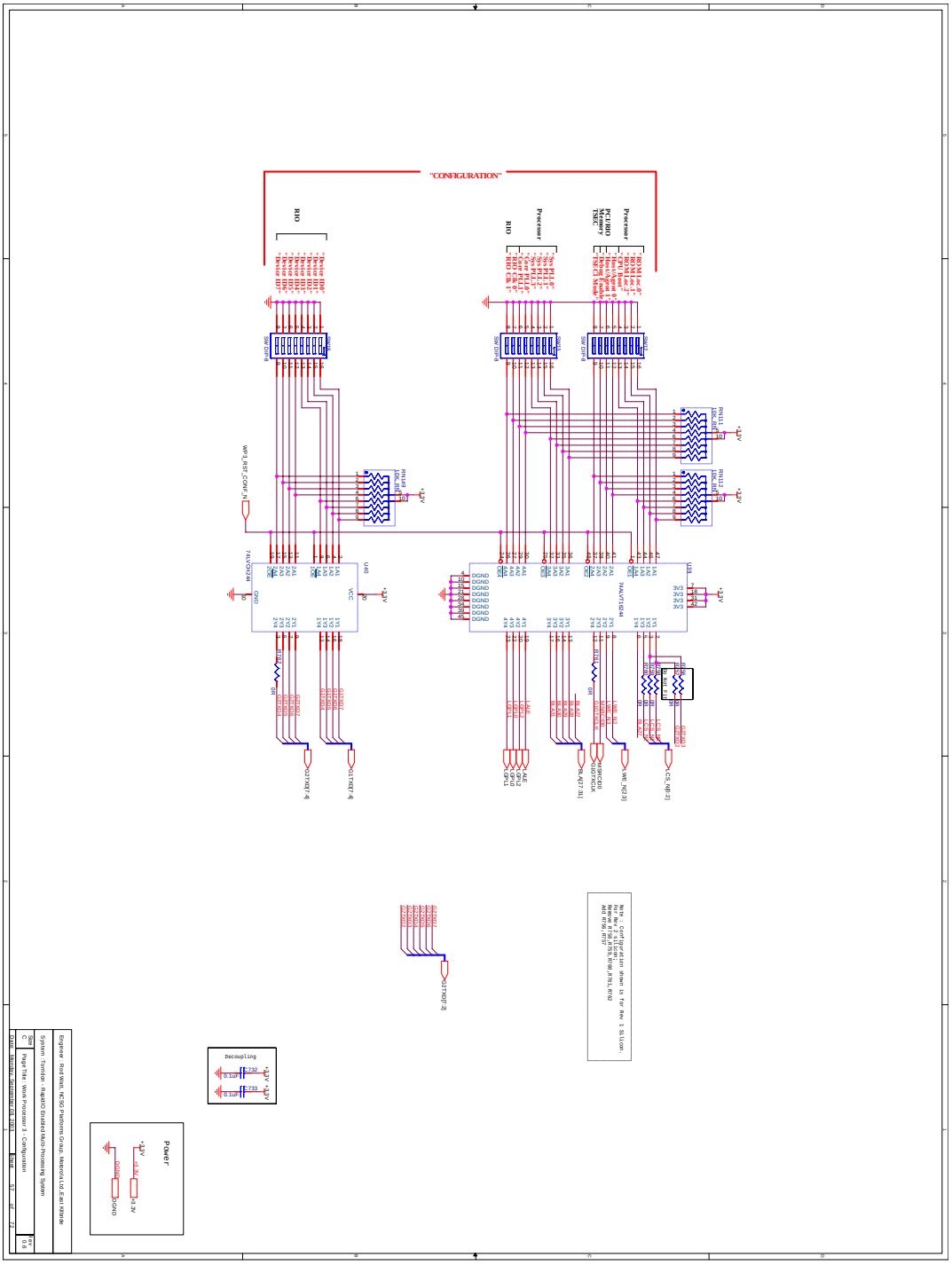


Figure A-55. Work Processor 3—Power On Configuration

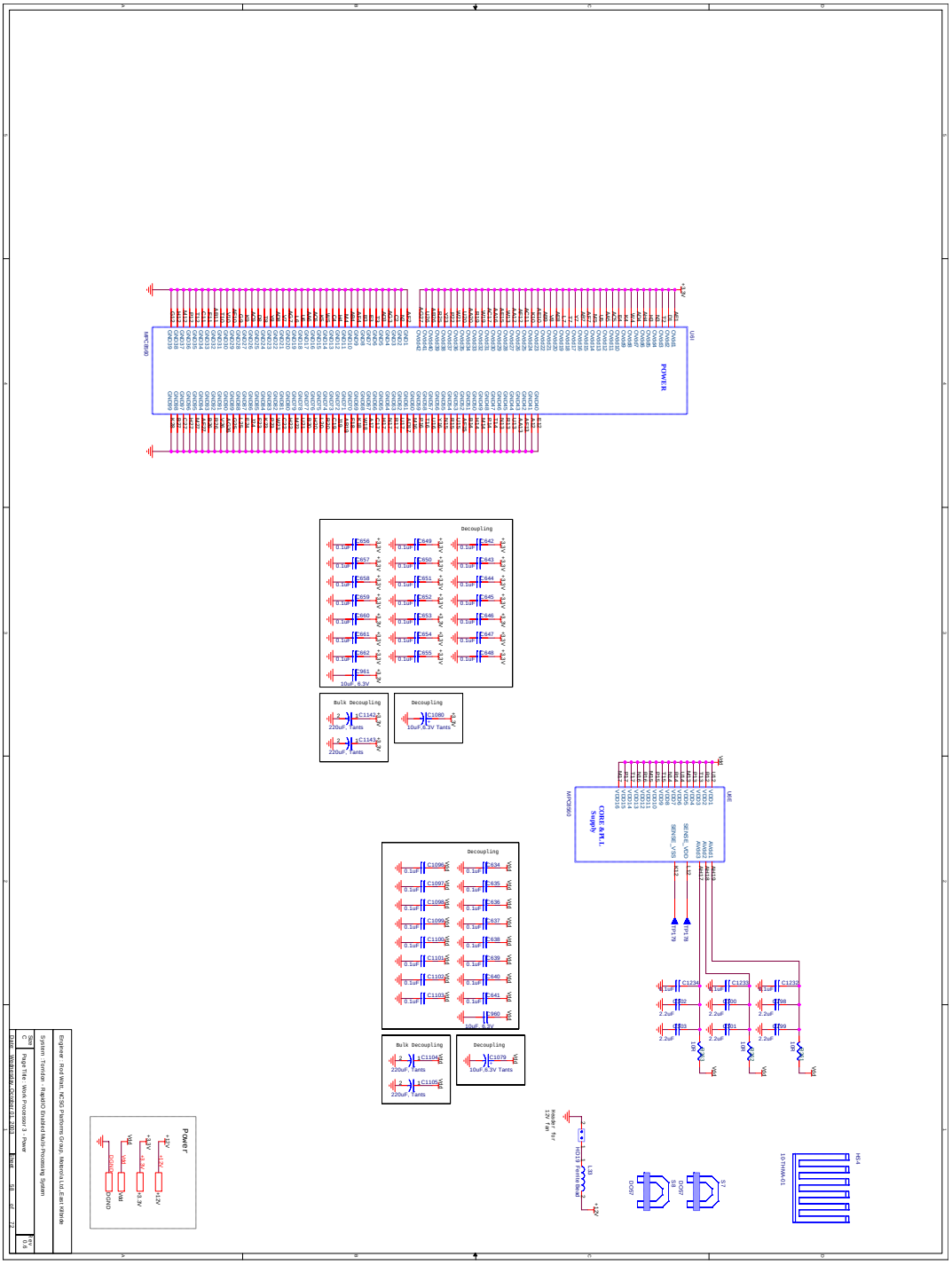


Figure A-56. Work Processor 3—Power

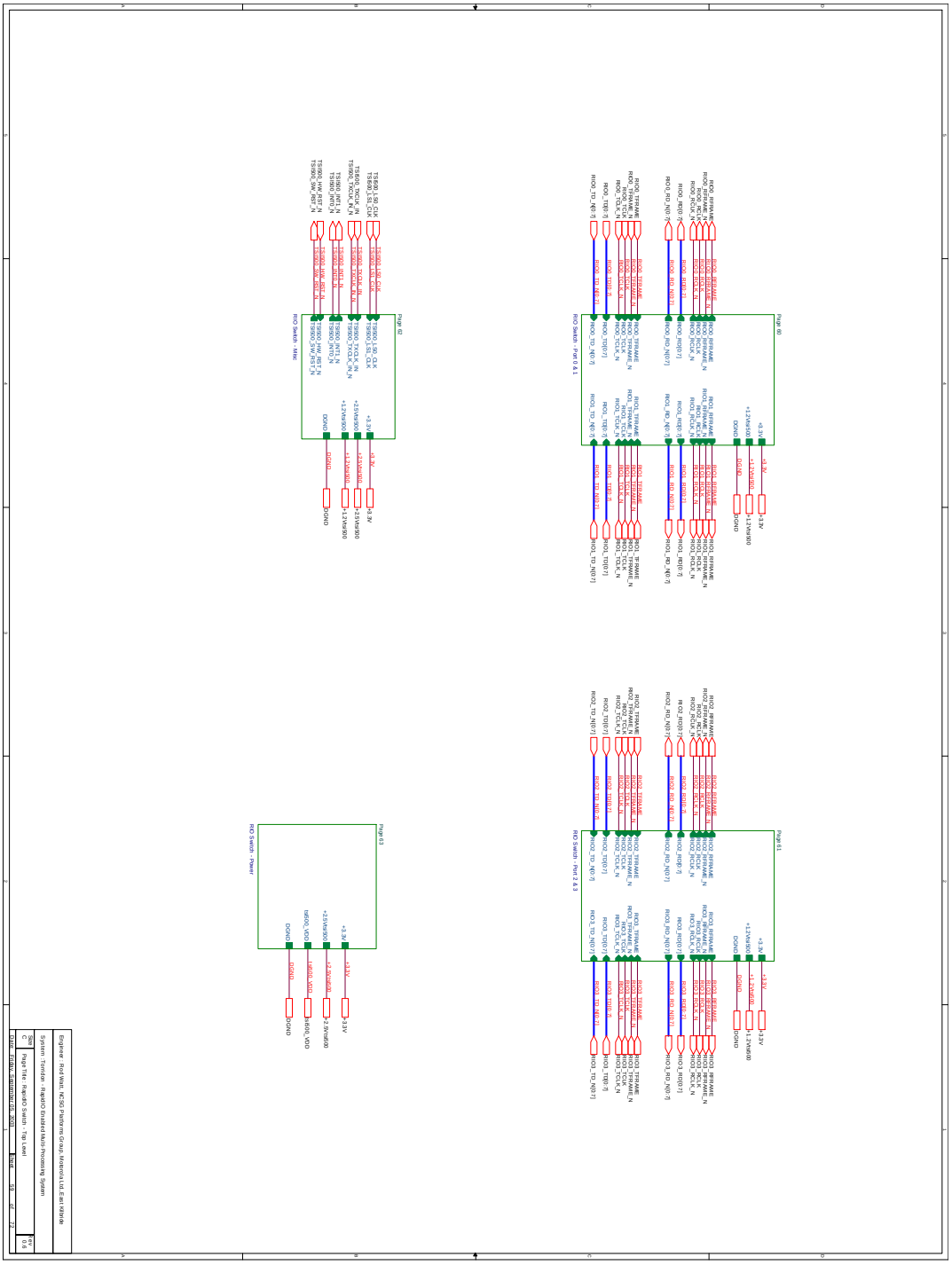


Figure A-57. RapidIO Switch—Top Level

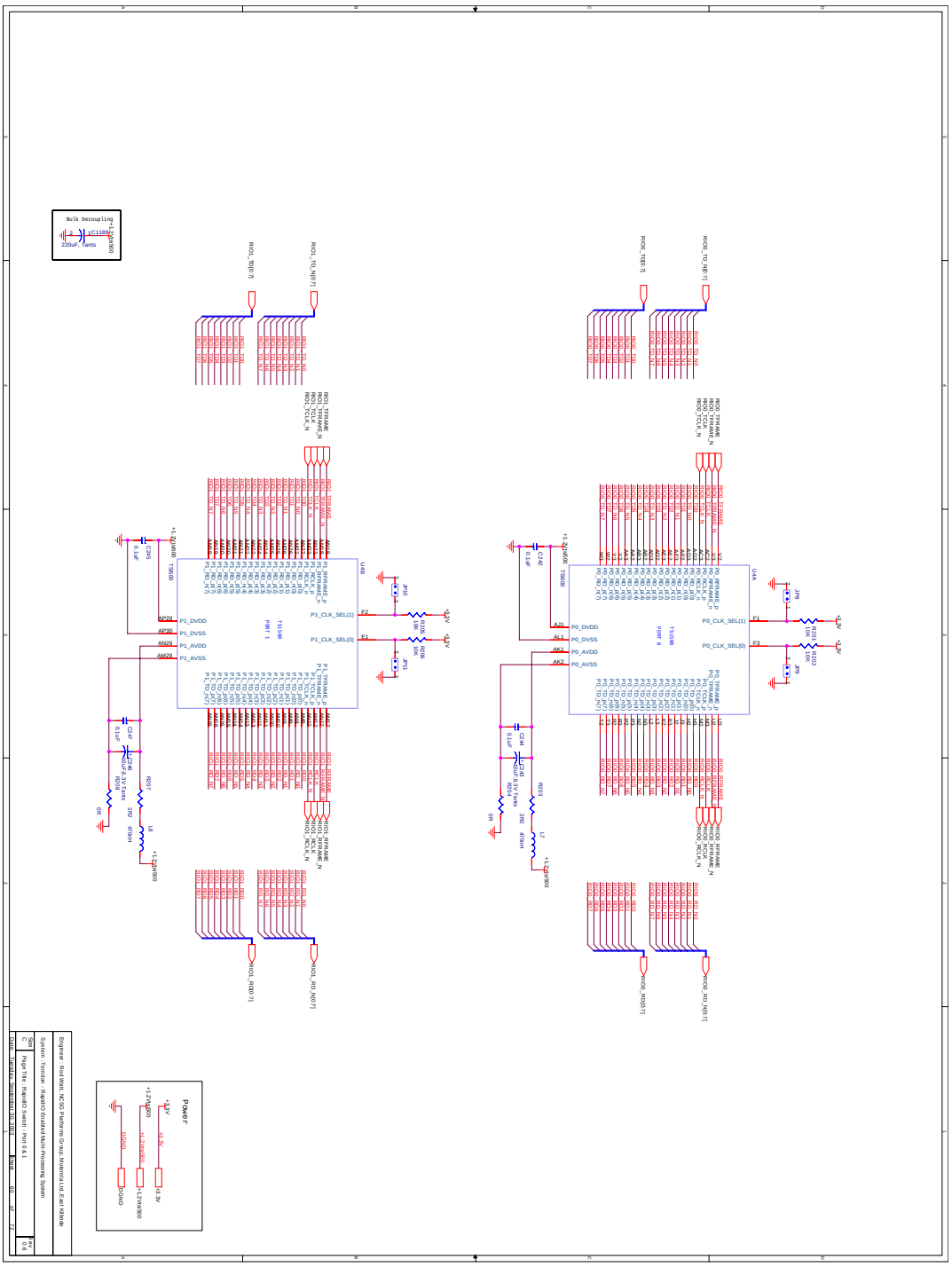


Figure A-58. RapidIO Switch—Ports 0 and 1

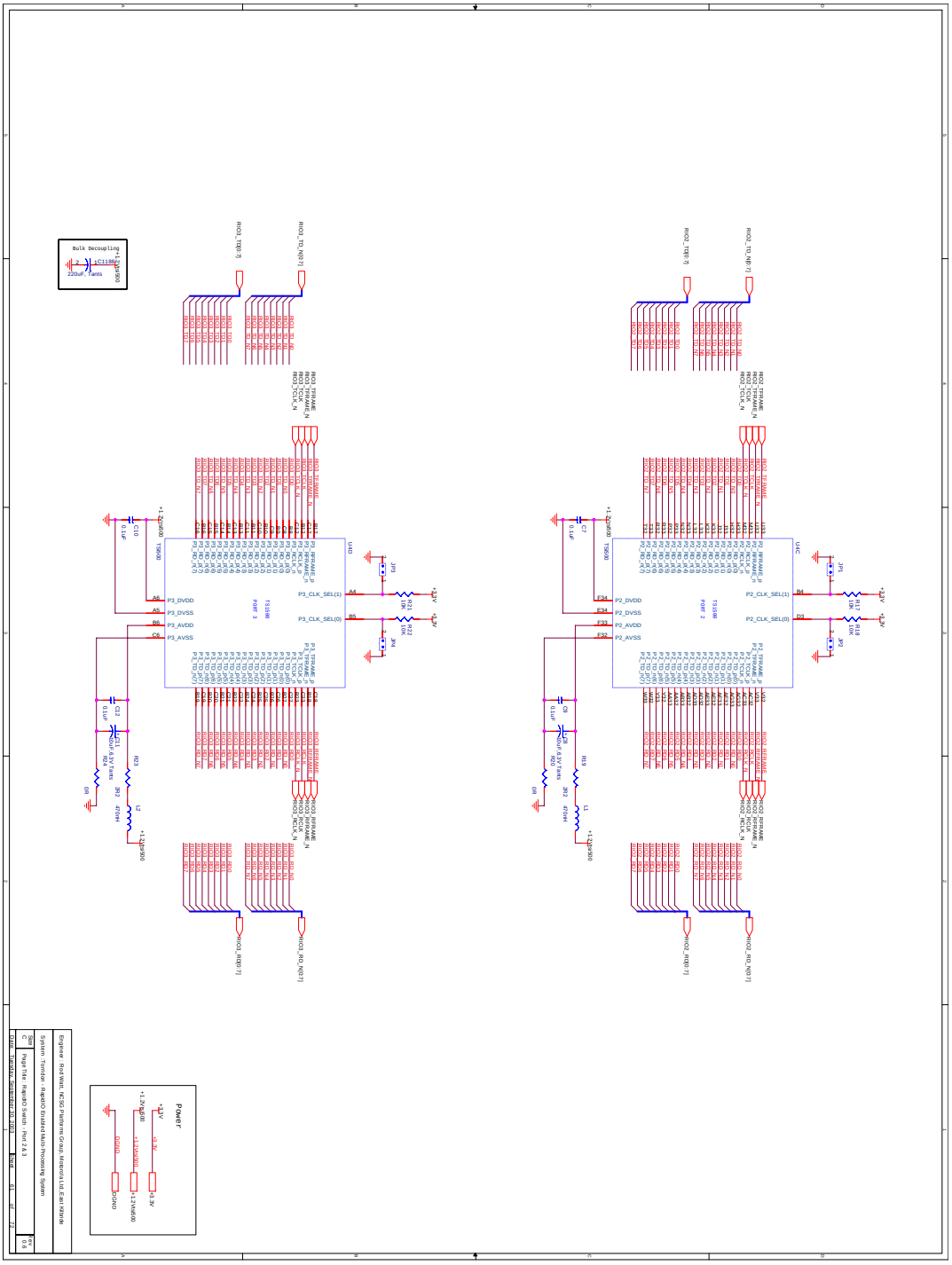


Figure A-59. RapidIO Switch—Ports 2 and 3

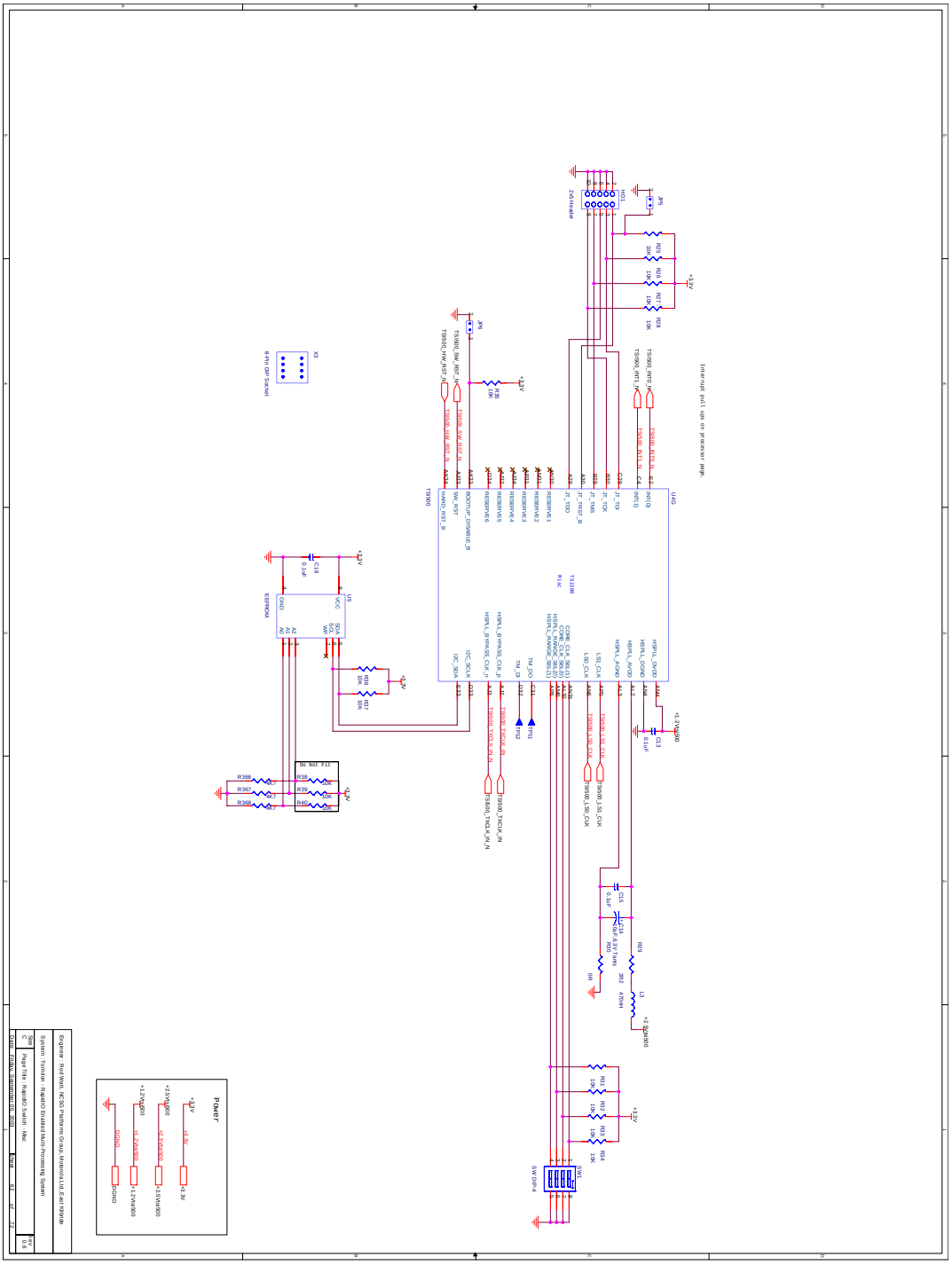


Figure A-60. RapidIO Switch—Misc

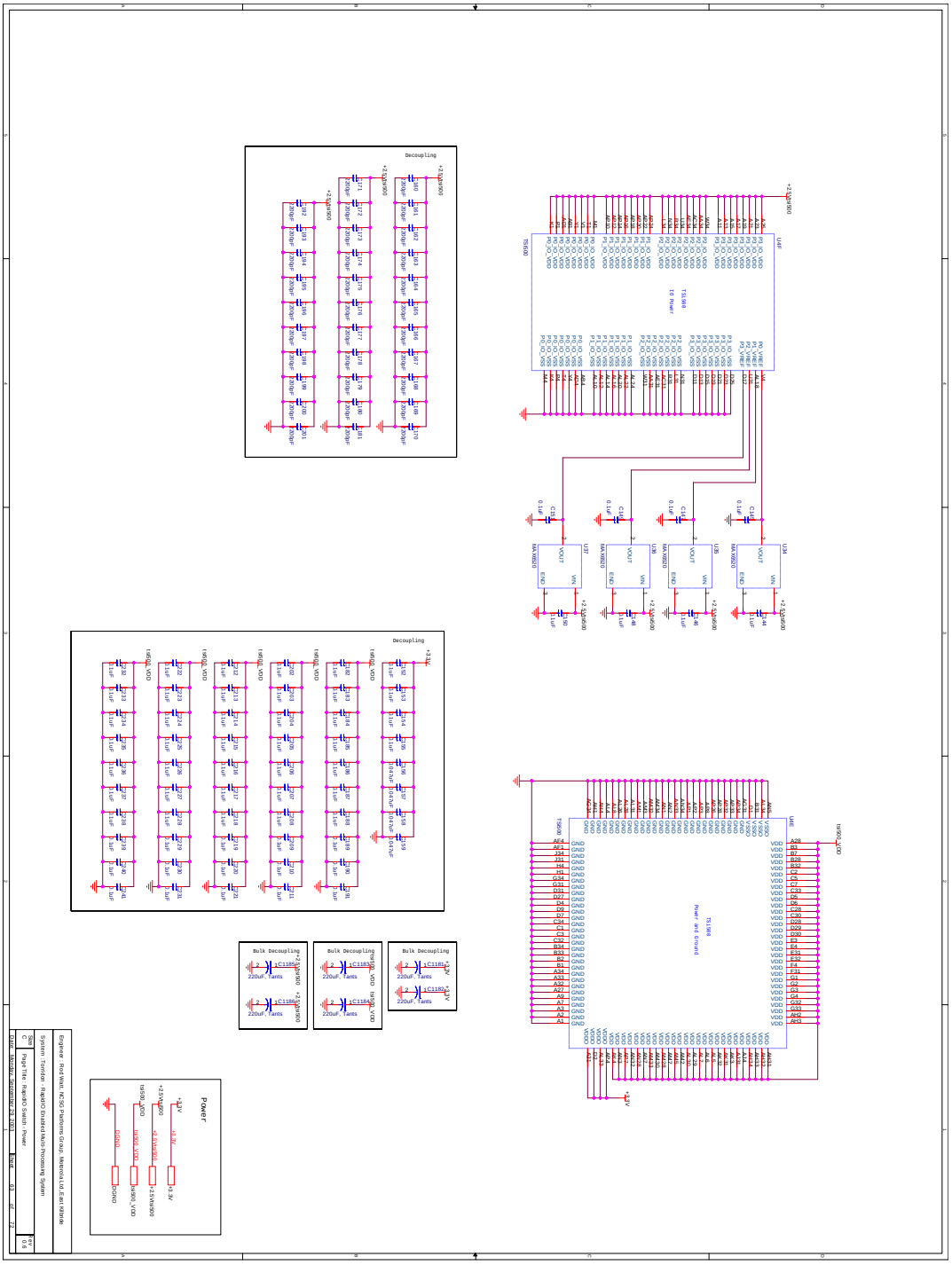


Figure A-61. RapidIO Switch—Power

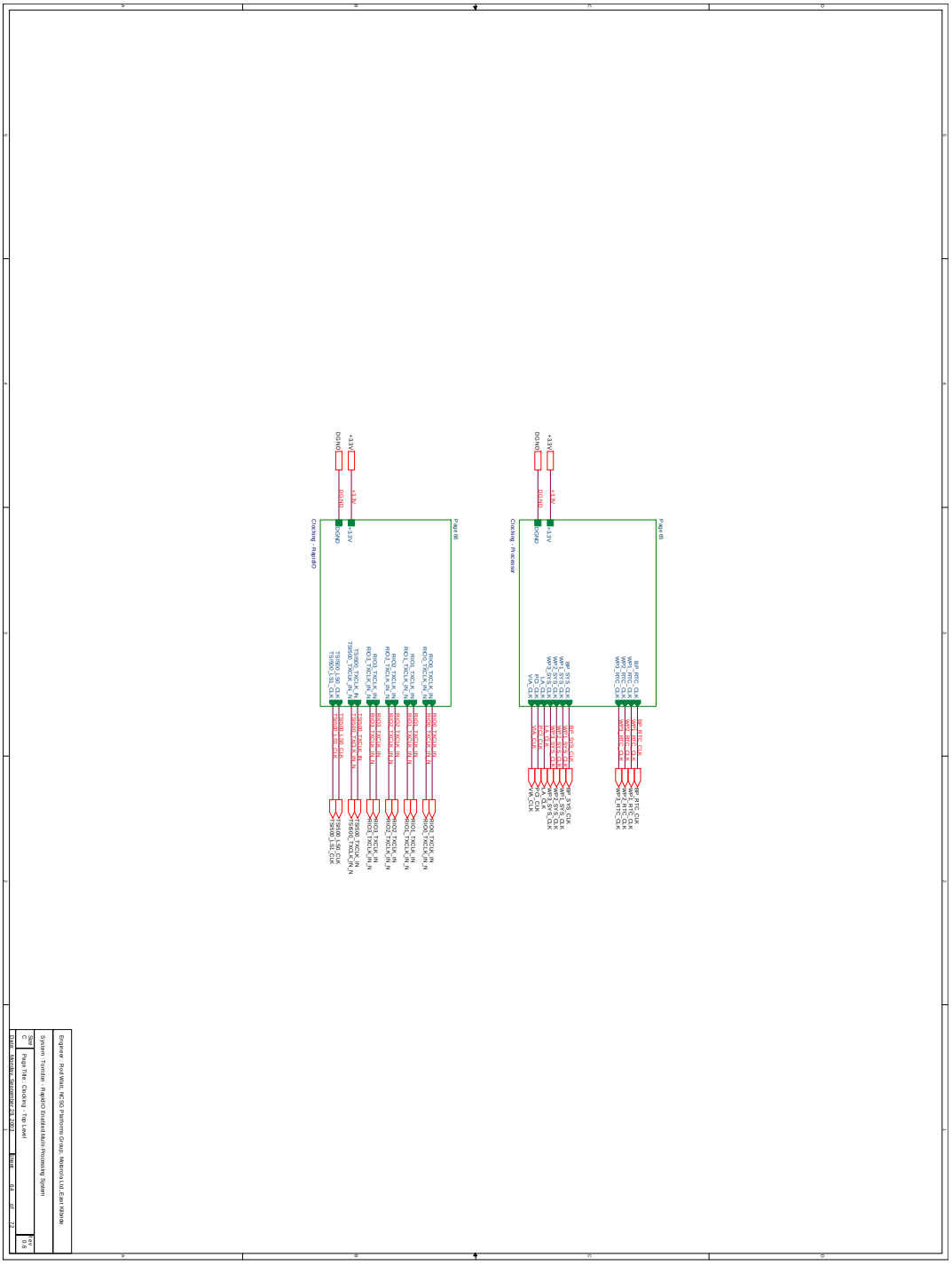


Figure A-62. Clocking—Top Level

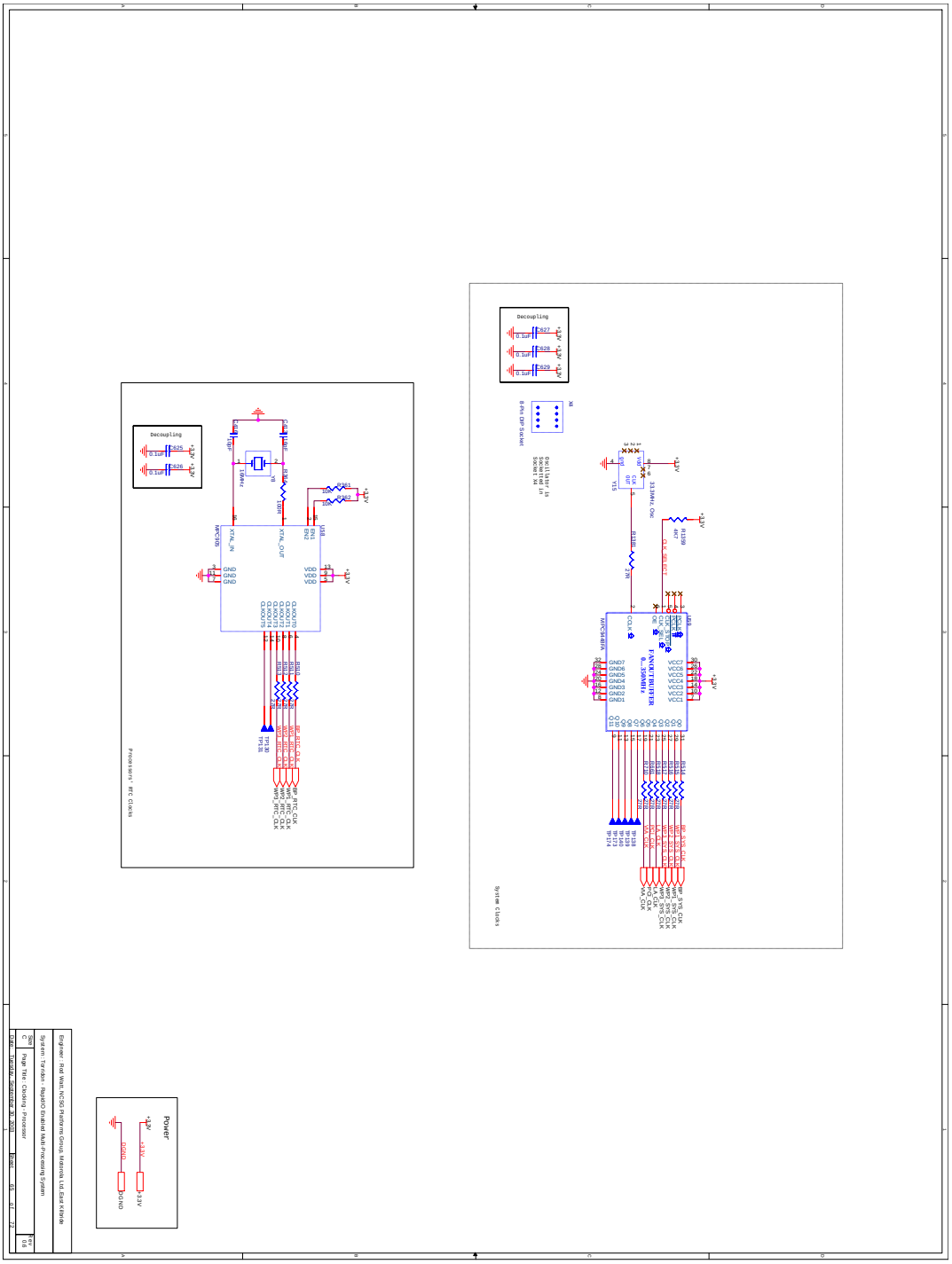


Figure A-63. Clocking—Processor

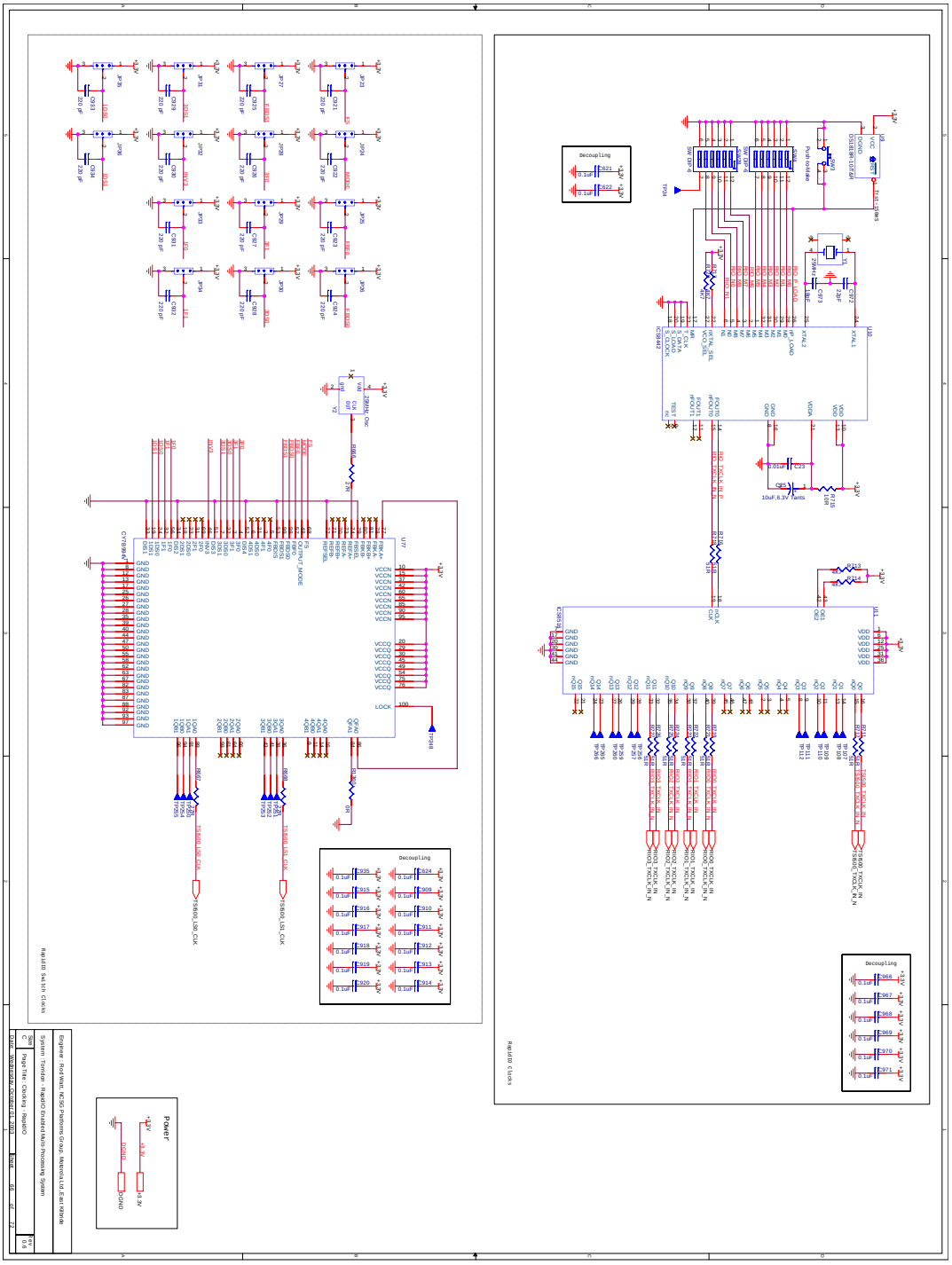


Figure A-64. Clocking—RapidIO

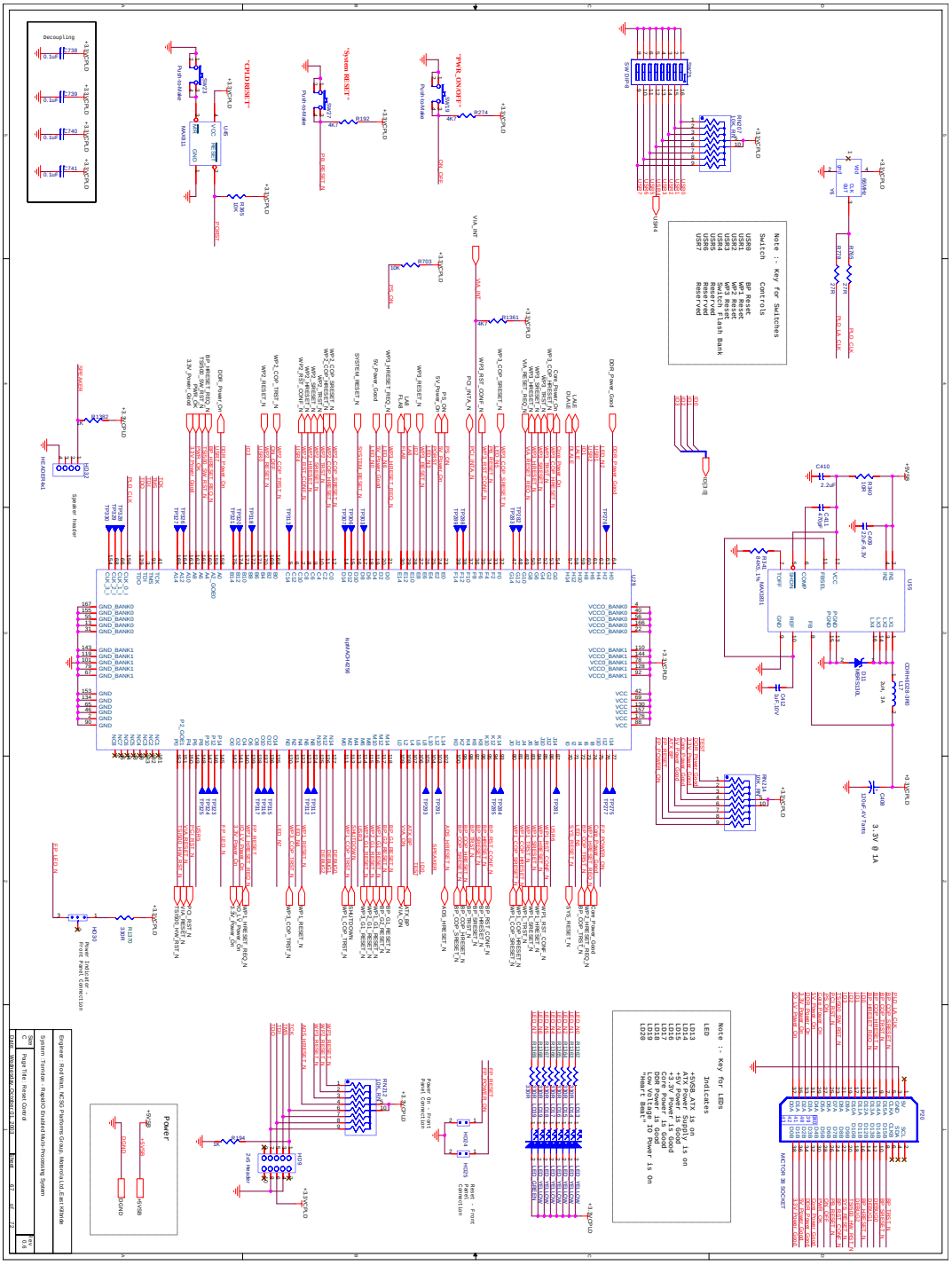


Figure A-65. Reset Control

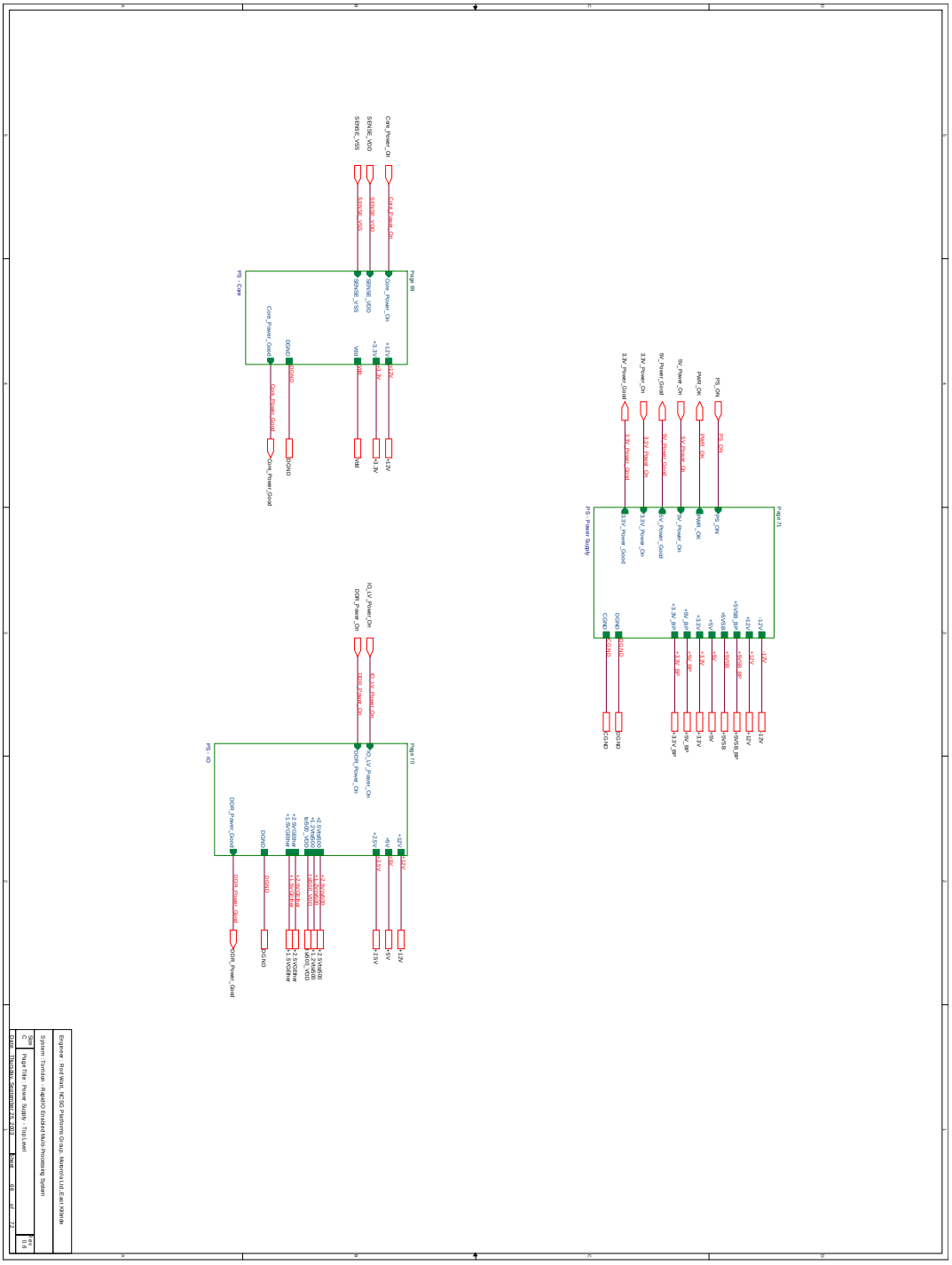


Figure A-66. Power Supply—Top Level

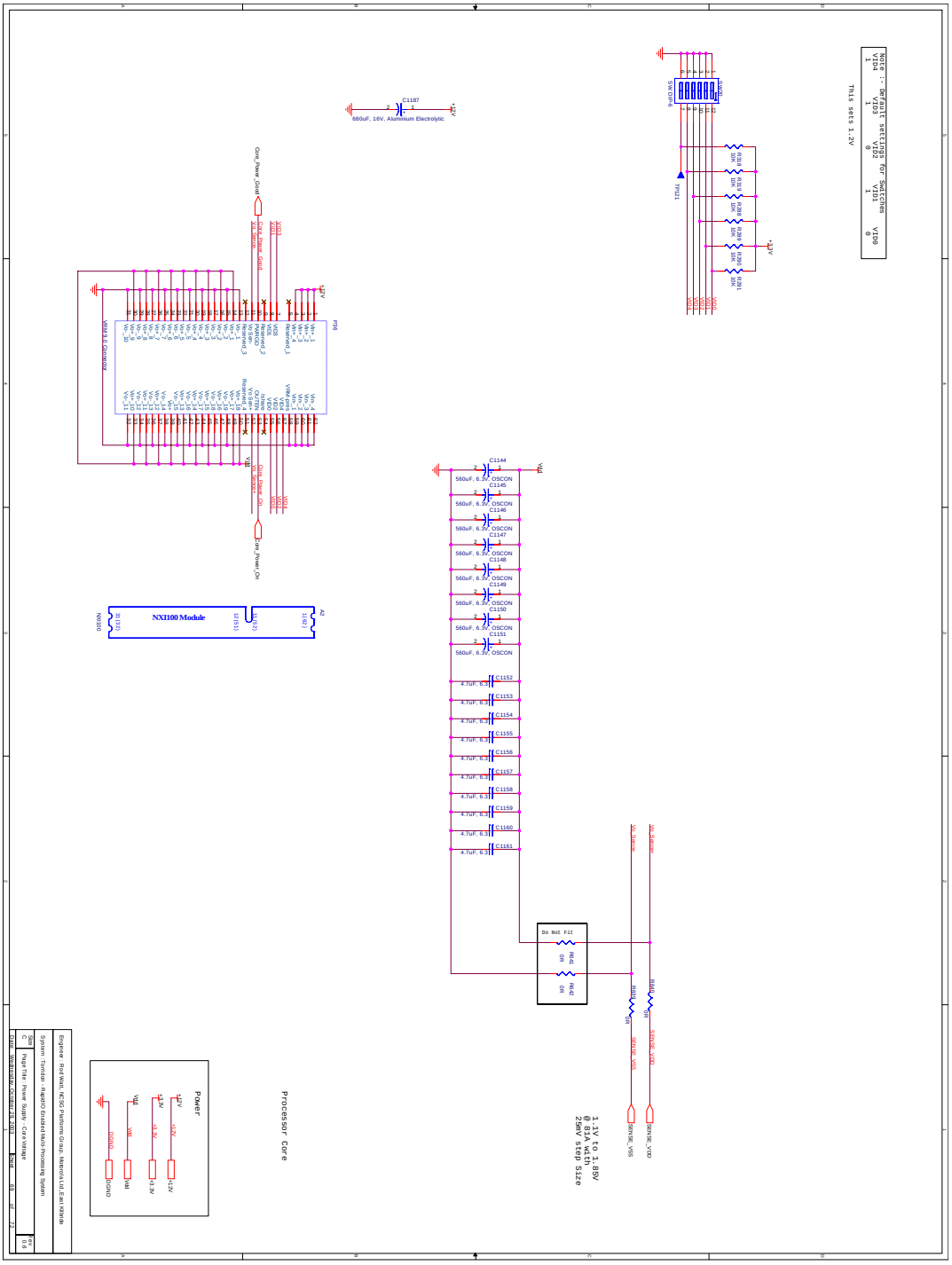


Figure A-67. Power Supply—Core Voltage

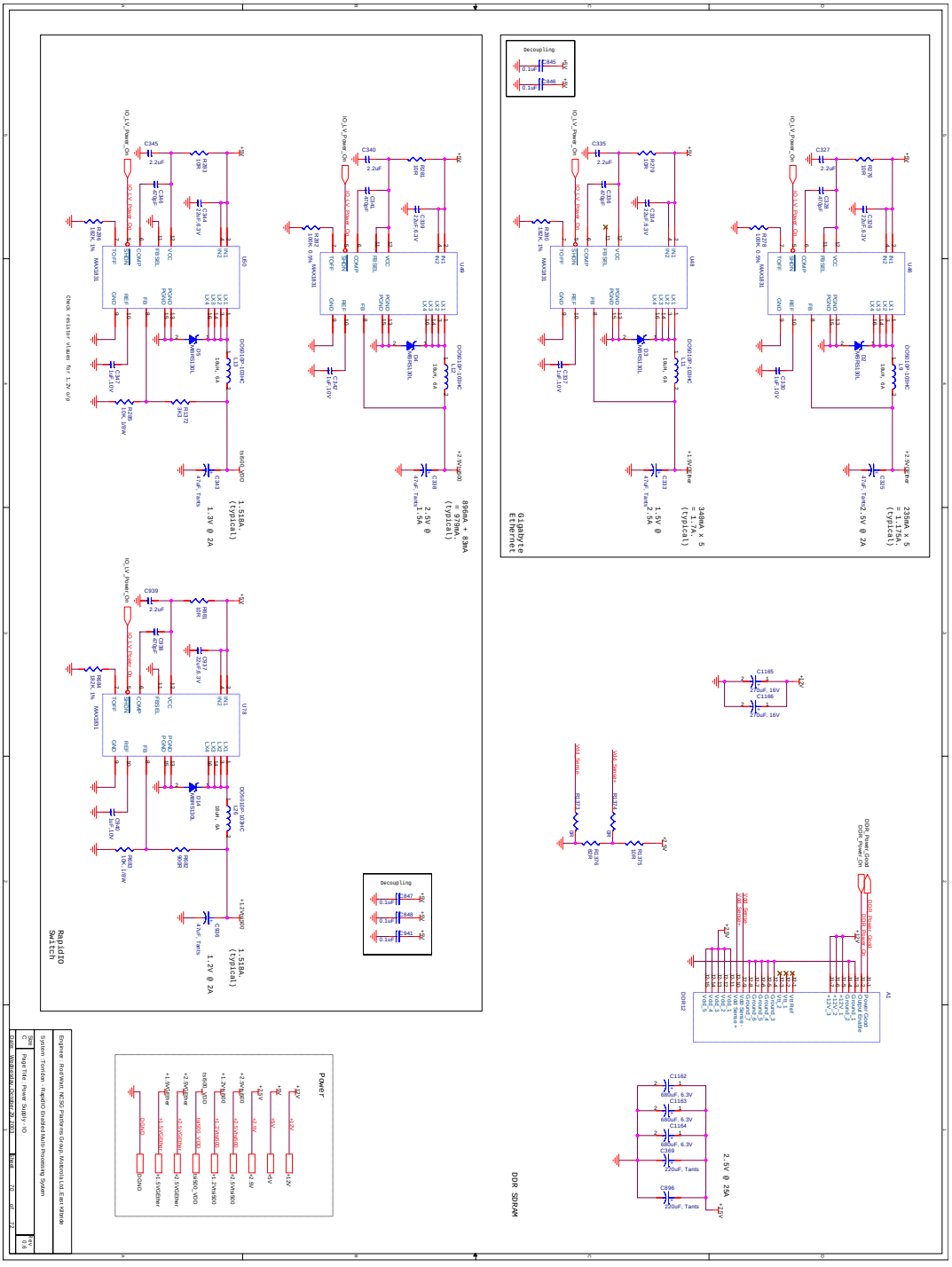


Figure A-68. Power Supply—IO Voltages

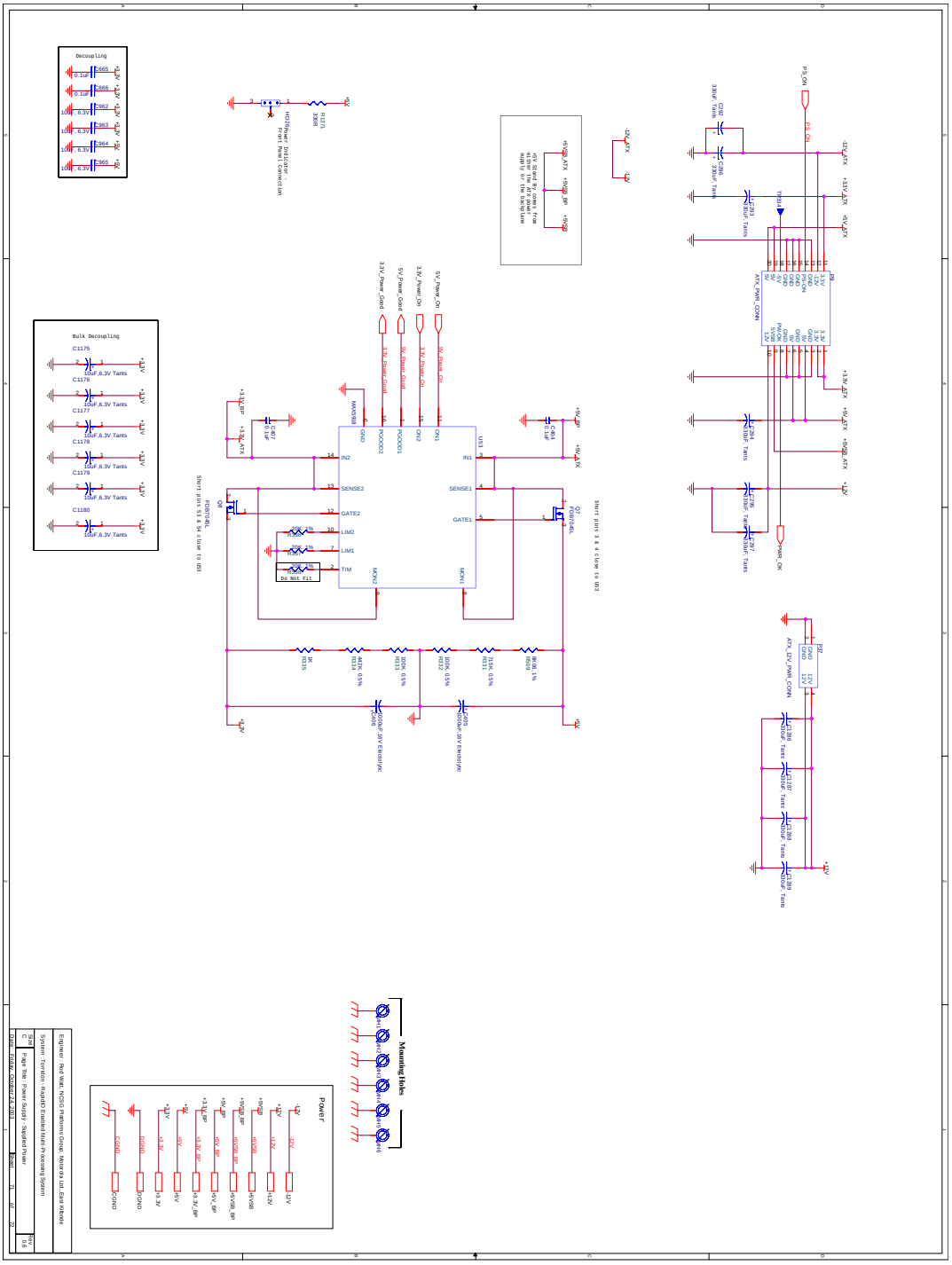


Figure A-69. Power Supply—Supplied Power

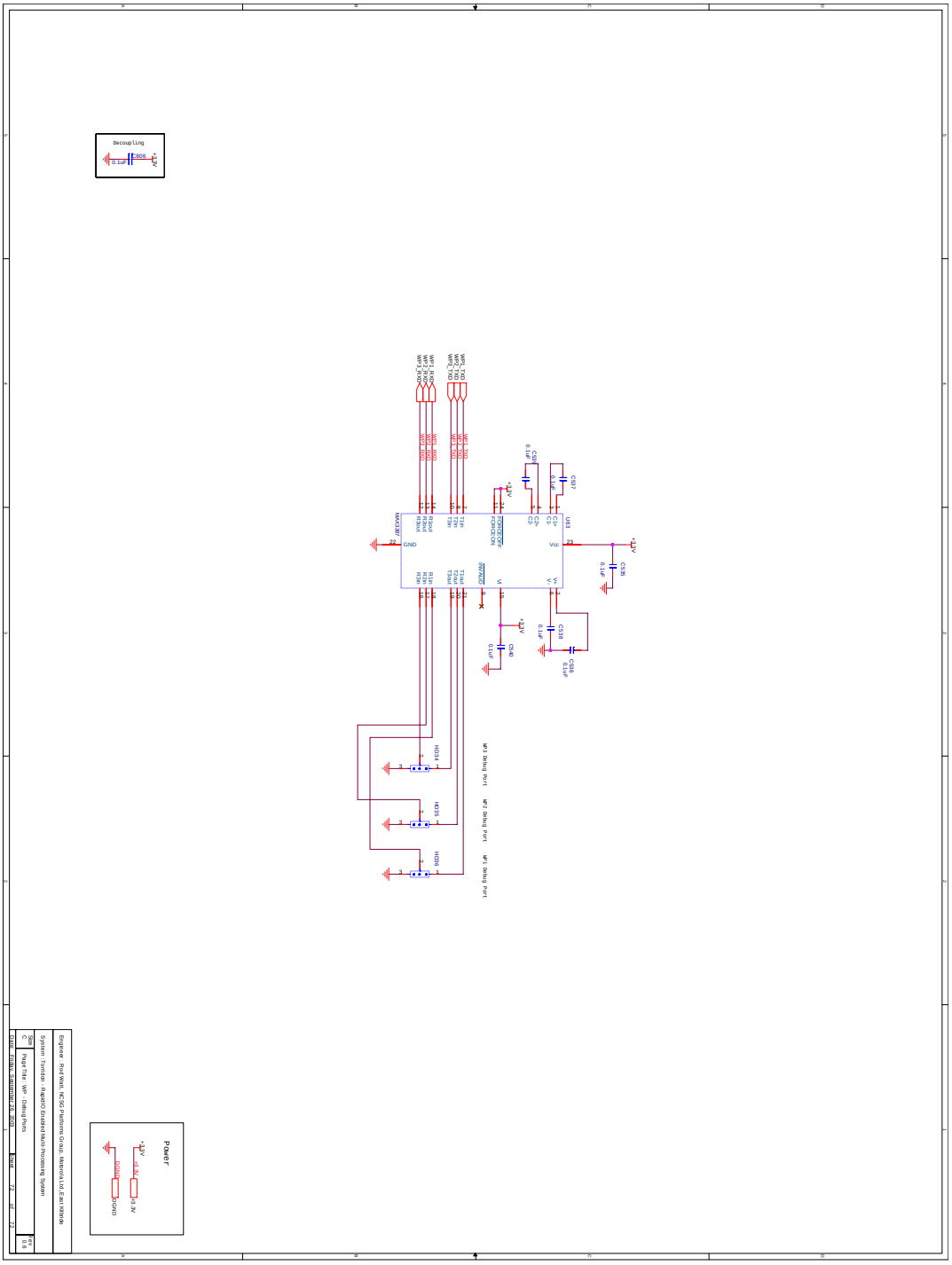


Figure A-70. WP—Debug Ports

Appendix B
Revision History

Table B-1. Revision History

Revision	Release Date	Changes
0.1	12/2004	Modified footer on front cover
0	11/2004	Initial release