NXP Semiconductors
User's Guide

Document Number: PCIECGFIMX7DUG
Rev. 0, 02/2017

PCIe® Certification Guide for i.MX 7Dual

1. Introduction

This document provides a description of the procedures, tools, and criteria for the PCI Express® (PCIe) Gen1 and Gen2 electrical compliance test for i.MX 7Dual.

Contents

2. Test equipment

2.1. Test board

The test is performed on the MCIMX7D EVK board.

2.2. Measurement equipment

This equipment is used to measure the signal quality:

- Oscilloscope: Agilent® DSO91304.
- Cables and adapters:
  - Two Rosenberger® SMP-SMP cables P/N: 71L-19K2-19K2-00305C.
  - Four Agilent SMA-SMP cables P/N: N4235-61602.
  - Four Agilent BNC connectors P/N:54855-67604.
- Test fixture: CLB3.0 X1/X16.
- Mini-PCIe cover for the PCIe board.

Figure 1. SMP-SMP cable

Figure 2. SMA-SMP cable

Figure 3. BNC connector

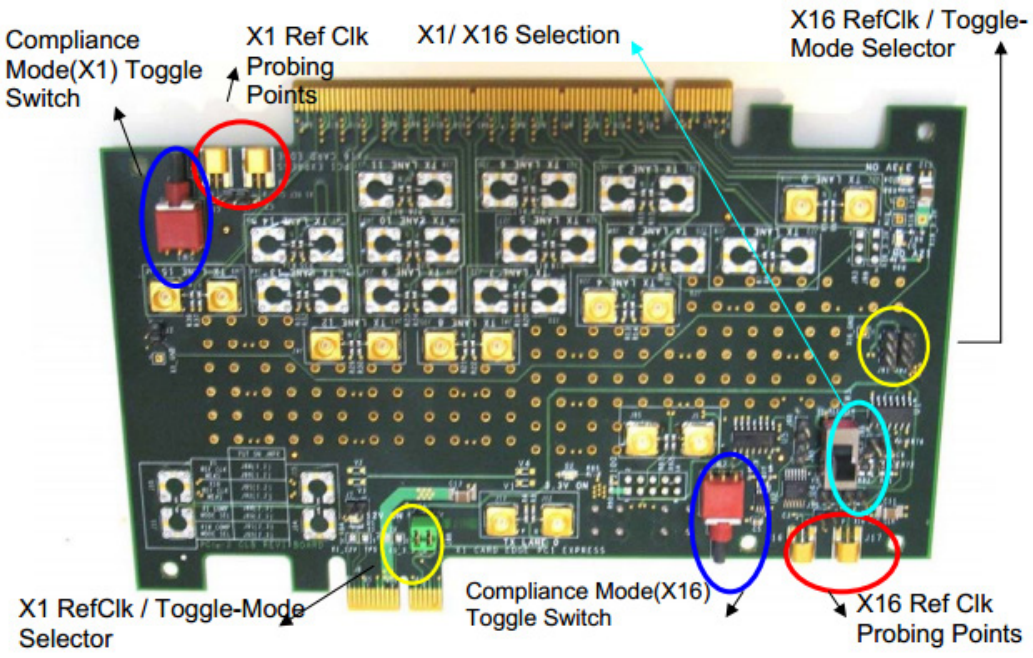

Figure 4. CLB3.0 X1X16 with several key features highlighted

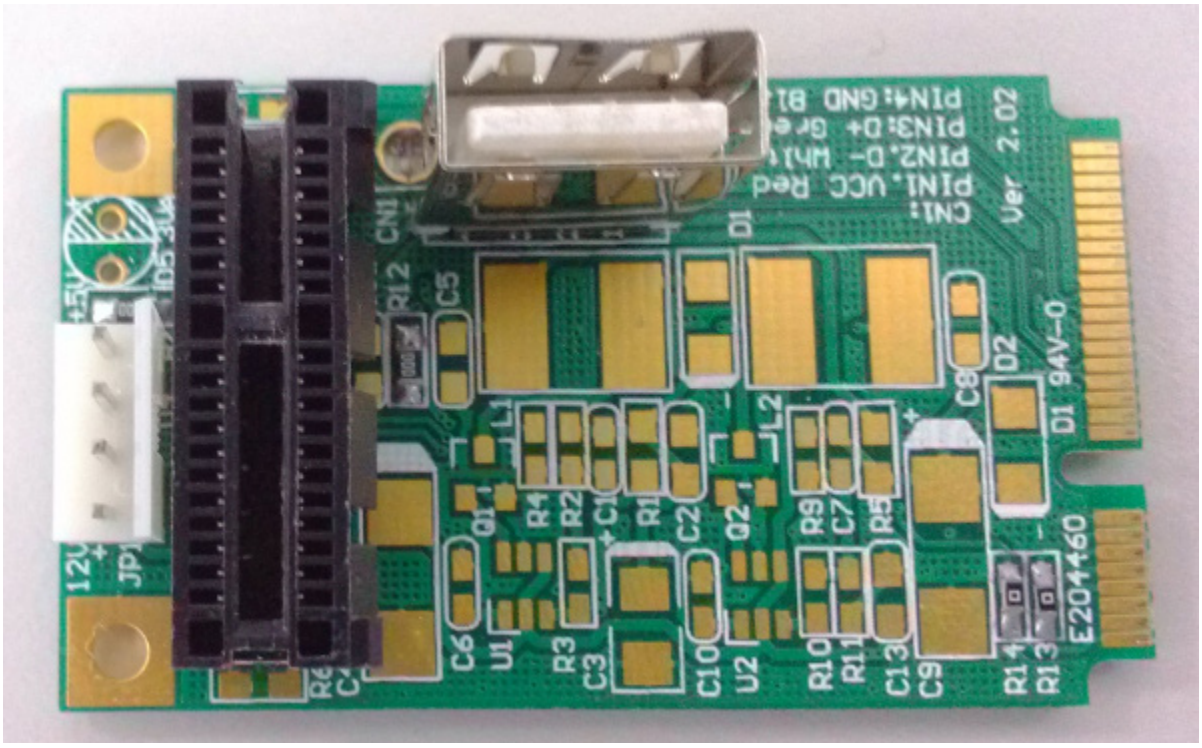

Figure 5. Mini-PCIe cover for the PCIe board

2.3. Test environment

- Operating system: Linux® OS L4.1.15_1.2.0.
- Additional software changes for the PCIe compliance test based on L4.1.15_1.2.0 are required. To access the software changes, visit community.nxp.com/docs/DOC-333261.

2.4. Analysis software

- N5393C PCI Express test application.

2.5. Additional information

- Test items: contains the electrical test only.
- Test method and equipment operation:
  - See *PCI Express Architecture PHY Test Specification, rev. 2.0*. (PCI-SIG: 2008, register at www.pcisig.com to download the document).
    www.pcisig.com/members/downloads/PCI_Express_Test_Spec_Electrical_Layer_2_0_rev_1_0_17Sept2012_Final.pdf
  - See *PCI Express 2.0 CEM Signal Quality Testing for Add-in Cards using Agilent DSO/DSA91304A 13GHz and DSOX/DSAX93204A 16-32GHz Real-Time Oscilloscopes, Version 1.2* (PCI-SIG, 20110; register at www.pcisig.com to download the document).
    www.pcisig.com/members/downloads/specifications/testprocedures/PCIE_2_0_Add_in_Card_test_Agilent_DSOX9xxxxx_v1_2.pdf?referring_url=%2Fkws
- 100 MHz reference clock: internal PLL clock (default).

3. PCIE test basic procedures

Perform the test as follows:

1. Perform the oscilloscope calibration and cable de-skew, as described in Appendix A[1].
2. Connect four BNC connectors to the oscilloscope channels 1, 2, 3, and 4.
3. Connect four SMA-SMP cables to the BNC connectors on the oscilloscope.
   - Connect the SMP end of the SMA-SMP cable on channel 1 to J13 on the CLB board (it is the positive data line).
   - Connect the SMP end of the SMA-SMP cable on channel 3 to J12 on the CLB board (it is the negative data line).
   - Connect the SMP end of the SMA-SMP cable on channel 2 to J16 on the CLB board (it is the positive clock line; 100 MHz).
   - Connect the SMP end of the SMA-SMP cable on channel 4 to J9 on the CLB board (it is the negative clock line; 100 MHz).

[1] See Appendix A in the document *PCI Express 2.0 CEM Signal Quality Testing for Add-in Cards using Agilent DSO/DSA91304A 13GHz and DSOX/DSAX93204A 16-32GHz Real-Time Oscilloscopes, Version 1.2*.

4. Insert the SD card that contains the PCIe test image into the SD4 slot and make sure that the boot switches (SW10, SW11, and SW12) are set properly.
5. Connect the mini-PCIe cover to the PCIe daughter board via the mini-PCIe connector (J15) on the i.MX7D EVK board.
6. Connect the CLB board via the PCIe connector (CN3) on the mini-PCIe cover to the PCIe daughter board.
7. Set the following on the CLB board:
   - Set the slide switch SW3 to “x1 REF CLK”, as shown in Figure 6.
   - Set the slide switch SW4 to “x1 REF CLK MEAS”, as shown in Figure 7.

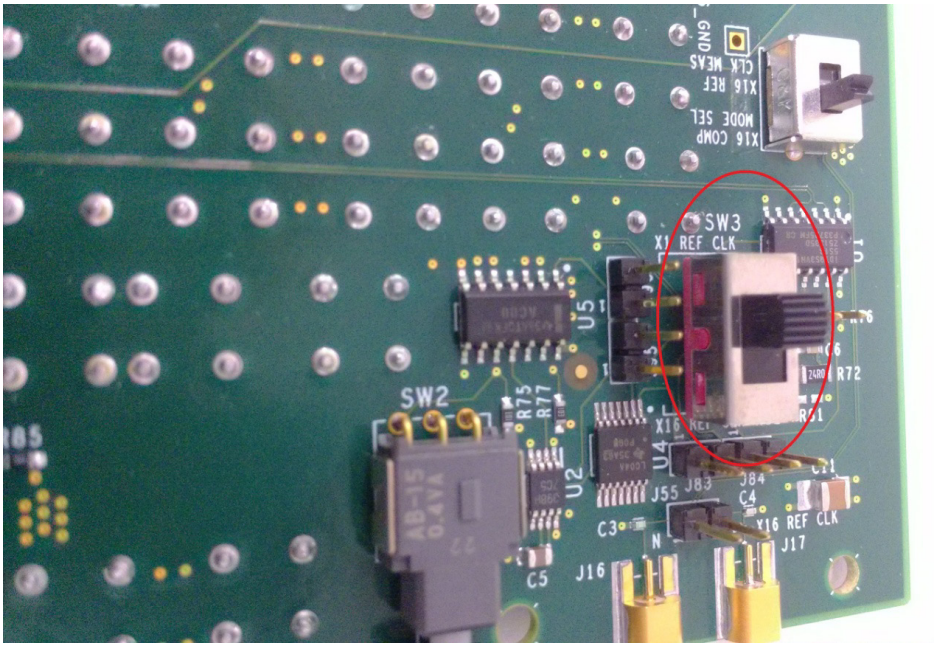

Figure 6. SW3 switch setting

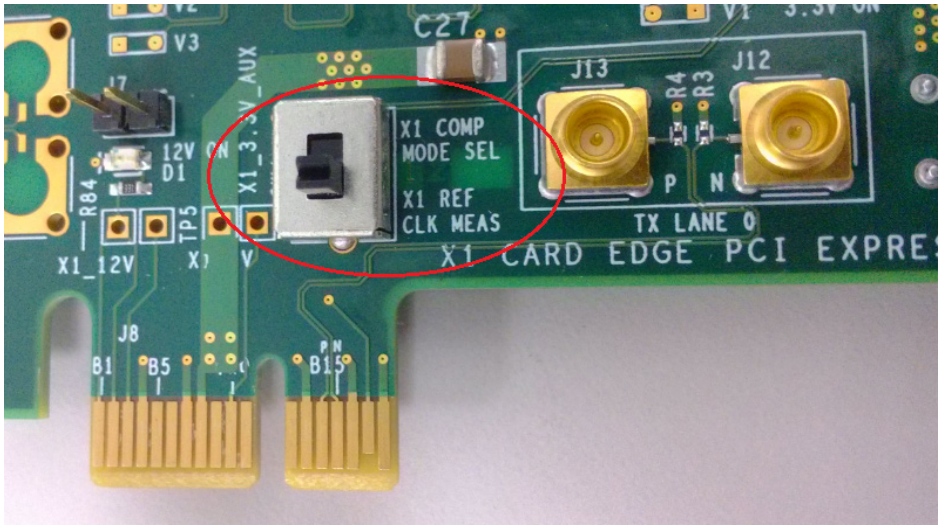

Figure 7. SW4 switch setting

8. The whole connection is shown in this figure:

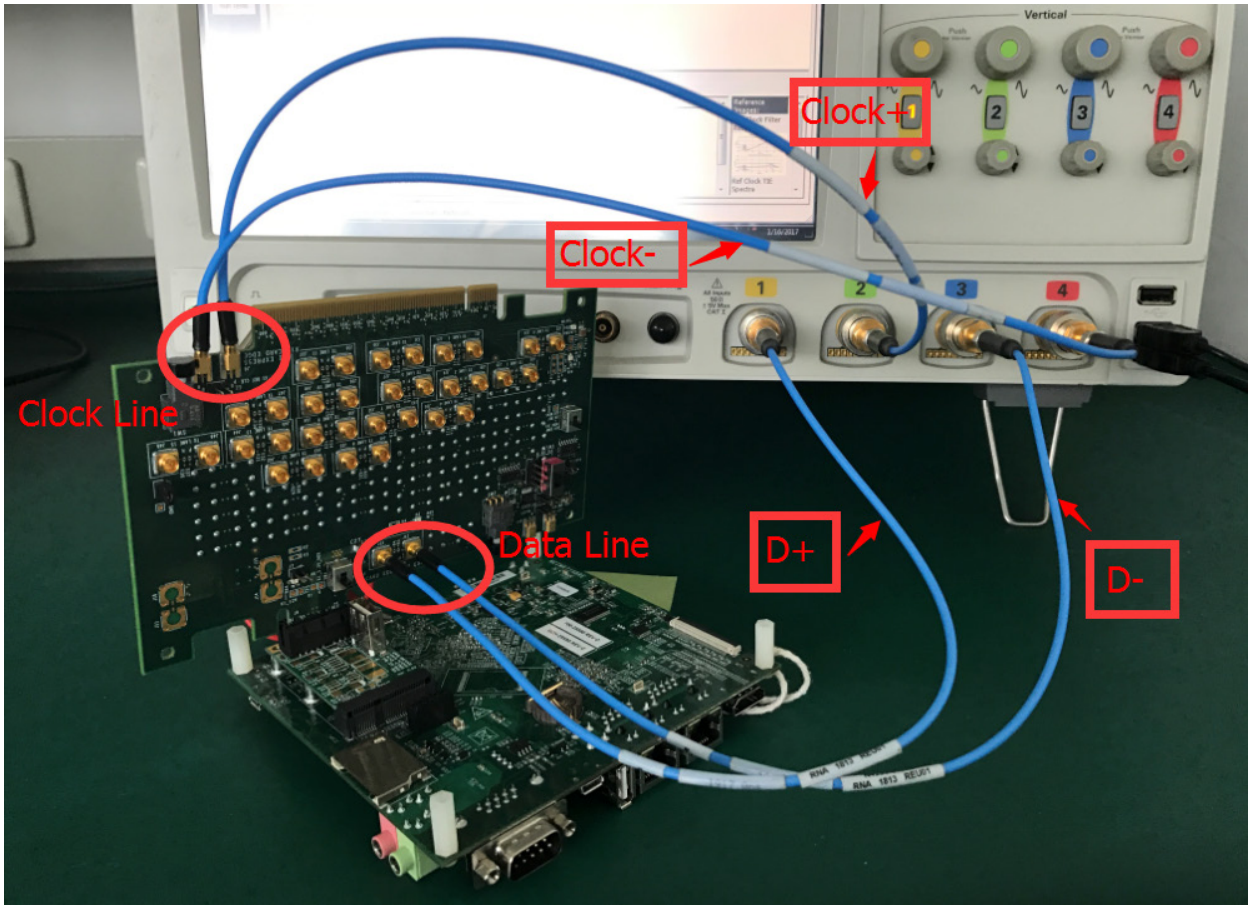

Figure 8. The whole connection

9. After the preparation is made, power the board on and run the PCIe test software on the oscilloscope:

   "Analyze—Automated Test Apps—N5393C PCI Express Test App"

10. Select the right options in the test software:
    - In the "Device" menu, select the right test mode (if you want to run the PCIE 1.1 test, select the "PCIE 1.1" option).
    - In the "Test Point" menu, select the "System Board Tests" and "RefClk Tests" options.
    - In the "Test Information" menu, select the "Clean Clock" option.
    - When performing the x1 lane test, you don't have to select anything in the "Data Lane" menu.
    - Keep the other options at their default values.

The following figure shows all the "Set Up" tab options.

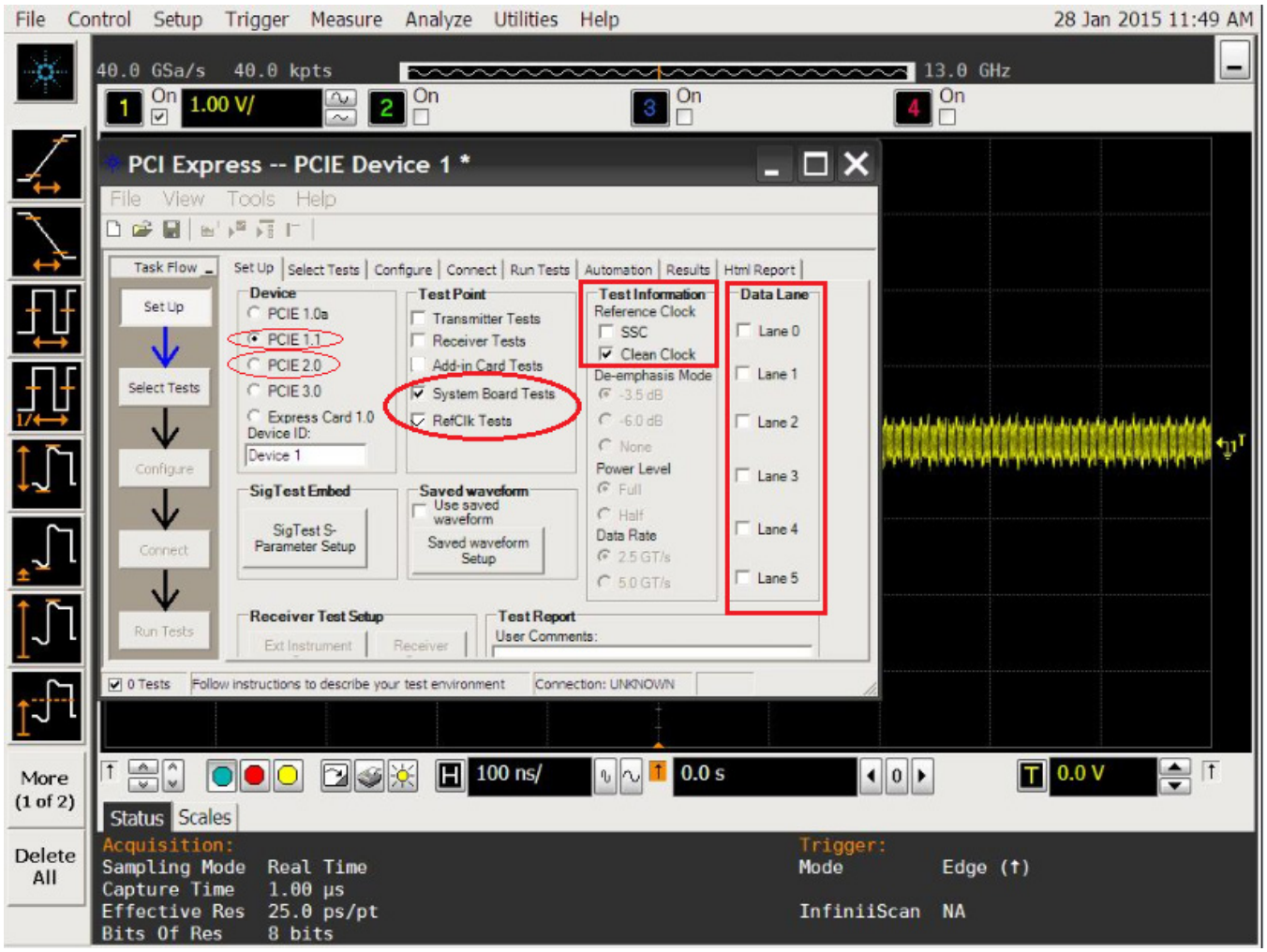

Figure 9. "Set Up" tab setting in the PCIe test software

11. In the "Select Tests" tab, select "test all".
12. In the "Connect" tab, double check whether the test cables are connected properly.
13. If you want to run the PCIE 1.1 test, select "Run Tests" and run the PCIE test.
14. If you want to run the PCIE 2.0 test, set the following:
    - Use one SMP-SMP cable to connect J85 to J4 and another SMP-SMP cable to connect J5 to J87, as shown in the following figure.

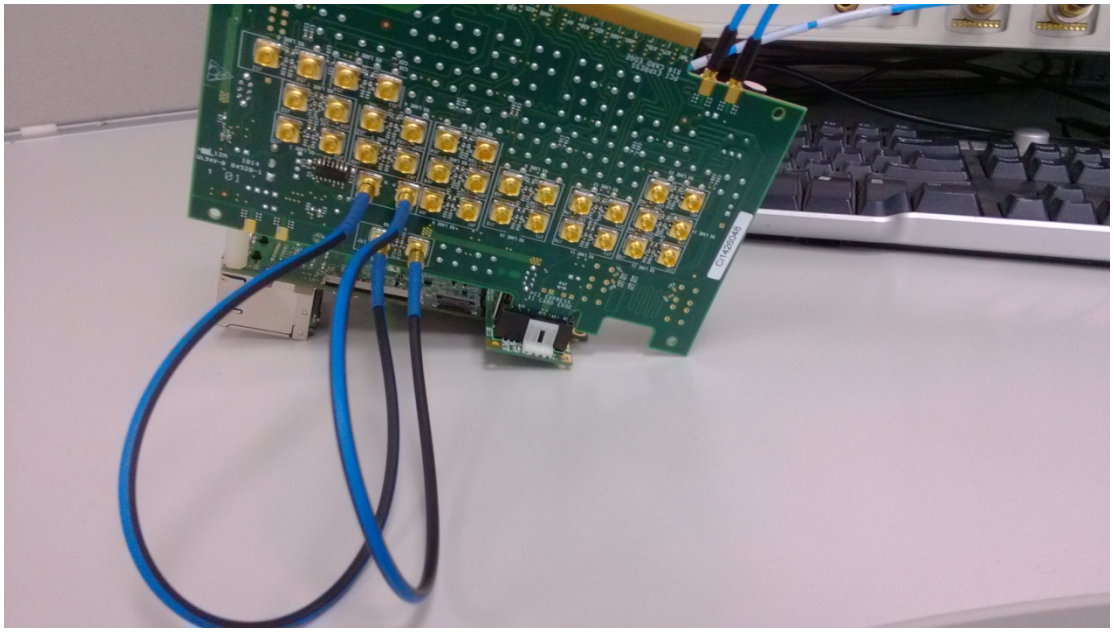

Figure 10. PCIE 2.0 test settings

- Set the slide switch SW4 to “x1 COMP MODE SEL”, as shown in the following figure.
- Press the SW1 button to make sure that the interval between the most closely spaced adjacent crossover locations is around 200 ps. (5 GT/s).

NOTE

When performing this setting, make sure that the board is powered on.

- Set the slide switch SW4 back to “x1 REF CLK MEAS”.

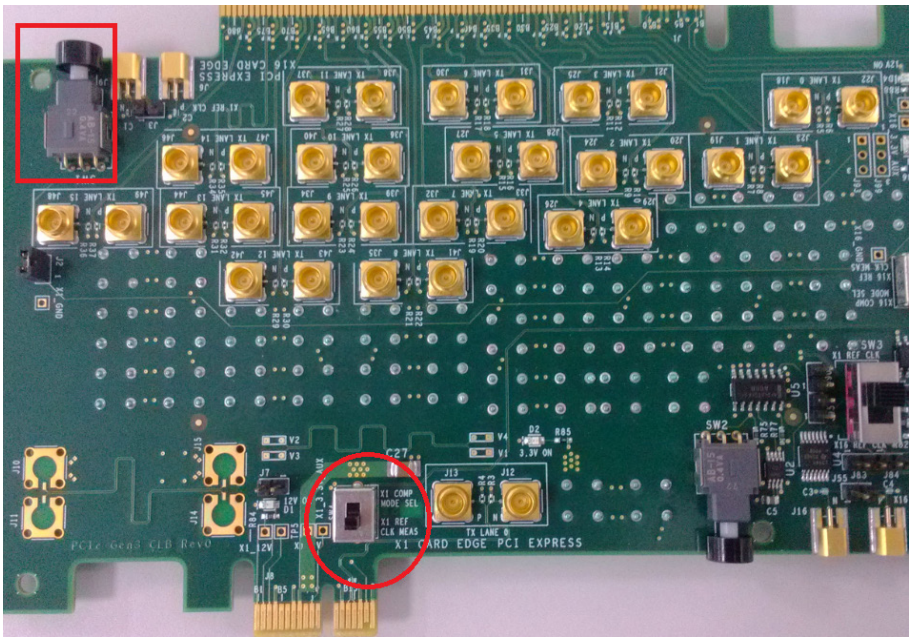

Figure 11. SW1 and SW4 settings for the PCIE 2.0 test

4. PCIE test results

On the i.MX7D EVK board, the internal clock is the default one. When performing the PCIE test, test the eye-width, phase jitter, rising edge rate, and so on. Obtain the detailed information from the test report.

4.1. PCIE 1.1 test results—internal clock

The detailed settings are provided in Section 2, "Test equipment". After the test, obtain the test results (as shown in the following table).

Table 1. PCIE 1.1 test results

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	System Board Tx, Unit Interval (PCIE 1.1)	399.9960 ps	48.3 %	399.8800 ps <= VALUE <= 400.1200 ps
✓	0	1	System Board Tx, Template Tests (PCIE 1.1)	Pass	100.0 %	Pass/Fail
✓	0	1	System Board Tx, Median to Max Jitter (PCIE 1.1)	18.15 ps	76.4 %	VALUE <= 77.00 ps
✓	0	1	System Board Tx, Eye-Width (PCIE 1.1)	354.89 ps	44.3 %	VALUE >= 246.00 ps
✓	0	1	System Board Tx, Peak Differential Output Voltage (Transition)(PCIE 1.1)	653.8 mV	41.0 %	274.0 mV <= VALUE <= 1.2000 V
✓	0	1	System Board Tx, Peak Differential Output Voltage (NonTransition)(PCIE 1.1)	565.2 mV	33.0 %	253.0 mV <= VALUE <= 1.2000 V
✓	0	1	Reference Clock, Phase Jitter (PCIE 1.1)	33.54 ps	61.0 %	VALUE <= 86.00 ps
✓	0	1	Reference Clock, Rising Edge Rate (PCIE 1.1)	2.02 V/ns	41.8 %	600 mV/ns <= VALUE <= 4.00 V/ns
✓	0	1	Reference Clock, Falling Edge Rate (PCIE 1.1)	2.01 V/ns	41.5 %	600 mV/ns <= VALUE <= 4.00 V/ns
✓	0	1	Reference Clock, Differential Input High Voltage (PCIE 1.1)	603 mV	302.0 %	VALUE >= 150 mV
✓	0	1	Reference Clock, Differential Input Low Voltage (PCIE 1.1)	-596 mV	297.3 %	VALUE <= -150 mV
✓	0	1	Reference Clock, Average Clock Period (PCIE 1.1)	-12 ppm	48.0 %	-300 ppm <= VALUE <= 300 ppm
✓	0	1	Reference Clock, Duty Cycle (PCIE 1.1)	50.2 %	49.0 %	40.0 % <= VALUE <= 60.0 %
✓	0	1	Reference Clock, Absolute Crossing Point Voltage (PCIE 1.1)	261.8 mV	3.9 %	250.0 mV <= VALUE <= 550.0 mV
✓	0	1	Reference Clock, Variation of VCross (PCIE 1.1)	40.7 mV	70.9 %	VALUE <= 140.0 mV
✓	0	1	Reference Clock, Absolute Max Input Voltage (PCIE 1.1)	601.1 mV	47.7 %	VALUE <= 1.1500 V
✓	0	1	Reference Clock, Absolute Min Input Voltage (PCIE 1.1)	-18.2 mV	93.9 %	VALUE >= -300.0 mV
✓	0	1	Reference Clock, Rise-Fall Matching (PCIE 1.1)	5.14 %	74.3 %	VALUE <= 20.00 %

The main information about the PCIE 1.1 test are shown in the above table.

4.2. PCIE 2.0 test results—internal clock

NOTE

When performing the PCIE 2.0 test, pay attention to step 14 (described in Section 2, "Test equipment").

The test results are shown in the following table.

Table 2. PCIE 2.0 test report

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	System Board Tx, Unit Interval (PCIE 2.0, 5.0 GT/s)	199.9990 ps	49.2 %	199.9400 ps <= VALUE <= 200.0600 ps
✓	0	1	System Board Tx, Template Tests (PCIE 2.0, 5.0 GT/s)	Pass	100.0 %	Pass/Fail
✓	0	1	System Board Tx, Peak Differential Output Voltage (Transition)(PCIE 2.0, 5.0 GT/s)	687.9 mV	43.1 %	300.0 mV <= VALUE <= 1.2000 V
✓	0	1	System Board Tx, Peak Differential Output Voltage (Non Transition)(PCIE 2.0, 5.0 GT/s)	574.4 mV	30.5 %	300.0 mV <= VALUE <= 1.2000 V
✓	0	1	System Board Tx, Eye-Width with crosstalk (PCIE 2.0, 5.0 GT/s)	161.48 ps	70.0 %	VALUE >= 95.00 ps
✓	0	1	System Board Tx, RMS Random Jitter with crosstalk (PCIE 2.0, 5.0 GT/s)	1.863 ps	75.0 %	VALUE <= 7.460 ps
✓	0	1	System Board Tx, Maximum Deterministic Jitter with crosstalk (PCIE 2.0, 5.0 GT/s)	12.312 ps	78.4 %	VALUE <= 57.000 ps
✓	0	1	System Board Tx, Total Jitter at BER-12 with crosstalk (PCIE 2.0, 5.0 GT/s)	38.524 ps	63.3 %	VALUE <= 105.000 ps
✓	0	1	System Board Tx, Eye-Width without crosstalk (PCIE 2.0, 5.0 GT/s)	161.48 ps	49.5 %	VALUE >= 108.00 ps
✓	0	1	System Board Tx, RMS Random Jitter without crosstalk (PCIE 2.0, 5.0 GT/s)	1.863 ps	71.5 %	VALUE <= 6.540 ps
✓	0	1	System Board Tx, Maximum Deterministic Jitter without crosstalk (PCIE 2.0, 5.0 GT/s)	12.312 ps	72.0 %	VALUE <= 44.000 ps
✓	0	1	System Board Tx, Total Jitter at BER-12 without crosstalk (PCIE 2.0, 5.0 GT/s)	38.524 ps	58.1 %	VALUE <= 92.000 ps
✓	0	1	Reference Clock, High frequency > 1.5MHz RMS Jitter (Common Clk) (PCIE 2.0, 5.0 GT/s)	2.28 ps	26.5 %	VALUE <= 3.10 ps
✓	0	1	Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Common Clk) (PCIE 2.0, 5.0 GT/s)	400 fs	86.7 %	VALUE <= 3.00 ps
✓	0	1	Reference Clock, High frequency > 1.5MHz RMS Jitter (Data Clk) (PCIE 2.0, 5.0 GT/s)	2.74 ps	31.5 %	VALUE <= 4.00 ps
✓	0	1	Reference Clock, Low frequency 10kHz - 1.5MHz RMS Jitter (Data Clk) (PCIE 2.0, 5.0 GT/s)	580 fs	92.3 %	VALUE <= 7.50 ps

The main information about the PCIE 2.0 test are listed in the above table.

5. Revision history

This table summarizes the changes done to this document since the initial release:

Table 3. Revision history

Revision number	Date	Substantive changes
0	02/2017	Initial release

How to Reach Us:

Home Page:
nxp.com

Web Support:
nxp.com/support

Document Number: PCIECGFIMX7DUG
Rev. 0
02/2017