Introducing the e5500 Core

The next core evolution in the QorIQ family of communications platforms

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1 Introduction

Welcome to the next generation of Power Architecture® processor technology, where 64-bit technology is unleashing a new wave of embedded solutions. The new Freescale e5500 core is the latest technology evolution in the QorIQ family of communications platforms, enabling applications to take advantage of 64 bits of data per clock cycle. With core frequencies scaling up to 2.5 GHz, and the ability to address more memory than ever before, the e5500 core provides significant technology advancements for high-performance embedded solutions.

2 The Benefits of 64-bit Core Processing

As embedded applications try to solve more complex problems, handle larger networks and implement new features, the need for compute processing on larger data sets grows. With the addition of the e5500 core, Freescale is enabling next-generation solutions to migrate to a core that can handle up to 64 bits of data in each clock cycle, empowering next-generation, computational-intensive embedded applications. This is especially beneficial in applications that perform image or video processing, or compute statistics, where moving and processing large amounts of data quickly is critical. The ability to perform 64-bit processing, versus 32-bit processing, will benefit a variety of market segments such as industrial applications, network solutions, security appliances and storage equipment, and will help drive the next generation of product development.

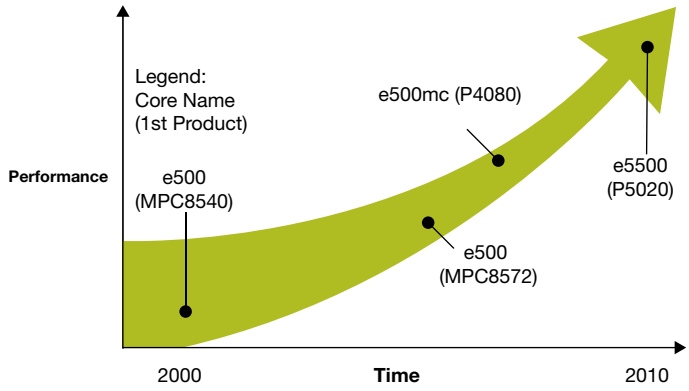
The e5500 core is also useful in embedded applications that are facing memory limitation issues. The ability to have user code address beyond 4 GB of memory is becoming critical for networking applications as networks increase their support for more subscribers, and for industrial and multimedia solutions that engage in increasingly complex image processing and rendering. The e5500 core enables user code to address up to 64 GB of flat memory space, removing the burden imposed in memory-bound systems today.

The e5500 provides the next-generation core technology available in the Freescale e500 family, enabling designers to take advantage of 64-bit processing through an optimized core well-suited for multicore environments.

3 The Evolution of the e500 Core Built on Power Architecture Technology

The new e5500 core leverages the long history of Freescale's e500 core, built on Power Architecture technology, which has been the fundamental building block in the PowerQUICC III processor family and now the QorIQ communications platforms. The e500 core was first introduced in 2000 as part of the MPC8540 family, and achieved core frequencies up to 1 GHz. It provided a seven-stage pipeline, with out-of-order execution, making it very efficient for embedded applications with code that provides a significant amount of branching. Freescale introduced the 1.5 GHz version of the e500 core in 2004, enabling higher levels of performance for embedded solutions.

Figure 1: The e500 Power Architecture® Technology Evolution



As shown in Figure 1, by 2007, a dual e500 core System-on-Chip (SoC) was available through the MPC8572 family, enabling designers to take advantage of two cores with a shared L2. In 2008, Freescale announced a new version of the e500 core, called e500mc, which specifically targets multicore enviroments. This core introduced the notion of a backside L2 cache as a lower latency architecture for multicore, and changed from embedded to a classic floating point unit (FPU). The core also introduced hypervisor support, used to manage and partition resources between different cores, which is critical for multicore applications. The e500mc core made its first debut in the QorIQ P4 platform as part of the QorIQ P4080 processor, an eight-core SoC that is the flagship processor of the QorIQ family of communications platforms.

Table 1: Comparison of the e500 Core Family

	e500	e500mc	e5500
Max Frequency	1.5 GHz	1.5 GHz	2.5 GHz
Power ISA Version	2.03	2.06	2.06 with all 64-bit
Pipeline Depth/Width	7/2	7/2	7/2
Integer Units	3	3	3
Floating Point	Embedded	Classic	Classic
L1 I/D Caches	32 KB	32 KB	32 KB
L2 Cache	Frontside	Backside	Backside
Hypervisor support	No	Yes	Yes

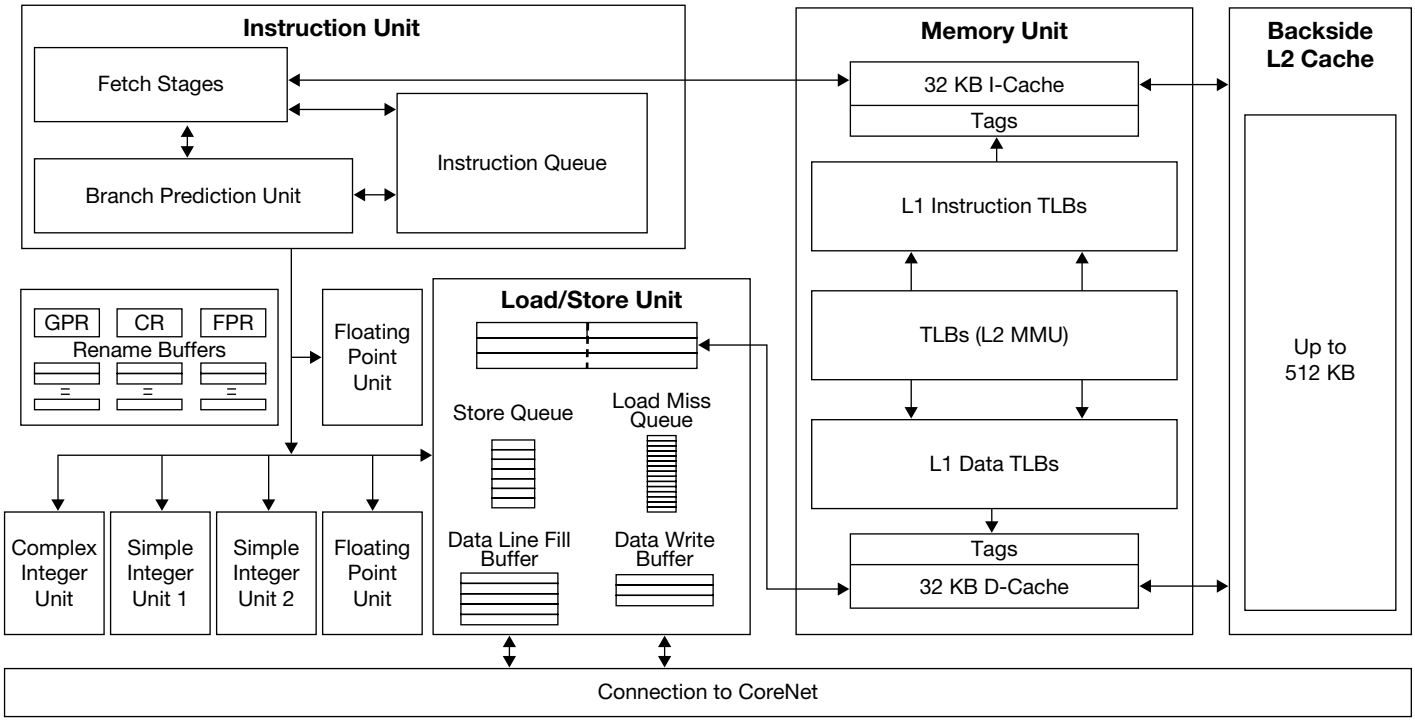
The e5500 core, announced in 2010, evolves the e500mc core with 64-bit processing, higher frequencies and improvements in the FPU, making it ideal for the next generation of high-performance, embedded multicore applications. Table 1 summarizes the e500 family and highlights the improvements made in frequency, cache architecture and the FPU that make the core technology the foundation for many high-performance embedded solutions today.

4 Architectural Overview of the e5500 Core

The e5500 is a superscalar, dual-issue core with out-of-order execution and in-order completion. It maintains the seven-stage, four-issue pipeline that is a trademark of the e500 family, but is able to provide additional performance, by scaling up to 2.5 GHz. This provides applications with 2x the performance increase of the previous Power Architecture generation, making it ideal for high-performance systems, such as control plane applications that benefit from core performance improvements.

Beyond frequency, e5500 core has improvements in the FPU, cache architecture and 64-bit computation, as well as provides hypervisor capabilities. It also takes advantage of the new Power Architecture ISA v2.06 and provides additional instructions for byte and bit-level acceleration. All of these elements combined together provide an overall 20 percent performance improvement in DMIPs/MHz from the e500mc core, giving designers more computational abilities within an embedded power envelope.

Figure 2: Block Diagram of the e5500 Architecture



4.1 Floating Point Unit

The e5500 core supports a high-performance IEEE® 754 FPU with double precision capabilities. It enables customers to see twice the single precision floating point performance when using the e5500 core, and up to four times the performance in double precision floating point calculations at the same frequency as previous e500 cores. Industrial applications in particular will benefit from the e5500 FPU, as many image processing and defense applications rely on single and double precision floating point calculations.

4.2 L2 Cache Architecture

The architecture of the cache within the e5500 core provides engineers with larger, backside L2 caches that can scale up to 512 KB. The backside cache is a lower latency architecture that helps to provide data and instructions quickly to the core, while reducing overall snoop traffic in the system. It provides significantly more private cache resources to lock cache lines into the L2, which helps to facilitate determinism and fast interrupt handlers. Furthermore, the L2 cache provides flexible allocation modes, including eight-way instruction or data allocation or any combination in between, which allows designers to use the cache most efficiently for their application.

4.3 64-bit Computation

64-bit processing is another significant element of the e5500 core, empowering applications to move and compute 64 bits of data at one time. This is an advantage across the architecture, as it means there are now 64-bit general purpose registers (GPR) and 64-bit computation instructions, which allow for higher data throughput via registers and more register storage. 64-bit virtual addressing is supported, and enables more virtual address space for applications. The e5500 also extends the memory capabilities of previous e500 cores as it enables applications to address up to 64 GB of flat memory space.

The e5500 core is also software compatible with the rest of the e500 family, which is critical for applications that have a large amount of legacy code. Designers have the option to run the core in 32-bit mode, making it a seamless migration from previous e500-based products while taking advantage of the higher frequency and floating point improvements. It also provides a compelling roadmap for customers that are looking at 64-bit processing for next-generation solutions, as the designer can start in 32-bit mode and later select to move to 64-bit mode.

4.4 Hypervisor Support

The ability to control the sharing of resources across multiple cores is one of the key elements of operating within a multicore environment. The e5500 core includes support for an embedded hypervisor that adds an additional hypervisor privilege level for easy partitioning and sharing of resources. Previous e500 cores only supported user and supervisor modes, while both the e500mc and e5500 supports a third “guest” mode. For more information on the QorIQ communications platform hypervisor features, please reference the white paper titled *Freescale’s Embedded Hypervisor for QorIQ P4 Series Communications Platform*.

5 Designing with the e5500 Core

Beyond the hardware architecture of the e5500 core, the next critical element in the design process is the software enablement of the technology. Freescale has developed a wide ecosystem of 64-bit enabled third-party software vendors, tool chains, models and libraries to assist engineers when designing in the e5500 core. For more information on Freescale’s tools and libraries, or its third-party ecosystem, please contact your local Freescale representative.

6 Conclusion

The new e5500 core introduces the next evolution in high-performance computing for embedded solutions. Enhancing the legacy of the e500 core family, the e5500 introduces 64-bit processing for embedded applications and provides higher levels of performance through increased core frequencies scaling up to 2.5 GHz, improvements in cache architecture and floating point performance, as well as hypervisor support. All of these architectural enhancements result in a 20 percent improvement of DMIPs/MHz from previous e500 cores. All of this performance within an embedded power envelope makes this core highly optimized for high-performance, power-sensitive applications. Welcome to the next generation of Power Architecture processors with 64-bit core technology from Freescale.

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