Freescale Semiconductor
Solution Guide

DSLAM8360EWP
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Using the PowerQUICC™ II Pro MPC8360E to Build an Intelligent DSLAM Line Card

Digital subscriber line access multiplexers (DSLAMs) are a leading broadband access technology, delivering high-speed data transmission over existing copper telephone lines. The technology gives service providers the ability to transform the existing public network into a high-performance, multi-service and feature rich network. DSLAMs support a wide variety of high-bandwidth applications including video-on-demand (VoD), voice over IP (VoIP), high-speed Internet access, and streaming multi-media content. Future evolution of the DSLAM market will see the migration from a centralized ATM-based to a decentralized IP-based architecture requiring yet more data processing capability from the end solution. Therefore, next generation DSLAM platforms will offer greater density, higher bandwidth, and lower cost per port. These features, coupled with greater service diversity, will offer new market segments to service providers while taking advantage of different DSL transport mechanisms, such as ADSL-> ADSL2+, VDSL->VDSL2, HDSL, and SHDSL.

Contents

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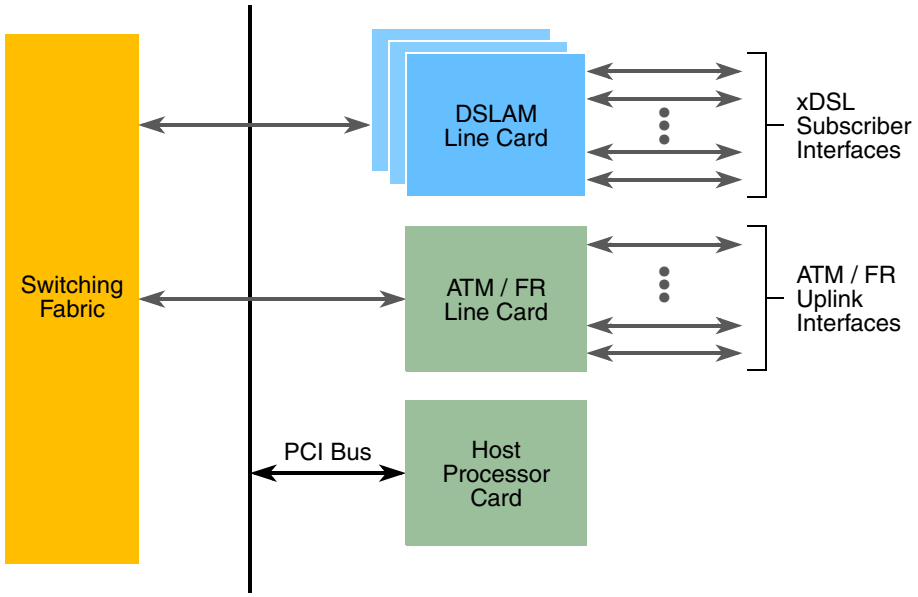

Figure 1. Internal Features of a Typical DSLAM

Figure 1 shows a typical DSLAM system. The xDSL subscriber's traffic is handled first by the DSLAM line-cards and then, via the switch fabric, is passed onto to the ATM or Frame Relay line card. This card aggregates the xDSL subscriber traffic into an uplink stream that is fed to an Internet Service Provider or company WAN. Traditionally, OEMs who designed these systems relied solely on ATM as a high-speed back plane transfer mechanism. With the development of Gigabit Ethernet, many new DSLAM designs are IP-packet switched. This facilitates delivery of IP-based services, such as Voice over IP (VoIP), video broadcast and distribution, and data networking. An intelligent DSLAM line card design must support both legacy ATM-based protocols, such as AAL0, AAL2, AAL5, and IMA, and also IP-based protocols such as IP or IPoA. A wide variety of link layer protocols also have to be supported regardless of whether it is an IP- or ATM-based network. These protocols include Ethernet, Frame Relay, PPP (Point to Point Protocol), PPPoA (over ATM), PPPoE (over Ethernet), IPoA (IP over ATM) and more recently, Multi-Protocol Label Switching (MPLS) over Ethernet or ATM.

1 Design Challenges

With the potential to offer multiple revenue streams from a single IP packet network, the ability to deliver voice, video, and data is the goal of every telecom operator. While IP is the key enabler, the challenge remains to support and interoperate between circuit and packet switched networks and between multiple standards and protocols.

Historically, DSLAM systems have been ATM-based with the primary role of aggregating multiple xDSL lines for the uplink to the external Central Office (CO) network, that is to say an Internet service provider or to a Wide Area Network (WAN). The number of subscribers that a DSLAM can handle is a key system requirement. Supporting such high densities of users per platform or card requires a range of different interfaces and speeds.

On the networking uplink side, where ATM is prevalent, IP routing is quickly gaining traction. A robust system must be able to handle support for ATM, frame relay, and TDM traffic while being able to handle IP-based traffic over Gigabit Ethernet. Consequently, any solution must be able to handle the diversity and interworking of networking technologies such as IP-to-ATM switching and Segmentation And Reassembly (SARing).

The trend towards increased value-added services such as Quality of Service (QoS) capabilities and VPN services necessitates a total system approach to the architectural solution. An architecture that leverages a universal line card

strategy will maximize software re-use, provide a high degree of integration, and provide adequate network interfaces and throughput for future design activities, while ensuring minimal system power and cost. A successful system approach will provide faster time to market, reduced development effort, and quicker return on investment.

Therefore, design challenges for a successful DSLAM line-card include the following:

- Ability to support the transition and eventual convergence of ATM and IP networks
- Increasing port density on line cards – typically 24 to 96 ports
- Increasing bandwidth from high performance services and standards, such as ADSL-> ADSL2+ and VDSL->VDSL2/+ for “triple play”
- Intelligence moving to the edge of the network as a traditional DSLAM assumes some edge router functionality
- Maximizing existing infrastructure to accommodate more users
- Maximize Return On Investment (ROI) by reducing cost per port or user
- Support required protocols such as ATM, IP, VLAN, RTP, PPP, PPPoE/oA, L2TP, Diffserv, ML-PPP, MPLS, POS, Routing, Bridging, QoS, and so on
- Managing QoS to ensure prioritization of latency sensitive traffic to meet service level agreements
- Configurable bandwidth based on policy configuration across ATM, PPP, Ethernet, and IP technologies
- Multiple QoS dictates the need for different hierarchical lP or ATM traffic scheduling and shaping capability
- Ensure the security/confidentiality of subscribers information
- Provide the ability to add new features and functions through software based on market and subscriber demands

A robust DSLAM line-card design must combine the best of density, throughput, functionality, scalability and cost-efficiency, to provide equipment vendors with a distinct competitive advantage.

2 Freescale Semiconductor Solutions

In the competitive DSLAM market, highly integrated, cost-effective and scalable system solutions are required. With these system requirements in mind, Freescale is pleased to introduce the latest addition to its popular PowerQUICC family of microprocessors—the PowerQUICC II Pro MPC8360E.

The MPC8360E incorporates the e300, 603e core which includes 32 Kbytes of L1 instruction and data caches, 32-bit PCI bridge, four DMA channels, USB support, dual 32-bit DDR memory controller, a double precision floating point unit and on-board memory management units. A block diagram of the MPC8360E is shown in Figure 2.

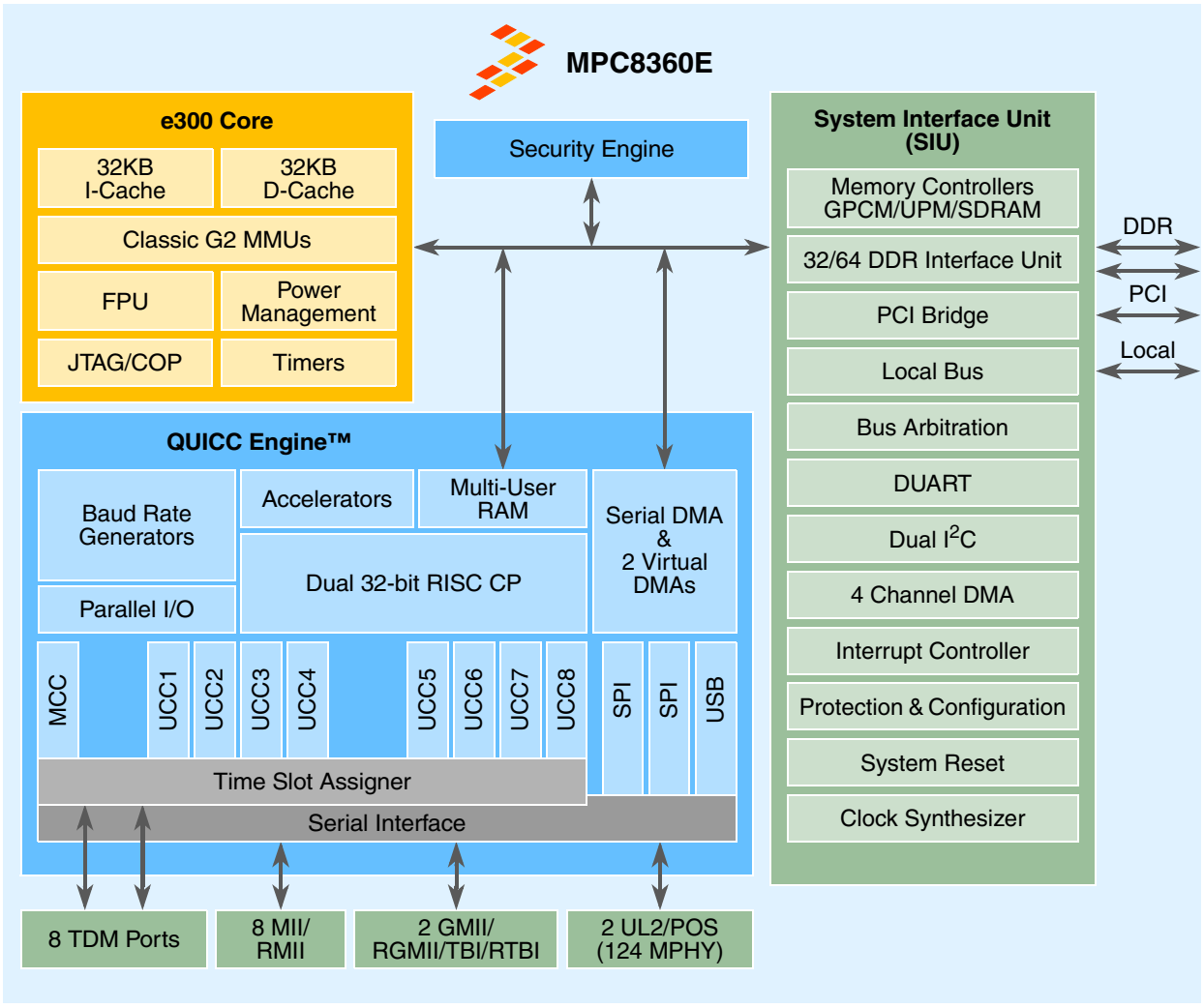

Figure 2. MPC8360E Block Diagram

A new communications complex—the QUICC™ Engine—forms the heart of the networking capability of the MPC8360E. The QUICC Engine contains several peripheral controllers and integrates two 32-bit RISC controllers. Each RISC controller can control multiple peripherals and work together to provide increased aggregated system bandwidth for higher throughput applications. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs) and multi-channel communication controller (MCC).

Each of the eight UCCs can support a variety of communication protocols: 10/100/1000 Mbps Ethernet through a Media-Independent Interface, ATM / POS PHY support up to OC-12 speeds, Serial ATM, Multi-PHY ATM, HDLC, UART, Multi-Link/Class PPP, BISYNC and 64 TDM channels. Each MCC is capable of supporting up to 256 TDM channels in either transparent or HDLC channel modes and multiplexing almost any combination of sub-groups into a single or multiple TDM stream. Inverse Multiplexing over ATM is supported and allows ATM traffic to be distributed across multiple E1/T1 circuits. This allows service providers to lease the exact bandwidth that subscriber's request.

In addition, the QUICC Engine can also support two UTOPIA level 2 or two POS interfaces, each interface capable of supporting 124 Multi-PHY, or up to two, 128 Multi-PHY interfaces using extended address mode. The QUICC Engine also features an integrated 8-port, L2 Ethernet switch which can provide 4 priority levels on each port,

VLAN functionality, IGMP snooping, network auto-negotiation function, store-and-forward switching and packet-error filtering. Enhanced interworking features within the QUICC Engine helps offload the main CPU. The QUICC Engine can provide ATM-to-ATM switching, Ethernet to ATM switching with L3 / L4 support and PPP interworking.

The MPC8360E's security engine allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, MD-5, and ARC-4 algorithms. It includes a public key accelerator and an on-chip random number generator.

In summary, the MPC8360E provides DSLAM line-card vendors with a highly integrated, fully programmable communications processor that allows reuse of existing legacy PowerQUICC II and III software drivers and microcode packages. This helps ensure that a low cost system solution can be quickly developed and will offer flexibility to accommodate new standards and evolving system requirements.

2.1 The PowerQUICC II Pro MPC8360E

The PowerQUICC II Pro MPC8360E is a high performance, highly integrated communication processor solution that offers the following.

2.1.1 MPC8360E Features

- High-performance, low power (< 5W typical power dissipation), and cost-effective communications processor
- The MPC8360E QUICC Engine offers a future proof solution for next generation designs by supporting programmable protocol termination, network interface termination, and interworking features to meet evolving protocol standards
- Single platform architecture supports the convergence of IP packet networks and ATM networks, including interworking between these networks
- Simplified network interface card design with a cost-effective single chip data plane/control plane solution for ATM or IP packet processing (or both). This reduced component count, board power consumption and board real estate.
- Universal network interface card design for multiple applications, which lowers costs and reduces time-to-market
- Built-in proprietary, hardware accelerators that accelerate data plane traffic, such as interworking, and control plane packet snooping, such as IGMP, VLAN tagging, DHCP, and so on
- DDR memory controller—one 64-bit or 2x32-bit interfaces that split data and control plane traffic at up to 333 MHz
- e300 PowerPC core (enhanced version of 603e core with 32K bytes of Level 1 Instruction and 32 Kbytes of Level 1 Data caches)
- 32-bit PCI interface
- 32-bit Local Bus interface
- USB
- Integrated 8-port L2 Ethernet switch
  - 8 connection ports of 10/100 Mbps MII/RMII & one CPU internal port
  - Each port supports four priority levels
  - Priority levels used with VLAN tags or IP TOS field to implement QoS

  - QoS types of traffic, such as voice, video, and data
- A security engine provides termination or encrypted plane traffic
- High degree of software compatibility with previous-generation PowerQUICC™ processor-based designs for backward compatibility and easier software migration
- Seamless connection to PowerQUICC III family devices for increased control (CPU) application processing requirements

2.1.1.1 Protocols

- ATM SAR up to 622Mbps (OC-12) full duplex, with ATM traffic shaping (ATF TM4.1) for up to 64K ATM connections
- Support for ATM AAL1 structured and unstructured Circuit Emulation Service (CES 2.0)
- Support for IMA and ATM Transmission Convergence sub-layer
- ATM OAM handling features compatible with ITU-T I.610
- PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP) and PPP mux in accordance with the following RFCs: 1661, 1662, 1990, 2686 and 3153
- IP termination support for IPv4 and IPv6 packets including TOS, TTL and header checksum processing
- L2 Ethernet switching using MAC address or IEEE 802.1P/Q VLAN tags
- Support for ATM (AAL2/AAL5) to Ethernet (IP) interworking
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics.
- Support for 256 channels or HDLC/Transparent or 128 channels of SS#7

2.1.1.2 Serial Interfaces

- Support for two UL2 / POS-PHY interfaces with 124 Multi-PHY addresses each.
- Support for two 1000Mbps Ethernet interfaces using GMII or RGMII, TBI, RTBI.
- Support for up to eight 10/100Mbps Ethernet interfaces using MII or RMII
- Support for up to eight T1 / E1 / J1 / E3 or DS-3 serial interfaces
- Support for dual UART, I²C and SPI interfaces.

System scalability is also made available through the number of UCCs and MCCs. The initial implementation offers eight UCCs and one MCC, however as a result of the system-on-a-chip design methodology used for the QUICC Engine, these numbers can be scaled to support an optimized mix of communications channels. The flexible architecture of the QUICC Engine allows customers to customize their own application protocol and filtering requirements, allowing Freescale to add more RISC engines and/or UCCs on future family derivatives.

2.2 Development Environment

Development tools, hardware platforms, software building blocks and application-specific software solutions are available from Freescale and our Freescale Alliance Program, including third party protocol and signaling stack suppliers, real time operating systems support and a variety of applications software support. All of this builds upon the existing industry standard PowerQUICC family support program.

2.2.1 Software Development Tools

To simplify and accelerate the development process, Freescale will provide a user-friendly, integrated development environment (IDE), which includes a compiler, instruction set simulator and debugger for the e300 PowerPC core.

2.2.2 Application Development System (ADS)

Freescale provides an ADS board as a reference platform and programming development environment for the MPC8360E with a complete Linux Board Support Package. The ADS board will support on-board DDR SDRAM memory, a PCI interface, and a debug port and can be configured with optional daughter cards supporting protocols such as OC-3 or OC-12 ATM, 8xT1/E1 and Ethernet (10/100/1000Base T).

Also available is a complete development system based around the AdvancedTCA (ATCA) form factor chassis with a choice of AMC cards that can be operate stand alone, or as modular inserts into the main processor baseboard. This allows maximum flexibility for prototyping wireless network interface, control and base band applications using Freescale silicon solutions.

2.2.3 Modular Software Building Blocks

The QUICC Engine will be supported by a complete set of configurable device API drivers and initialization software. Figure 3 shows the wealth of software protocols that the QUICC Engine with the e300 PowerPC™ core is able to provide.

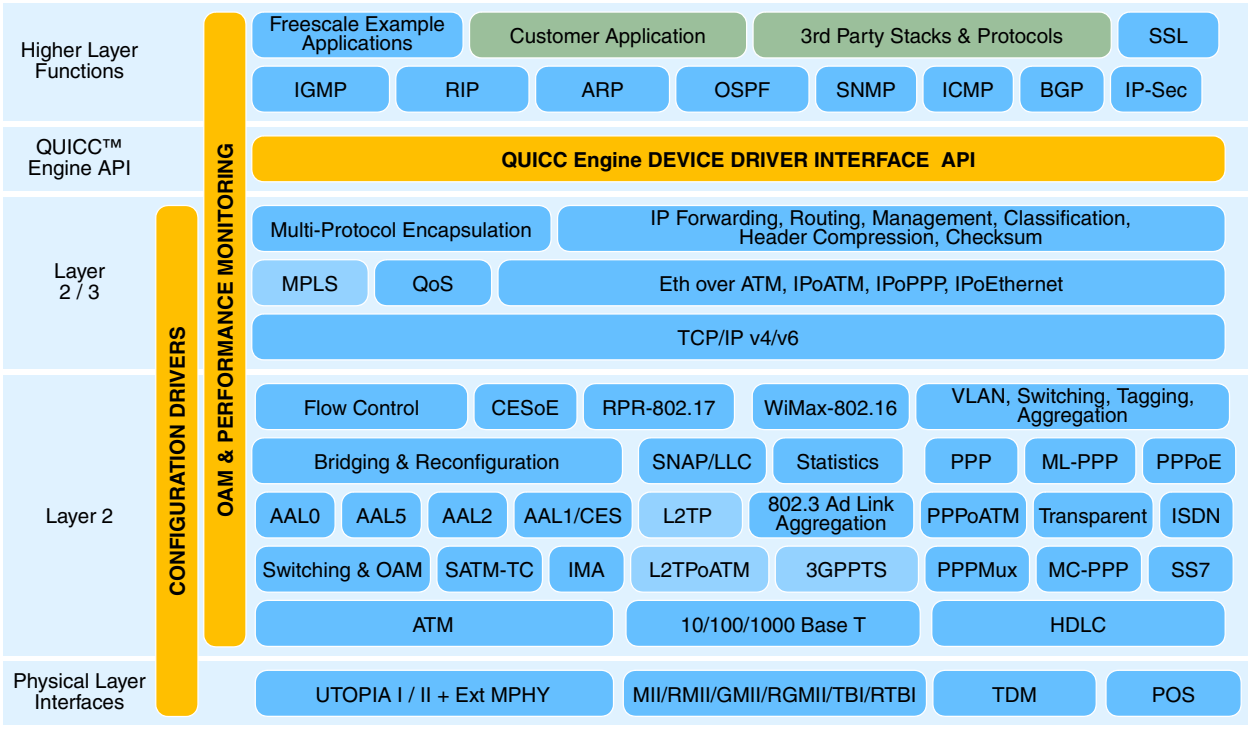

Figure 3. Software Protocol Support for the QUICC Engine

3 Application Example

The internal features of the MPC8360E make it suitable for a wide variety of network communication applications. The diagram in Figure 4 illustrates how an intelligent DSLAM line-card can be readily implemented.

In this example, the versatility of the UCCs handle the convergence of both packet and circuit switched networks because both ATM and Gigabit Ethernet functions can be supported. As shown on the left-hand side of Figure 4, subscribers are connected to the DSLAM line-card via the DSL PHYs and the integrated UTOPIA interface on the MPC8360E.

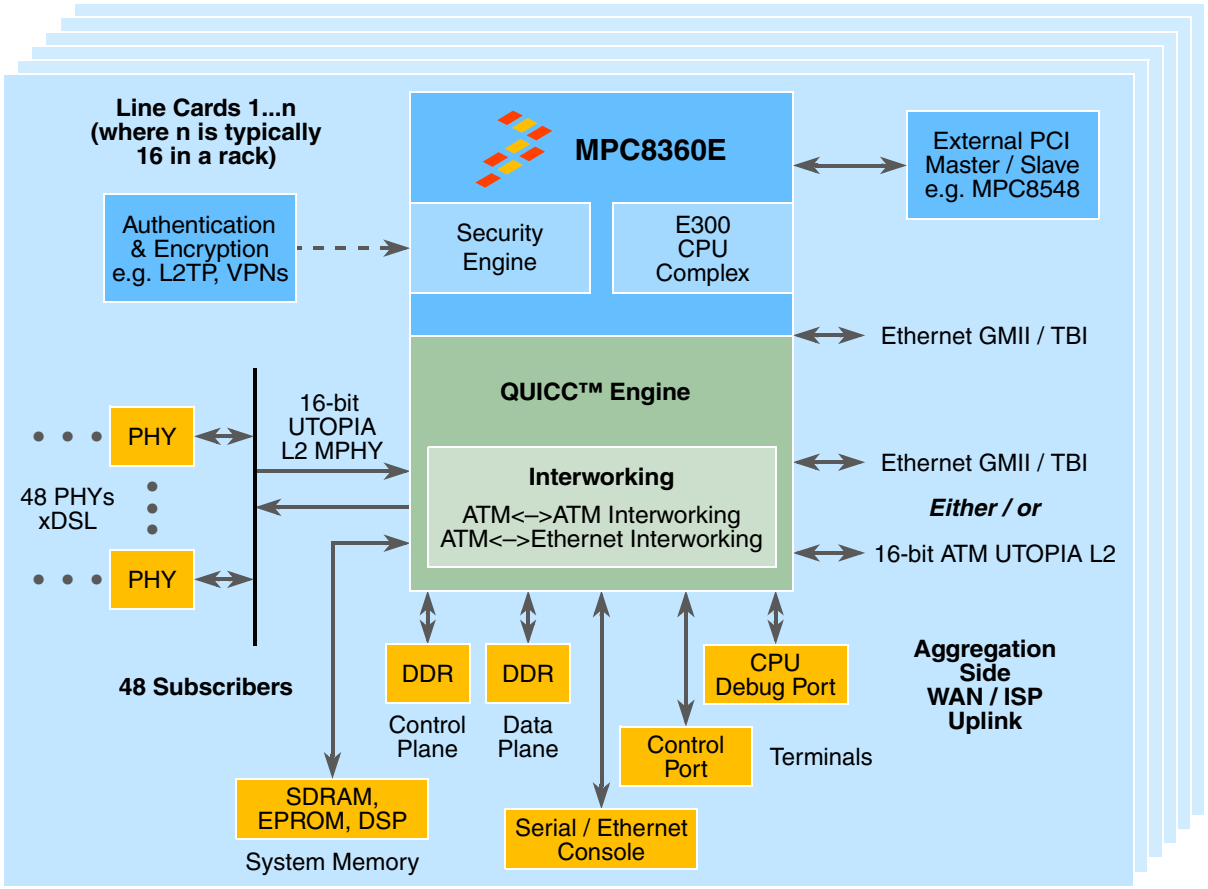

Figure 4. MPC8360E Line Card Implementation

If, for example, the application in Figure 4 is handling 48 ports of ADSL2 each port will have a maximum data rate of 12Mbps downstream (for Annex A & B compliant equipment) and 1Mbps upstream (for Annex J compliant equipment). This generates an aggregate bandwidth of 624Mbps that must be handled through the uplink. The uplink connection to a WAN or the service provider's central office can be made using either of the two integrated Gigabit Ethernet interfaces or by implementing an ATM interface via the UCCs. Either way, the uplink connection can be made regardless of the type of switch fabric used in the uplink network.

In this type of application, the MPC8360E makes use of its internal interworking features to offload the e300 CPU. Here, ATM-ATM interworking would be used to transfer data from the ATM based DSL subscriber inputs, through the RISC cores within the QUICC Engine and out through the other ATM UTOPIA on the uplink port. In the event that the uplink switch fabric is Ethernet-based then ATM-Ethernet interworking would also be provided by the MPC8360E QUICC Engine. Subscribers could also connect directly to the DSLAM line-card using E1/T1 lines. In

this scenario, the built-in IMA microcode could be used to bundle multiple E1/T1 lines together into a higher bit stream ATM connection for the uplink.

The main system memory is provided by the DDR interface, which can either support one 64-bit or two 32-bit interfaces. The dual DDR architecture provides an extremely efficient way of partitioning system control parameters. This helps ensure that data is not blocked as the data plane can be completely decoupled between the QUICC Engine and DDR memory and any control plane transactions. The local bus can be used for connected SDRAM, DSPs (for VoIP applications), or FLASH Eprom. The remaining unused UCCs can be configured as system terminals to allow some external I/O mechanism for debug and control.

Using the other unused interfaces on the MPC8360E a more integrated solution can be produced. For example, the PCI interface could be used to connect further devices such as the PowerQUICC III MPC8548 for additional CPU processing power or to provide connection to the main host processor card or backplane (as shown in Figure 1). Lastly, if the MPC8360E is used, the security engine could provide an efficient way of implementing secure VPN tunnels without burdening the main e300 core.

4 Summary

The PowerQUICC II Pro MPC8360E with the new QUICC Engine is a significant step forward in performance, integration and cost effectiveness for a wide variety of applications. For flexible, high performance, DSLAM line cards, the MPC8360E offers a comprehensive feature set that enables cost effective solutions with an unrivalled level of versatility to evolve as both standards and the system requirements change.

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