Motorola's PowerPC 603™ and PowerPC 604™ RISC Microprocessor: the C4/Ceramic-ball-grid Array Interconnect Technology

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Abstract - The Motorola PowerPC 603 and PowerPC 604 microprocessors are available in the 21mm controlled-collapsed-chip-connection/ceramic-ball-grid-array single-chip package (C4/CBGA). This paper will introduce the C4/CBGA interconnect technology and address the following: 1) the PCB land definition and board preparation requirements, 2) the ball-grid-array to board assembly methods, 3) the electrical design considerations, 4) the heat transfer mechanism and thermal control options, and 5) the CBGA-to-PCB testing and reliability.

NOMENCLATURE

AF	=	acceleration factor
$T_{max_{l, f}}$	=	highest T_{on} temperature (K); lab, field
$\Delta T_{l, f}$	=	$T_{on} - T_{off}$; lab, field
$f_{l, f}$	=	thermal cycling frequency; # of cycles; lab, field must be at least 6 per day
Q_c =		die power, W
Θ_{jc}	=	die junction-to-case resistance,°C/W
Θ_{jl} =		die junction-to-lead (i.e., ball) resistance, °C/W
Θ_{ja}	=	die junction-to-ambient resistance, °C/W

INTRODUCTION

PowerPC 603 and PowerPC 604 RISC Microprocessors

The scaleable PowerPC™ microprocessor family (Figure 1), jointly developed by Apple, IBM, and Motorola, is being designed into high-performance cost-effective computers (including notebooks, desktops, workstations, and servers). The PowerPC microprocessor family ranges from the PowerPC 601™ microprocessor to the PowerPC 620™ microprocessor. The PowerPC 603 microprocessor is a low-power implementation of the PowerPC Reduced-Instruction-Set-Computer (RISC) architecture. The

PowerPC 604 microprocessor is a 32-bit implementation of the PowerPC architecture, and is software and bus compatible with the PowerPC 601 and PowerPC 603
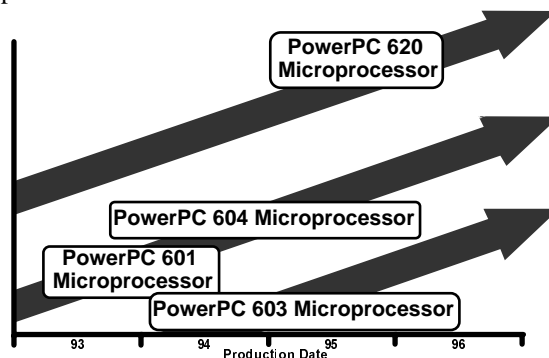

Figure 1. The PowerPC Microprocessor Family.

microprocessors. Both the Motorola PowerPC 603 and PowerPC 604 microprocessors are available in the 21mm controlled-collapsed-chip-connection/ceramic-ball-grid-array single-chip package (C4/CBGA) (Figure 2) [1,2].

Objective

In this paper we wish to address the following topics: 1) the C4/CBGA interconnect technology, 2) the PCB land definition and board preparation requirements, 3) the CBGA package-to-board assembly method, 4) the electrical design considerations, 5) the heat transfer mechanisms and thermal control options, and 6) the CBGA package-to-printed-circuit-board testing and reliability.

BACKGROUND

First-level Interconnect Technology: C4-Ceramic-Ball-Grid Array Package

The use of C4 die on a CBGA interconnect technology offers significant reduction in both the signal delay and the microelectronics packaging volume [3-5]. Figure 2 shows the salient features of the C4/CBGA interconnect technology. The C4 interconnection provides both the
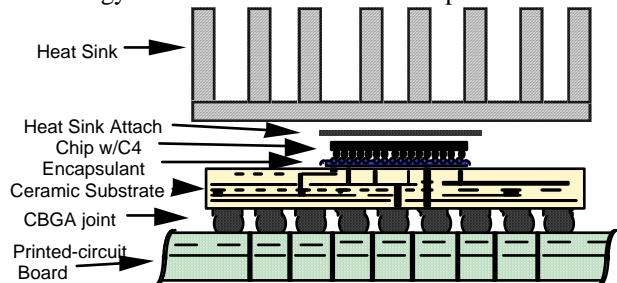

Figure 2. C4/Ceramic-Ball-Grid Array: Exploded Cross-sectional View with Optional Heat Sink (not to scale).

electrical and the mechanical connections for the die to the ceramic substrate. After the C4 solder bumps are reflowed epoxy (encapsulant) is under-filled between the die and the substrate. Under-fill material is commonly used on large high-power die; however, this is not a requirement of the C4 technology. The package substrate is a 21mm multilayer-cofired ceramic for both the PowerPC 603 and the PowerPC 604 microprocessor. The package-to-board interconnection is by an array of orthogonal 90/10 (lead/tin) solder balls on 1.27 mm pitch. During assembly of the C4/CBGA package to the board, the high-melt balls do not collapse. To optimize the availability of wiring tracks or "escapes" in the next-level interconnect (e.g., printed-circuit board), the signals are primarily located in the outer rows of the package ball array; while, the power/grounds are located in the interior region of the package.

Second-level Interconnect Technology: Land Definition
Printed-circuit board (PCB) layouts recommended for use have the surface mount pad diameter specified at 0.72mm (28.5 mils) +/-0.038mm (1.5 mils). Two suggested land patterns (referred to as a "dog bone") are shown in Figure 3 with solder-mask-defined pads and non-solder-mask-defined pads. Due to etching of copper surface features, 0.69mm (27 mil) minimum diameter measured at the top of the copper pad for a non-solder-mask-defined pad is suggested. Either hot-air-solder-level coated (HASL) or benzotriazole passivation over copper can be used successfully due to the 1.27mm (50 mil) pitch BGA footprint.

BOARD-LEVEL ASSEMBLY

CBGA packages can be attached to boards using standard SMT assembly techniques. Both clean and no-clean, rosin-based, 63/37 Sn/Pb solder pastes yield acceptable results. The paste can be screened onto the PCBs using a 0.20mm (8 mil) thick stencil, with 0.84mm (33 mil) apertures.
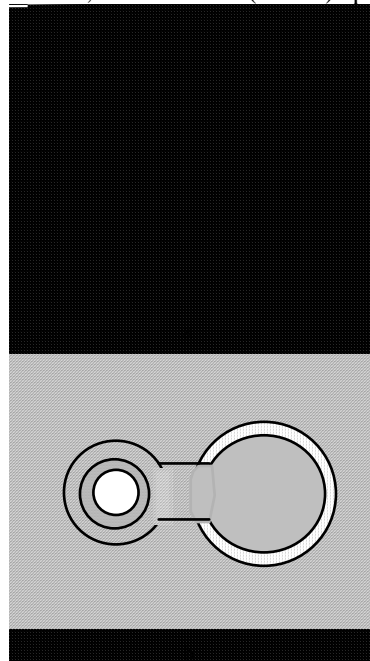

Figure 3. BGA land patterns a) solder mask-defined, b) copper-etched feature.

Component placement can be accomplished by low-cost, semiautomatic placement equipment. An acceptable method can be as simple as using split screen optics and manual placement for low volumes of packages with high yields. A more practical method for moderate volumes would involve programming a pick and place machine to pick up CBGA from a standard shipping tray and place the component into a vibratory centering fixture. Following the centering process, a vacuum nozzle would be used to place it onto the pre-programmed PCB site. Placement accuracy of up to approximately 1 pad diameter will yield acceptable results due to the self centering effects of the molten solder.

Populated PCBs can be reflowed in a conventional convection or infra-red (IR) furnace. During reflow profile development, thermocouples should be attached at interior and exterior leads to verify temperatures across a CBGA. CBGA soldering temperatures should generally peak in the range of 214 to 223°C. The ramp-up and cool-down gradients below 2°C/second, and a dwell time above liquidus should be maintained for about 75 seconds.

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ELECTRICAL CHARACTERISTICS

The total system electrical noise is influenced by the electrical characteristics of the package, as was discussed extensively in [6]. That is, the chip drivers, package parasitics and loadings in the PCB impact the total electrical noise. Electrical performance simulations that used a 3D resistance-inductance-capacitance (RLC) parametric modeling optimization study were completed on the PowerPC 603 and PowerPC 604 microprocessor C4/CBGA package (to include the impact on printed-circuit board routability) [7,8]. This section discusses electrical package performance inhibitors, package characteristics, and the system applications of the C4/CBGA package for the PowerPC 603 and PowerPC 604 microprocessors.

Package Performance Inhibitors

Package parasitics in high performance systems have a direct affect on the system performance. There are three primary areas that negatively affect performance in a package: impedance mismatches, crosstalk, and simultaneously switching outputs.

Impedance mismatch and crosstalk are controlled by the inclusion of reference planes. This addition coupled with controlling the dielectric thickness and line width controls the impedance and minimizes the coupling between adjacent lines. Simultaneous Switching Noise (SSN) is a function of three conditions: 1) the number of switching outputs, 2) the transition time (relating to di/dt) of these outputs, and 3) the package power/ground path inductance.

The appropriate number of package power/ground connections is affected by the number of ground connections to the device and the distance to the system ground. Since the PowerPC™ 604 microprocessor uses C4/CBGA technology, the power and ground connections are maximized, and the electrical path from the device to the system power and ground are kept to a minimum.

The PowerPC™ 604 microprocessor has a 64-bit external data path. This wide data path slows the bus rate; however, this is at the expense of increasing the number of switching signals. This increase causes the net current requirement for a data path event to approximately double when compared to a 32-bit external data path. This doubling will cause the current though the power/ground path inductance to also double. The effect of doubling the current will cause an increase in SSN.

To understand the data bus switching noise mechanism, an earlier version of the RISC chip with same number of data bus lines was used as a test vehicle. The chip was packaged in the 25 mm CBGA, and assembled on an application board. A special test pattern was written to identify the impact of: 1) the driver switching skew, 2) linearity of the noise level as a function of the number of switching drivers, 3) the percentage of the total noise contribution from switching noise, and 4) the crosstalk noise. The results have shown a linear increase in driver switching noise; for example, the noise doubles when 64 drivers are switched versus 32. Experimental measurements also showed negligible crosstalk noise from the CBGA package.

The SSN was monitored on the quiet line, by switching all the lines of the data path (active lines) except one (quiet line). The active lines are switched from an all high state to an all low state (data shows the falling edge to be worst than the rising edge). The quiet line was held low. Simulations for the PowerPC 604 microprocessor have shown SSN values below the noise budget of 0.7 V.

Electrical Socketing

In recent years the personal computer industry has used sockets extensively for high performance microprocessors. The disadvantage of using a socket for high performance systems is the increase in the power and ground inductance. Currently, two types of BGA sockets are available. These two types of sockets use different imbedded conductors. One uses solid metal conductors while the other uses gold filaments (similar in construction to steel wool). These conductors electrically connect the solder balls of the CBGA package to the PCB.

The BGA sockets currently available contain relatively small inductance from the package solder ball to the printed-circuit board. One might expect the power and ground path inductance to increase by 3-7%. This is primarily because the distance is small. The small inductance will have little impact on the signal electrical performance.

HEAT TRANSFER MECHANISMS AND THERMAL CONTROL OPTIONS

Primary Heat Transfer Path: Attached Heat Sink

To increase the thermal dissipation capability of this technology, a heat sink may be mated to the silicon [9,10]. In this C4/CBGA package, the silicon chip is exposed; therefore, the package "case" is the top of the silicon (Figure 2). For cases with an attached heat sink, the primary heat transfer path is as follows: heat generated on the active side (ball) of the chip is conducted through the silicon, then through the heat sink attach material and finally to the heat sink where it is removed by natural or forced-air convection. The junction-to-ambient resistance is then,

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$$\Theta_{ja} = \Theta_{jc} + \Theta_{\text{heat sink attach}} + \Theta_{\text{heat sink}} \qquad (1)$$

The silicon thermal resistance is quite small. That is, the die junction-to-case thermal resistance is 0.075°C/W and 0.033 °C/W for the PowerPC 603 and PowerPC 604 microprocessors; respectively. Therefore, for a first-order analysis the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms.

Alternate Heat Transfer Path: Conduction to the PCB
The internal-package conduction resistance terms for the alternate heat transfer path is the contribution of: C4, under-fill, package substrate, package leads/balls. For a one-dimensional model, the die junction-to-lead thermal resistance is:

$$\Theta_{jl} = 1/(1/\Theta_{C4} + 1/\Theta_{\text{under-fill}}) + \Theta_{\text{package}} + \Theta_{\text{lead}} \qquad (2)$$

The results of 3D modeling predicted the die junction-to-lead thermal resistance was 3.4 °C/W and 2.2 °C/W, for the PowerPC 603 and PowerPC 604 microprocessors; respectively.

For lower-power microprocessors, the use of a heat sink may not be necessary. This path alone may be adequate for low-power chips, however, it is a function of the board population and the system-level boundary conditions. Heat conducted through the silicon may be convectively removed to the ambient air. In addition, a second parallel heat flow path exists by conduction, through the C4 bumps and the epoxy under-fill, to the ceramic substrate for further convection cooling off the edges. Then from the ceramic substrate heat is conducted via the leads/balls to the next-level interconnect; whereupon the primary mode of heat transfer is by convection and/or radiation.

Thermal Enhancement Options: Forced-air Cooling and Heat Sink Options
Computational fluid dynamics (CFD) methods were used to solve the steady-state conjugate heat transfer problem using a commercially-available software which uses the finite-volume method [11]. The calculation domain was subdivided into cuboidal volumes. A progression in grid refinement was performed, until grid independent temperatures were achieved. A CBGA with a C4 thermal test die was utilized for model validation. Modeled and measured results were found to agree within approximately a 10% difference over the range from natural convection to 4 m/s. Once the models of the test vehicle were validated, other models were generated for the PowerPC 603 and PowerPC 604 microprocessors. The worst-case power dissipation for the PowerPC 603 microprocessor is 3 watts,

while the PowerPC 604 microprocessors is 13 watts [1,2]. Then models were run for moderate air velocity, with the package mounted to a one-signal layer printed-circuit board with no heat sink which concurs with SEMI standards [12].

For the case when no heat sink was present for an air velocity of 1 m/s, the die-junction temperature rise above ambient is 60 °C for the PowerPC 603 microprocessor and
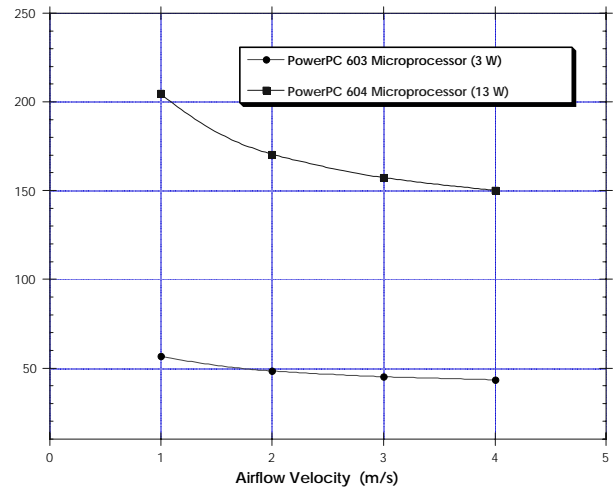

Figure 4. Model Results for the PowerPC 603 and PowerPC 604 Microprocessor (at 3 and 13 watts; respectively) Temperature Rise above the Local Ambient with No Heat Sink.
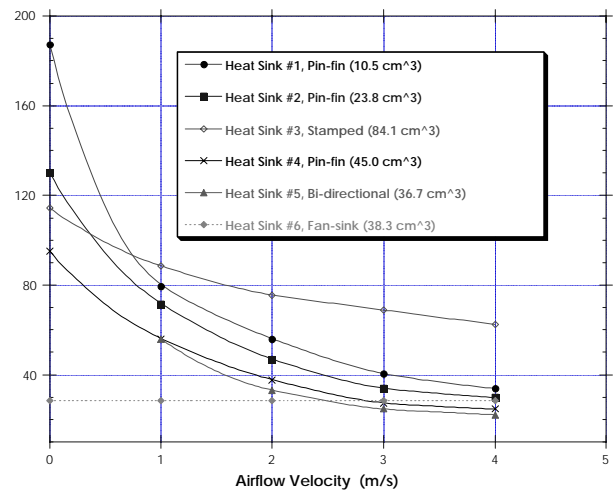

Figure 5. Model Results for the PowerPC 604 Microprocessor (13 watts) Die-junction temperature Rise for Various Heat Sink Options: Adiabatic Board.

is 205 °C for the PowerPC 604 microprocessor (Figure 4).

Typical die-junction temperatures should be maintained between 85 and 110 °C. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the computer cabinet before it reaches the component. A computer cabinet inlet-air temperature may range from 30 to 40°C. The air temperature rise within a cabinet may be in the range of 5 to 10°C. Thus, the allowable die-junction component temperature rise above ambient can range from 35 to 75 °C.

Clearly, the temperature rise for the PowerPC 604 microprocessor is too high and thermal enhancements are required. First, the internal-package thermal conduction paths were examined. The junction-to-case is silicon and its contribution to the overall heat transfer path is less than 1%. Thus, for the PowerPC 604 microprocessor, the addition of extended-surface heat sinking was the next consideration. For an adiabatic-board case, commercially-available heat sinks were modeled and the temperature rise for the 13 watt PowerPC 604 microprocessor is shown in Figure 5. This graph may be used as an initial selection guide for a variety of boundary conditions. Let us assume, for most computer systems in an office environment, a 60 °C die-junction component temperature rise above ambient is typical. Thus, three of the heat sinks would meet this criteria at 1 m/s of air velocity. If air velocity is increased further to 2 m/s, then five of the heat sinks meet this criteria. Of the passive heat sinks designs, the bi-directional offers the best thermal performance, for its relatively small spatial volume. The integral-fan pin-fin heat sink which promotes impingement airflow offers the best thermal performance; however, being an active device it requires external power. In addition, a system's designer might need to consider a "fail safe" thermal-control system in the event of a fan failure.

Board-level Component Population Considerations

Thermal performance data presented thus far has been for a single component mounted to a one-signal layer card. The next consideration is the board-level interaction effects of similarly powered neighboring components. That is, board-level thermal flux would rise with increasing component population, thereby limiting the ability of the PCB to act as a heat sink. As a case study let us consider various component population configurations for the PowerPC 603 microprocessor. For the case of a single component mounted to one-signal layer card, the die-junction temperature rise is approximately 50 °C (Figure 6). For the data presented in Figure 6, the PowerPC 603 microprocessor had a 3 watt power dissipation and an air velocity of 2 m/s, with no heat sink.

Now let us consider, the fully populated case with all nine components (at 3 watts), the center component temperature rise is approximately 135 °C. Notice that even if the center component is not powered, the die-junction component temperature rise is 90°C, due to heating from adjacent neighbors. This example demonstrates the need for microelectronics thermal engineers to conduct board-level and system-level thermal simulations to accurately predict component operating temperatures. In addition, due to the complex nature of heat transfer mechanisms, any models should be empirically validated.
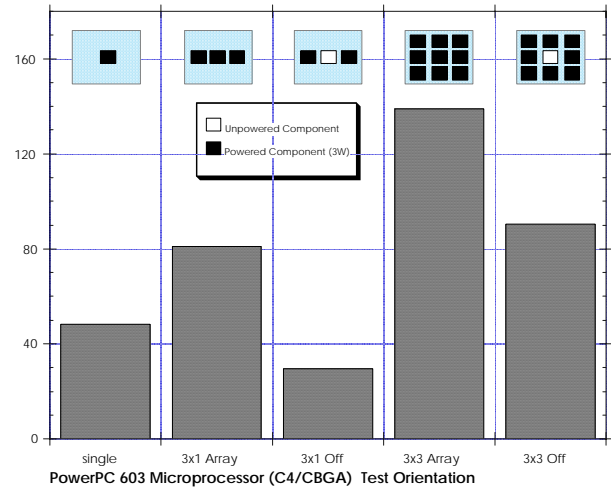

Figure 6. Model Results for the Populated Board Cases, Interaction Effects of the PowerPC 603 Microprocessor (3 watts) Temperature Rise above the Local Ambient with No Heat Sink.

CBGA-TO-BOARD SOLDER JOINT RELIABILITY

PCB Test Vehicle Description

The printed-circuit boards used to evaluate CBGA-to-board solder joint reliability testing, were 1.57mm (62 mils) thick FR-4 four-layer boards with two one-ounce copper planes in the center to simulate power and ground, and half-ounce copper on the top and bottom for signal layers. The surface mount pad diameter averaged 0.74mm (29 mils). The target diameter tolerance was 0.72mm (28.5 mils) +/- 0.038mm (1.5 mils) (Figure 3).

The BGA footprint used in this study for both package sizes was designed to be used in conjunction with a daisy chain package (without die) to detect opens. Each CBGA site had two testable chains, representing high-DNP and low-DNP joints.

Each substrate was designed to mate to the PCB dual-daisy-chain pattern so that each interconnection element

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between the substrate and PCB (ball) could be continuously monitored electrically. Each PCB had eight CBGAs. A gold-plated edge connector on each board provided 18 connections (2 commons and 16 signals), allowing two individual nets to be monitored on each part. Hot-air-solder-level (HASL) PCB finish was evaluated.

PCBs were characterized to have a glass-transition temperature (Tg) of 118°C minimum and a thermal-expansion coefficient of 21 ppm/°C in the array site (18 ppm/°C in the base material) [14].

CBGA Reliability Test Vehicle Description

Substrates (21mm and 25mm) used to study CBGA solder joint reliability were designed to mate to a PCB so that each connection to the PCB was monitored continuously during thermal cycle testing. The daisy-chain pattern on the substrate has connections made without using a C4 chip; therefore, a co-fired conductor layer is used to provide the interconnections. This technique is preferred for independent testing of the CBGA joints over others because it isolates the board interconnections (and not the other connections internal to the package).

Solder Joint Fatigue Accelerated Testing Methodology

Accelerated air-to-air temperature cycle testing for CBGA joints were cycled over a range of 20°C to 80°C (at 3 cycles per hour) for the 25mm packages [14] and 0°C to 100°C (at 1.5 cycles per hour) for the 21mm packages.

There were 40 CBGAs in each test cell. A minimum of four minutes dwell time at the temperature extremes was applied to allow creep/stress relaxation. To avoid thermal shock in the joints, the ramp rate was limited to less than 20°C/minute. The temperature cycling testing was consistent with IPC-SM-785 [15].

Electrical current was applied to the test nets, and each net was polled every ten seconds for resistance increases. A failure was defined as a resistance increase $\geq 300\Omega$ for $0.20\mu s$. The recommended failure criteria was $\geq 300\Omega$ for $>1\mu s$ [15]; therefore, the criteria used was more conservative. An event had to occur ten times within ten percent of the cycle number of the first occurrence to be considered a valid failure.

To characterize the thermal test chamber, boards (thermocoupled at the joint under test) were strategically placed to monitor test temperature. Up to nine thermocouples were used to characterize a test chamber. Temperature variation from package to package was kept under 2°C at the dwell temperatures. Throughout thermal cycling, digital and chart recorders tracked test temperatures of the air and solder joints.

When 50 percent of the nets in a given cell failed, the CBGAs in that cell were removed from the test. After visual inspection at 40 times, selected samples were crosssectioned and polished. Sorted data from accelerated temperature cycling (ATC) tests were entered into statistical analysis software. Log-normal graphs were generated to determine N_{50} (number of cycles in which 50 percent of the population of a given cell fail).

C4/CBGA-to-Board Reliability

For illustrative purposes, the fatigue-life results of the 25mm CBGA tested from 20°C to 80°C is presented in Figure 7 and is compared to 0°C to 100°C for both 25mm[16] and 21mm substrates. The CBGA wear-out mechanism follows a log-normal distribution. Final separation is characterized as a primary crack propagating through the eutectic solder at the PCB side of the high-lead ball as verified by cross-sectioning [17].

The purpose of accelerated-temperature-cycle testing is to compare the mechanical and the electrical robustness of the assembly when subjected to a thermal cyclical environment. Correlation to the accelerated temperature cycle testing and actual field use can be made by use of daisy-chain test vehicles and the application of a modified Coffin-Manson relationship [18]. Acceleration factors can be calculated to predict field-life cycles from the accelerated-stress test results.
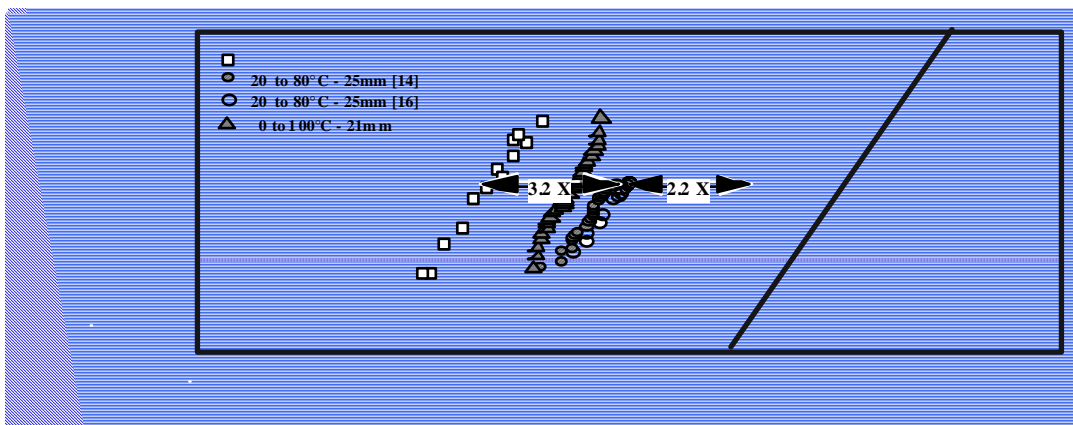
Figure 7. CBGA fatigue life distributions (log-normal) for and 25mm substrates air-to-air temperature cycled from 20°C-80°C and 0°C to 100°C compared to predictions made for the two temperature cycle conditions using Equation 3. Also, 21mm CBGA data for 0°C to 100°C is shown. Projections for a field examples are also shown for each substrate size.

The version of the Coffin-Manson equation typically used for CBGAs has been previously described[14]. For solder interconnections of a fixed geometry, the strain term can be reduced to a delta temperature term, ΔT, which comprises each thermal cycle as illustrated in equation 3.

$$AF = [\Delta T_l/\Delta T_f]^{1.9}(f_f/f_l)^{1/3}\exp[1414(1/T_{max_f} - 1/T_{max_l})] \quad (3)$$

The acceleration factor (AF) is simply a multiplier applied to a known set of data to predict the failure rate of the condition. In the case of 25°C-55°C and 20°C-80°C, the AF (or multiplier) is 2.2X (assumptions for this calculation will be presented in a later sub-section). In other words, the fatigue life of the smaller ΔT is 2.2 times longer than the 20°C-80°C case. Typically, the 50% fail value is applied to the AF factor to translate between failure distributions (Figure 7).

In consideration of the system-level thermal design options presented, the ΔT's presented in this section are considered to be typical upper bounds that may be expected during product use, 25 - 55°C [13]. Thermal excursions occur through turn-on/turn-off cycles of computer systems. The greatest reliability concern in the C4/CBGA packaging technology is solder fatigue in the CBGA joints during these thermal excursions [5]. Small ΔT's associated with the interconnect joint equate to longer life when compared to large ΔT's. Therefore, thermal management design can influence the solder joint temperature rise (ΔT's).

CBGA Solder Fatigue Life Projections
Predictions for typical computer applications were projected by using accelerated test data and the method

described as follows: a) failure distributions, such as those from Figure 7 were extrapolated down to the 0.01% (100ppm) and 0.1% (1000ppm) levels, b) the number of cycles to failure at those levels were noted, c) the number of cycles was then multiplied by an acceleration factor (Equation 3) for the temperature range of interest.

The fatigue life estimates described above are generally thought to be very conservative for the solder joints studied. The assumptions are: 1) on the average, the system would be turned on and off up to 6 times per day [Coffin-Manson 24 hour period] and 2) the system would be cycled over the full thermal excursion each and every time the system was turned on.

The maximum solder fatigue damage frequency that can be applied for most desktop office environment operating temperatures is 1 on-off cycle every 4 hours (i.e., 6 per 24 hours). This is due to the solder requiring time to stress relax at both temperature extremes (full on and full off) generated in the office environment. During the course of an average work day, which is generally considered to be 8 to 10 hours long it is probable then to accumulate maximum fatigue damage by having 2 evenly spaced on-off cycles. Cycles occurring more frequently do not accumulate as much damage per cycle as the above described situation. More frequent cycling, while higher in total number of cycles, do not necessarily accumulate more solder fatigue damage than a low number of long cycles.

The above method was utilized to make predictions for the PowerPC 603 and PowerPC 604 microprocessors both using 21mm CBGA packages. These predictions are shown in Figure 8. The assumptions used for Figure 8 were calculated to be consistent with [15]. Failure rates of

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100ppm (0.01% cumulative package failures) are plotted and failure rates of 1000ppm (0.1% cumulative package failures) can be easily calculated by multiplying the 100ppm number of cycles by 1.3.
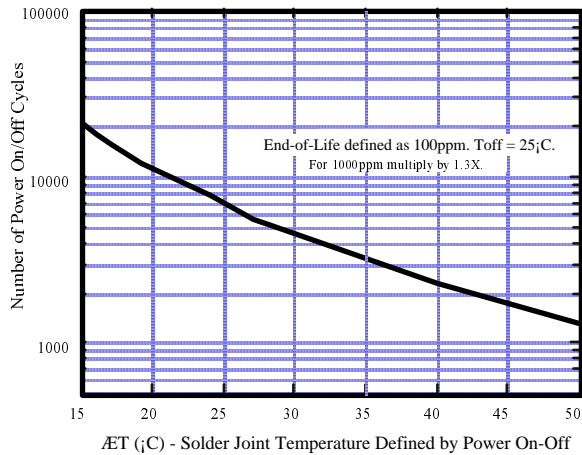

Figure 8. 21mm CBGA Solder Fatigue Field Life Projections. Each cycle is assumed to represent the full temperature excursion.

Figure 8 shows the solder joint fatigue life for the 21mm ceramic ball-grid-array (CBGA), the package for the PowerPC 603 and PowerPC 604 microprocessors to be over 10,000 cycles for an average full on/off cycle ΔT of 20°C. For a desktop computer application turned on and off on the average of one time per day, the equivalent fatigue life would be over 27 years for the 21mm CBGA. A 'worst' case desktop situation, as described above would, with 2 on-off cycles per work day would yield over 10 years

SUMMARY AND CONCLUSIONS

The following conclusions are noted:
• Assembly of C4/CBGA packages may be done with common SMT equipment and offers very low assembly defect yields when compared to similar leaded quad-flat-pack technology.

• The electrical package parasitics (RLC) are improved with the C4/CBGA when compared to similar leaded quad-flat-pack wire-bond technology.

• For airflow velocities from 1 to 2 m/s, the PowerPC 603 microprocessor, may not require heat sinking; however, heat sinking may be required if the PCB board has high thermal loading.

• The PowerPC 604 microprocessor will require heat sinking to maintain its die-junction temperature less than 100 °C. Of the passive heat sinks designs the bi-directional offered the best thermal performance for its spatial volume. Note, due to silicon die fragility any heat sink attach material must be structurally compliant. Finally, the board-level component population and system airflow are the other thermal control key factors.

• It was estimated that the solder fatigue life of a 21mm CBGA at an average on-off ΔT of 20°C to be over 27 years. Small ΔT's associated with the interconnect joint equate to longer life when compared to large ΔT's. Therefore, thermal management design can influence the solder joint temperature rise (ΔT's). Due to efficient designs, high power devices were found to have relatively cool board temperatures.

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APPENDIX

Table 1. PowerPC 603 and PowerPC 604 RISC Microprocessors [1,2]

Microprocessor	Transistors	Performance	Power	Die	CBGA Substrate	CBGA Substrate
		SPECint92/	Dissipation	Size	Size	Leads
		SPECfp92	(watt)	(mm)	(mm)	
PowerPC 603	1.6 million	75/85	3 @80 MHz (Full)	7.5x11.5	21x21	255
PowerPC 604	3.6 million	160/165	13 @100 MHz	12.4x15.8	21x21	255

Table 2. C4/CBGA Internal-Package Thermal Conduction Resistance (3D model results) [10]

Thermal Resistance	PowerPC603 Microprocessor	PowerPC604 Microprocessor
Die Junction-to-Case	0.075 °C/W	0.0329 °C/W
Die Junction-to-Lead	3.4 °C/W	2.2 °C/W

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Motorola's PowerPC 603™ and PowerPC 604™ RISC Microprocessor: the C4/Ceramic-ball-grid Array Interconnect Technology;
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