

White Paper

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*PowerQUICC III™ Overview:
Family of Next Generation
Integrated Communications
Processors*



*NCSD Business
Development*

Users of communications processors, including system architects and hardware and software engineers, have stated that their platform needs hinge on increasing processing power as well as increasing interconnect performance while lowering their overall system cost. Significant enhancements to control and data plane processing, memory, and interconnects are required to be able to serve the future needs of the imaging, networking, storage, wired and wireless communications, and general-purpose computing markets.

With the PowerQUICC III™ family of integrated communications processors, Motorola unveils the PowerQUICC III System-on-a-Chip (SoC) architecture, its latest solution designed for the needs of the embedded markets. The PowerQUICC III family of integrated communications processors alleviates bottlenecks by combining a high performance core with high-performance I/O.

This paper provides an overview of the PowerQUICC III product family and describes how it delivers enhanced integration together with performance headroom for intensive control plane processing tasks and increased forwarding plane bandwidth. This paper also highlights market and technical trends, gives a technical summary of the initial PowerQUICC III offerings, and provides specific applications examples using the PowerQUICC III as a complete solution. The following topics are addressed:

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1 Introduction

Motorola, the industry leader in communications processors with more than 5000 design wins and over 82% market share in communications processors (Gartner Dataquest), now offers its next generation integrated communications processor, the PowerQUICC III. The PowerQUICC III is the third generation PowerQUICC family, building on the success of the PowerQUICC I and PowerQUICC II families. In addition to the comprehensive functionality offered by the first members of this family, the advanced, flexible architecture enables easy integration of value-added intellectual property (IP) for future market-specific products.

Motorola's next generation integrated communications processor is positioned to be the premier integrated processor solution in many markets including wireless infrastructure, multiservice access platforms, DSLAM, edge routers, storage, switches, and media gateway. The PowerQUICC III employs a host of leading industry standards and innovative Motorola technologies including the high-performance e500 core that implements the PowerPC™ Book E architecture, RapidIO™ interconnect technology, Motorola's OCeaN crossbar switch fabric, dual gigabit Ethernet interfaces, double data rate SDRAM (DDR SDRAM), and 64-bit PCI-X/PCI interface controllers.

As a testament to its flexible architecture and System-On-a-Chip (SoC) design, the PowerQUICC III family provides two different configurations of highly integrated communications processors. The MPC8540 provides dual gigabit Ethernet interfaces, a dual universal asynchronous receiver transmitter (DUART), a four-channel direct memory access (DMA), a multi-channel interrupt controller, one 10/100-Mbit Ethernet interface, a double data rate (DDR) SDRAM memory controller, a 64-bit PCI-X/PCI controller, and a RapidIO interconnect. Raising the bar even higher, the MPC8560 offers a full feature set including an enhanced PowerQUICC II compatible communications processor module (CPM) in addition to all of the features of the MPC8540. PowerQUICC III's CPM is a higher performance version of its predecessor in the PowerQUICC II family operating at speeds of up to 333 MHz and incorporating support for new microcode packages. The CPM features three fast serial communications controllers (FCCs), two multi-channel controllers (MCCs), four serial communications controllers (SCCs), one serial peripheral interface (SPI), and one I²C interface. The CPM is software compatible with the PowerQUICC II family, providing the opportunity to leverage previous investments in Motorola's PowerQUICC architecture.

2 Market Overview

Trends in the networking and telecommunications markets are driving the need for more processing capability to handle more complex algorithms, larger and faster memory subsystems, and higher bandwidth communications as the amount of data to be processed and forwarded increases. Also, there is an increasing demand for tailored services and interworking capability as IP, TDM, ATM, and other protocols are leveraged across existing core networks.

Communications protocols are becoming more complex and are demanding higher performance in communications processors. Traffic engineering techniques in the enterprise routing realm are becoming more complex in order to better control the flow of packets inside an IP network. More complex encapsulation protocols such as multi-protocol label switching (MPLS) provide explicit flow control, but require greater processor involvement. These techniques as well as continuing growth in infrastructure networks will cause a predicted increase in the size of routing tables by 20% in the next year. New routers must support features like multicast, quality of service (QoS), voice, and security, all of which increase the complexity of IP forwarding.

As the number of wireless subscribers double, going from one billion today to a predicted two billion in 2005, the demand for customized and tiered applications and services will become more apparent. Services

have become the differentiator for service providers, and thus, they have the challenge of personalizing their service packages. Consolidating IP functionality and voice over IP (VoIP) gateway functionality in DSLAMs will, for example, allow more services to be offered in the DSL market.

Today there are several types of networks that communicate via a range of different protocols such as frame relay, IP, TDM, and ATM based standards. Since no single protocol yet dominates the communication industry across all markets and support for existing infrastructure investments will be needed into the foreseeable future, interworking between protocols and equipment will continue to be essential.

The following discusses how the PowerQUICC III addresses many of the above concerns facing companies developing solutions for communications markets.

Answering the high performance needs of the industry, the Book E architecture e500 core performance yields up to 2.3 MIPs/MHz (est. Dhrystone 2.1) and also contains a signal processing engine (SPE) designed to perform some DSP signal processing tasks such as FFT, FIR, matrix operations, 64-bit load/store operations, and more. The PowerQUICC III core complex also includes a 256-Kbyte second-level (L2) cache, configurable as high-speed local SRAM that can facilitate content-aware IP forwarding by allowing fast examination, storing, and accessing of IP buffer descriptors. This fast memory is located close to the core to reduce latency issues. The integrated double data rate memory controller will yield higher memory bandwidth overall allowing data rates of up to 333 MHz.

The CPM contains a dedicated RISC processor optimized for handling communications and protocol handling tasks. The functionality supported by this on-chip resource allows implementation of critical protocols like ATM Adaptation Layer 2 (AAL2) for important functions such as VoIP and can be modified via downloadable microcode as well. The CPM functionality enables interworking between different protocols.

To support the system need for high bandwidth, high reliability, low latency connections between the various critical components (either on a single board or between boards in a chassis), the PowerQUICC III is equipped with a high-speed point-to-point interface called RapidIO. This technology is specifically designed for high-performance embedded markets. RapidIO, in conjunction with dual gigabit Ethernet controllers and legacy support such as PCI and 64-bit 133 MHz PCI-X, ensures that the PowerQUICC III family provides high performance interconnect capability in conjunction with standard programmable interfaces for easy interoperability.

Simply stated, the PowerQUICC III with its 1 GHz-capable core, 166 MHz (333 MHz data rate) DDR memory bus, 333 MHz CPM, and a host of other key features empowers the networking and communications industry to address the technical challenges facing industry today and in the future.

3 Feature Introduction

Motorola's leading PowerQUICC III architecture integrates two main processing blocks as shown in Figure 1. One block is a high-performance embedded e500 core; the other is the communications processor module (CPM). A description of the e500 core and its performance enhancements follows. Next, the DDR SDRAM memory controller, integrated 10/100/1000 Ethernet controllers, 64-bit PCI-X/PCI controller, RapidIO interconnect, and the CPM offered with the full feature MPC8560 implementation are included in the feature lineup.

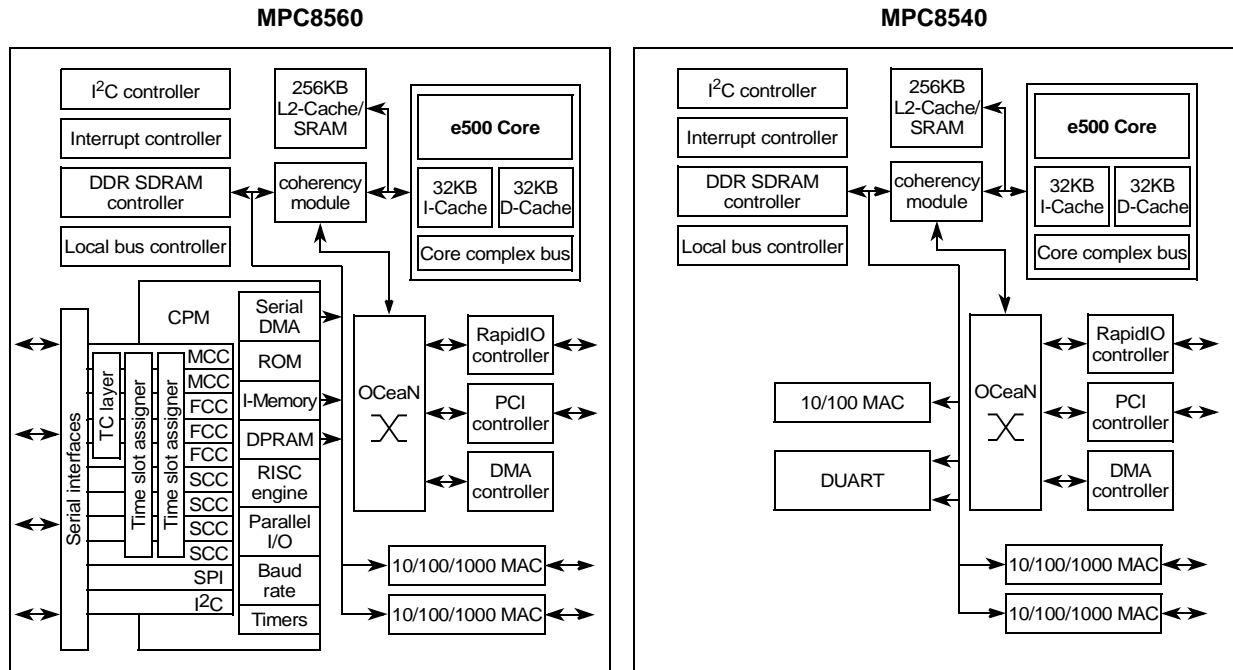


Figure 1. MPC8560 and MPC8540 Architectural Overview

3.1 e500 Core

The PowerQUICC III contains an e500 core for processing PowerPC architecture instructions. The e500 core provides 64-bit general-purpose registers (GPRs), but implements the 32-bit portion of the Book E architecture. This high performance core operates at up to 1 GHz yielding 2.3 MIPs/MHz.

The PowerQUICC III family of communications processors contain numerous micro-architectural improvements over previous communications processors that implement the PowerPC architecture. One of the main changes is the addition of a signal processing engine. The signal processing engine provides 222 new instructions that accelerate typical signal processing functions such as FIR filtering and FFT algorithms. In addition, the SPE load/store instructions can speed up generic load/store operations. Single-instruction, multiple-data operations included in the SPE package provide a cost effective technique for accelerating computation. The SPE is unique in that it can operate on integer, fractional, and single-precision floating-point data.

Additional performance enhancements have been implemented in the e500 core such as improved branch prediction and prefetch-under-miss, out-of-order issue, deeper store queue, and improved support for critical interrupts. The e500 core also includes multiple simple execution units which allow for parallel instruction execution.

3.2 System Architecture

There are several noteworthy features implemented in the highly integrated PowerQUICC III SoC architecture. Among this set of features are the:

- On-chip memory unit
- e500 coherency module (ECM)
- Local bus

- On-chip network (OceaN)
- Embedded programmable interrupt controller (PIC)
- Direct memory access controller (DMA)

This architecture is shown in Figure 2.

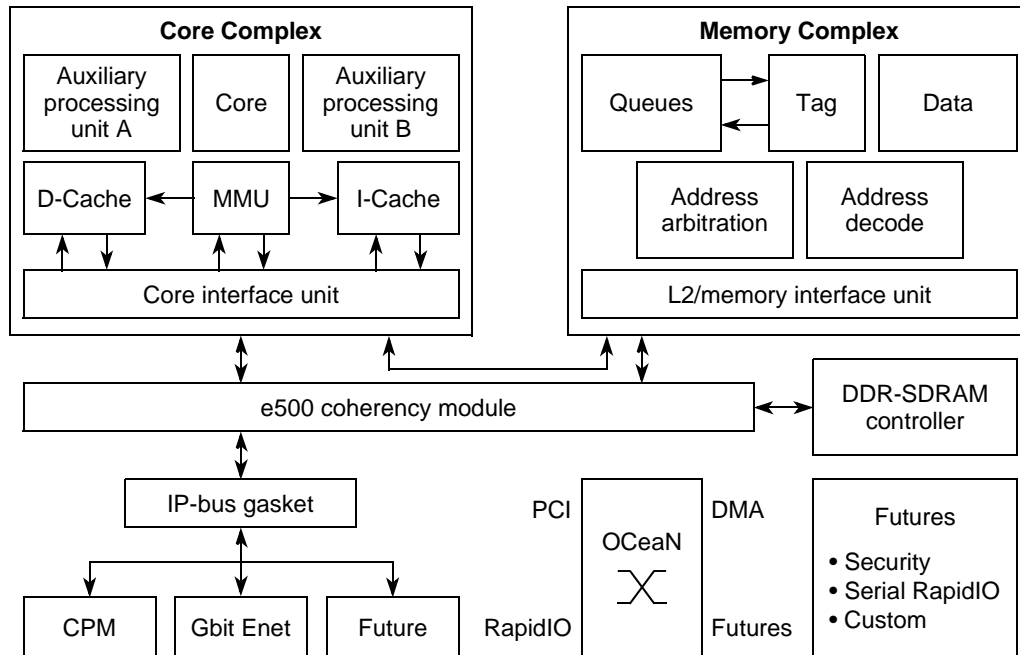


Figure 2. PowerQUICC III SoC Architecture: System-on-Chip with Building Blocks

3.2.1 On-Chip Memory

The on-chip memory unit is an internal 256-Kbyte memory array that can be configured as memory-mapped flexible SRAM, as a look-aside L2 cache, or a combination of 128-Kbyte SRAM with a 128-Kbyte L2 cache. This unit serves as high speed externally accessible memory that can be used to store buffer descriptors or as supplemental cache. Configured as cache, the unit supports locking of the entire cache or selected lines and supports streaming on input or output data buses. SRAM operation supports relocation and is byte accessible. The on-chip memory unit comes equipped with ECC protection for the data in both cache and SRAM memory arrays.

Performance enhancing features of the on-chip memory unit include the ability to reduce memory access latency by allowing external devices (PCI/X, RapidIO, Ethernet, CPM) to write data directly into the L2 cache while also writing to main memory. This is known as ‘stashing.’ The locking mechanism implemented, guarantees that data can be protected to ensure that it will not be evicted due to capacity invalidations. Two key benefits of this feature are the reduced latency and increased bandwidth. Latency is reduced due to the L2 being physically located closer to the core (and other devices) than external DDR SDRAM main memory, thus allowing for faster completion of reads and writes compared to off-chip memory. Frequently accessed data can be placed in on-chip SRAM so that any updates are now on-chip, eliminating additional write traffic to off-chip main memory, leaving more DDR bandwidth for other data traffic. Because the on-chip memory unit is fully pipelined, and can provide data at the rate of 128 bits/cycle, on-chip memory provides increased bandwidth resulting in twice the maximum theoretical bandwidth provided by even that of the DDR SDRAM controller.

3.2.2 e500 Coherency Module (ECM)

The e500 coherency module (ECM) is the hub of the PowerQUICC III processor. It forms a platform for building SoCs, and maintains coherency between I/O traffic to DDR memory, memory on the local bus and the e500 L1 and L2 caches. It is also optimized for low latency access to DRAM.

A central, extensible switching component, the ECM routes request and data traffic among the core, L2 cache, OCeaN peripherals (RapidIO, DMA, and PCI), system memory, the three-speed Ethernet controllers, the CPM, the I²C controller, the local bus controller, and the DUART. Speculative reads, a low latency data return bus, and request streaming are some of the noteworthy latency reducing features of the ECM.

The ECM is equipped with a speculative read bus that provides early speculative dispatch of read requests to local, prefetchable system memory regions. Speculative reads reduce memory access latencies by permitting page and bank lookup to begin three to four cycles earlier when no pending memory requests are being serviced. A dedicated low latency data bus returns system memory read data to the core. This direct data path reduces data latency by removing the need to access the potentially heavily loaded shared global data bus to return read data to the core. The ECM is able to stream successive requests from any given master, and can dispatch a new transaction every cycle.

3.2.3 Local Bus

The local bus controller port allows connections with a wide variety of external memories, DSPs, and ASICs. The address pins are multiplexed with the 32-bit data bus to keep pin count low. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip-select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The user-programmable machine (UPM) can be programmed to create simple or complex timing patterns to interface to synchronous devices or custom ASIC interfaces. The SDRAM machine can be used to control single data rate synchronous DRAM. An internal delay-locked loop (DLL) is used for local bus clock generation to optimize timing margins for board designs. Frequencies up to 166 MHz are supported. Each of the eight chip selects can be configured such that the associated chip interface can be controlled by the GPCM, UPM, or SDRAM controller. All three may exist in the same system. The local bus supports up to 2 Gigabytes of address space per chip select and also provides parity support.

3.2.4 On Chip Network (OCeaN)

The on-chip network (OCeaN) provides a four-port interconnect fabric enabling fast communication between the RapidIO controller, PCI/PCI-X controller, DMA controller, and e500 coherency module. The OCeaN fabric supports a split transaction, packet based, request/response protocol. It is a priority based interconnect, assigning each packet a priority by the device connected to the source port. Because each OCeaN device connects to the OCeaN fabric through independent source and destination ports, a device can send and receive simultaneously. Each port can transfer up to 64 bits of data per OCeaN clock cycle (up to 333 MHz) yielding a peak cross-sectional bandwidth of 85 Gigabits/sec. The switching fabric can post up to six transaction requests before receiving a grant to service the first request, enabling more efficient use of the fabric when heavily loaded. Support of request reordering allows a request to another port to pass a blocked transaction ahead of it. The OCeaN fabric arbiter uses the assigned priority to avoid deadlock and guarantee forward progress and provides per port arbitration with completion priority arbitration. The OCeaN fabric also facilitates future IP block reuse at each port.

3.2.5 Programmable Interrupt Controller (PIC)

The embedded PIC implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC unit is an extension of the MPC8245 PIC. Sixteen programmable interrupt priority levels are supported. It provides for 12 external interrupts (with fully nested interrupt delivery), 4 message interrupts, 4 global high resolution timers with interrupts, plus 32 other internal interrupt sources. The PIC adopts the OpenPIC architecture and implements the logic and programming structures according to that specification. Control bits in the PIC configuration registers for each interrupt allow OpenPIC processing of interrupts to be bypassed. In these cases, the interrupts can be routed to either the critical interrupt input of the e500 core or to an interrupt output pin for external processing. Interrupt summary registers in the PIC programming model allow for fast identification of the interrupt source in these cases.

3.2.6 DMA Controller

The PowerQUICC III device provides a general purpose four-channel hardware DMA controller in addition to the dedicated DMA engines private to each of the on-chip Ethernet controllers and the CPM. This general purpose DMA controller supports direct data movement among RapidIO, PCI, PCI-X, and the local bus interfaces, including the local address space and local memory. Transfers may be initiated and controlled by the core or by remote masters.

The DMA controller resides on the OCeAN crossbar and can transfer up to 64 bits per cycle at the OCeAN clock frequency (333 MHz), yielding a peak bandwidth capacity of 21.3 Gigabits/sec. The DMA controller's programming model was designed to work efficiently with RapidIO devices. The PowerQUICC III DMA controller also supplies a programmable channel bandwidth-limiting mode to avoid starvation when multiple channels are executing transfers concurrently or when the channel's operation is controlled by an external master. Additionally, it affords software the flexibility of having the DMA controller begin processing descriptors that have already been built, while software simultaneously continues to construct more descriptors in memory. This capability comes from its programming model that allows software to configure each of the four DMA engines independently and to interrupt on completed segment, chain, or error conditions. The DMA controller supports three external hardware handshake pins for each channel providing a request/acknowledgement mechanism.

3.2.7 Dual Data Rate SDRAM Memory Controller (DDR SDRAM)

The PowerQUICC III has a 64-bit interface and supports DDR-I SDRAM clock frequencies up to 166 MHz (enabling a 333 MHz data transfer rate). DDR SDRAM technology is a derivative of the SDRAM standard. The PowerQUICC III implementation was designed to be low latency to the processor and allows for DDR SDRAM banks to be built using DIMMs or directly-attached memory devices. Fifteen multiplexed address signals provide for device densities of 64 Mbits, 128 Mbits, 256 Mbits, 512 Mbits, and 1 Gbit. Four chip select signals support up to four banks of memory. Each bank supports up to 1 Gbyte of memory.

The DDR SDRAM controller has two main modes of operation optimized for the expectation of spatial locality of memory accesses: page mode and auto-precharge mode. Page mode supports up to four simultaneous open pages per chip select and subsequently can dramatically reduce access latencies for page hits. Other features of the DDR SDRAM memory controller include the ability to employ continuous or discontinuous memory mapping along with read-modify-write transactions for RapidIO atomic increment, decrement, set, and clear operations. Sleep support for self-refresh SDRAM and support for auto-refreshing is provided. The controller has on-the-fly power management using the clock enable signal and has 2.5-V SSTL2 compatible I/O. Additionally, the DDR SDRAM memory controller supports full ECC with single-bit error correction and double error detection possible.

3.2.8 Three Speed Ethernet Controller

The PowerQUICC III has two three-speed Ethernet controllers (TSECs) serving as general-purpose, high-speed communication links. Each TSEC incorporates a media access control sublayer (MAC) that supports 10-, 100-, and 1000-Mbit/sec Ethernet/802.3 networks with MII, GMII, RGMII, TBI, and RTBI physical interfaces. Each TSEC includes DMA functions, support for jumbo frames (up to 9.6 Kbytes), and programmable CRC generation. Additional noteworthy features of the TSEC include a 256-entry hash algorithm for individual and multicast addresses and the ability to store headers directly into the L2 cache.

3.2.9 PCI/PCI-X Controller

The PowerQUICC III provides an interface that supports legacy peripheral component interconnect (PCI) or high-speed PCI-X connections. When configured for PCI 2.2 compatibility, the interface supports operation up to 66 MHz, and can be configured for either 64-or 32-bit PCI bus widths, an enhancement from the previous generation of PowerQUICC processors. The interface supports the 64-bit dual address cycle (DAC).

The PowerQUICC III further supplies host and agent modes. On-chip arbitration with support for five request and grant signal pairs provide value through integration. The high-performance interface offers PCI-to-memory and memory-to-PCI streaming, as well as memory prefetching of PCI read accesses and posting of PCI-to-memory and processor-to-PCI writes. Snooping of inbound accesses is also configurable.

When configured for PCI-X 1.0a compatibility, the interface allows point-to-point connections with frequencies up to 133 MHz and bus widths of either 32-or 64-bits. The controller supports up to four outstanding split transactions. All PCI-X ordering rules are enforced, but a relaxed-ordering configuration can also be enabled.

3.2.10 RapidIO

The RapidIO interface unit on the PowerQUICC III is a high-performance, point-to-point, source-synchronous, low-pin count, packet-switched system level interconnect that can be used in a variety of applications. It delivers significantly greater bandwidth, scalability, and reliability than other interconnects used today. The RapidIO controller is a key enabler in the networking and communications industry supplying the much desired replacement for proprietary interconnects by providing an open standard solution addressing the high performance embedded market. The RapidIO architecture provides a rich variety of features including high data bandwidth, low-latency capability, as well as support for message-passing. The RapidIO unit on the PowerQUICC III communications processor is based on version 1.2 of the *RapidIO Interconnect Specification*. It supports the I/O and message passing logical specifications, common transport, and the 8/16 LP-LVDS physical layer RapidIO interconnect specifications.

The PowerQUICC III RapidIO controller includes support for 4 transaction priority levels, ordering within a priority level, CRC error management, single-byte to 256-byte transactions, and 8-bit wide data ports. The physical layer of the RapidIO unit can operate at applied clock frequencies of up to 500 MHz. Because the interface is defined as a source-synchronous, double data rate, LVDS signaling interconnect, the theoretical unidirectional peak bandwidth is 8 Gbit/sec for an 8-bit port. However, separate receive and transmit ports operate independently, resulting in an aggregate theoretical bandwidth of 16 Gbit/sec. See <http://www.rapidio.org> for more information on RapidIO.

3.2.11 Communications Processor Module

The MPC8560, the full featured integrated communications processor in the PowerQUICC III family, implements an embedded 32-bit RISC controller as a part of its high performance communications module (CPM) operating at 333 MHz. The CPM is the communications center of the PowerQUICC III processor providing internetworking capability for ATM, TDM, Ethernet, and other protocols while maintaining software compatibility with the PowerQUICC II. The CPM supports three fast serial communications controllers (FCCs) optimized for synchronous high-speed data protocols and supporting 10/100 Mbit/s Ethernet, ATM up to OC-3 rates, and high-level data link control (HDLC) up to T3/E3 rates. The CPM supports, in addition, 2 multichannel controllers (MCCs) handling up to 256 channels of HDLC or transparent protocols. The CPM provides four serial communications controllers (SCCs) used for supporting HDLC, HDLC bus, transparent mode, UART, Bisync, and Appletalk/Localtalk. Additionally, the CPM comes equipped with one serial peripheral interface (SPI) and an I²C interface. CPM ROM microcode implements protocols such as AAL1 circuit emulation service (CES) and RAM microcode packages for protocols such as Signaling System #7 (SS7) and AAL2. The combination of the e500 core and the CPM, along with the versatility and performance of the MPC8560, provides enormous potential to system designers developing networking and communications products. The CPM block diagram is represented in Figure 3.

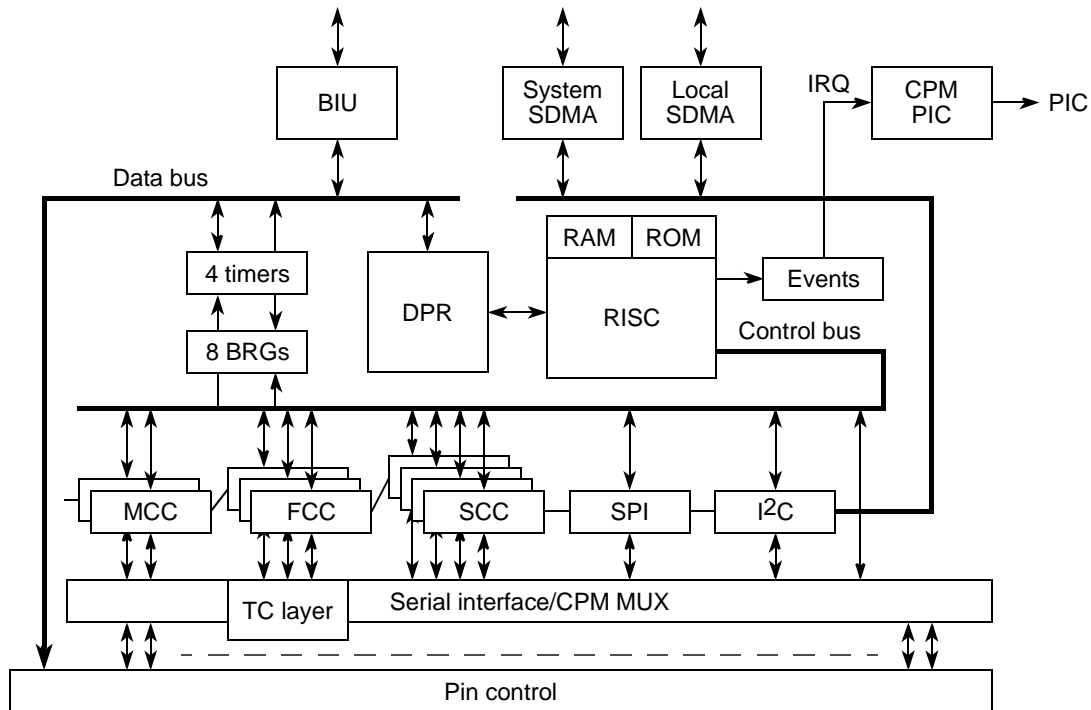


Figure 3. CPM Block Diagram

Performance enhancements include the local bus having optimizations to handle CPM performance such as support of non-standard transfer sizes on the SDRAM controller, that is, for access to ATM connection tables. The direct local bus connection reduces the load that the CPM causes on the main bus.

The CPM can handle lower-layer tasks and DMA control activities while leaving the e500 core free to handle higher-layer tasks. The CPM, therefore, offers relief to the system core as a satellite processing element, suitable for small, often repeated protocol handling tasks. This offers the potential to free up the CPU to perform control plane or other processing intensive activities.

The existing microcode packages developed initially for the PowerQUICC II product family are directly portable to the PowerQUICC III, and add value by enabling higher-level functions such as ATM switching, inverse ATM multiplexing (IMA), and automatic ATM-to-Ethernet switching to list just a few. Users may potentially simplify their designs by leveraging one or more of the microcode sequences in this list. The multi-service platforms (MSP) microcode is one such example. It implements most of the ATM layer functionality, which includes most of the general switching, traffic shaping, policing, and operations, administration and management (OAM) functions, as well as provides support for additional features such as multi-cast. In a variety of applications, such microcode adds significant value by performing functions using the CPM that would otherwise require additional external components or place an additional burden on the CPU. It is clear that in many applications, the CPM is an essential resource. See the *MPC8560 PowerQUICC III™ Integrated Communications Processor Reference Manual* for more information about the CPM and how it can be employed.

3.2.12 Debug Support

The PowerQUICC III includes several features, that together comprise noteworthy debug capability. The e500 core provides enhanced levels of hardware and software debug support compared to previous cores that implement the PowerPC architecture, such as instruction and data breakpoints and program trace mode. Access to the internal debug mode facilities is provided using Book E architecture instructions as well as through the debug interrupt mechanism. There is also a substantial level of debug support for the major interfaces, such as the local bus interface, the DDR SDRAM interface, and the PCI interface. In addition to the external interfaces, the PowerQUICC III provides triggering capabilities based on user programmable events and internal visibility to the local processor interface, and the RapidIO interface via the watchpoint and trace buffer features.

The PowerQUICC III has IEEE 1149.1 compliant JTAG boundary scan capabilities. There are two common on-board processors (COPs), one on the core complex and one for the remaining logic on the integrated device. The system access port uses the JTAG port to access the system memory map, allowing for debug and run control. Pin visibility is provided at these major interfaces: PCI/PCI-X, local bus interface, and DDR DRAM interface. Limited visibility, through a 256×64 trace buffer, is also provided for the local processor interface and on the internal RapidIO outbound interface. All of this visibility can help the user debug the system and software through inverse assembly and reconstruction of the fetch stream.

In addition to the visibility aids, other debug features such as internal and external triggering via programmed modes in the watchpoint monitor and trace buffer, can be very useful in system debug. The watchpoint monitor can be programmed to assert the TRIG_OUT signal when a programmed event occurs. The trace buffer block can be used as a second watchpoint monitor. The watchpoint monitor and the trace buffer can be triggered by one another, a performance monitor event, or from an external source via the TRIG_IN signal.

4 Applications

With their processing power and strong interconnect capability, the MPC8540 or MPC8560 can serve in many applications, whether it functions as the only processor in the product, the system controller that controls ASICs or other processors, as a control processor on a line card subject to the coordination of the system controller, or as a data plane processor utilizing the CPM functionality. The MPC85xx family is targeted to provide solutions in various application contexts such as cellular base-stations and radio network controllers, high-end switches, edge routers, firewall and other packet filtering processors, network processor controllers, control plane processors for high-end routers, VPN controllers (in conjunction with security processors), VoIP controllers (in conjunction with DSPs), network attached storage (NAS)/storage

area network (SAN)/network file system (NFS) storage controllers, and a wide range of industrial control applications outside the typical network communications domain, including automotive and even desktop applications.

Though just a sample of the applications that can be realized using the PowerQUICC III, five applications are detailed in this section to illustrate the applicability of the PowerQUICC III in today's communication and networking applications. This section will show the PowerQUICC III as a key element in the following: a wireless 3G base station, an enterprise router, a storage area network, a DSLAM, and a media gateway application. The example applications show the flexibility a system designer has in implementing a communications system using the PowerQUICC III. Although these applications are only shown at a high level, it is still clear that the functionality offered by the PowerQUICC III family makes it suitable in a broad range of applications.

4.1 3G Wireless Infrastructure

Third generation (3G) base station controllers (BSCs) also referred to as radio network controllers (RNCs) serve as the bridge machinery between traditional circuit-switched portions of the network and new packet-switched portions of the network. The RNC is the intelligence in the base station subsystem (BSS) that handles all functionality involved with management of the radio path. An RNC typically has two different planes: the control plane and the interface plane. The control plane is central for control of all internal RNC elements, disk management, Ethernet access, memory management, traffic management, and switching.

The PowerQUICC III can be employed to realize much of the RNC's functionality. The interconnect between the two planes can be implemented using one or more of the high-performance interconnect facilities offered with the PowerQUICC III, including the OC-3 interface, Ethernet, PCI, or RapidIO. The PowerQUICC III is especially suitable for the disk or for memory management with its high-performance DDR SDRAM controller and local bus interface. Gigabit Ethernet links can be utilized for connecting the CPU to other operation and maintenance control portions of the network with which the RNC must communicate. Serial communications controllers, the serial peripheral interface, and the inter-integrated circuit controller (I²C) included in the CPM offered with the MPC8560 controls I²C devices, such as microcontrollers, EEPROMs, real-time clock devices, A/D converters, and LCD displays. The other channels of the CPM (FCCs, MCCs, SCCs, etc.) allow the ability to interface with a wide variety of WAN standards (ISDN, ATM, etc.), LANs, and proprietary networks. Depending on the configuration and requirements of the system, the PowerQUICC III allows connectivity to T1/E1/J1 framers, T3/E3 framers, or OC-3/STM-1. Also featured are an eight-channel ATM-TC layer for T1/E1/J1 or DSL and support for inverse ATM multiplexing for connection through the UTOPIA multi-PHY as well as the built-in ATM-TC layer.

The communications module has been optimized to support a wide variety of industry leading DSP banks on the local bus. This configuration is shown in Figure 4.

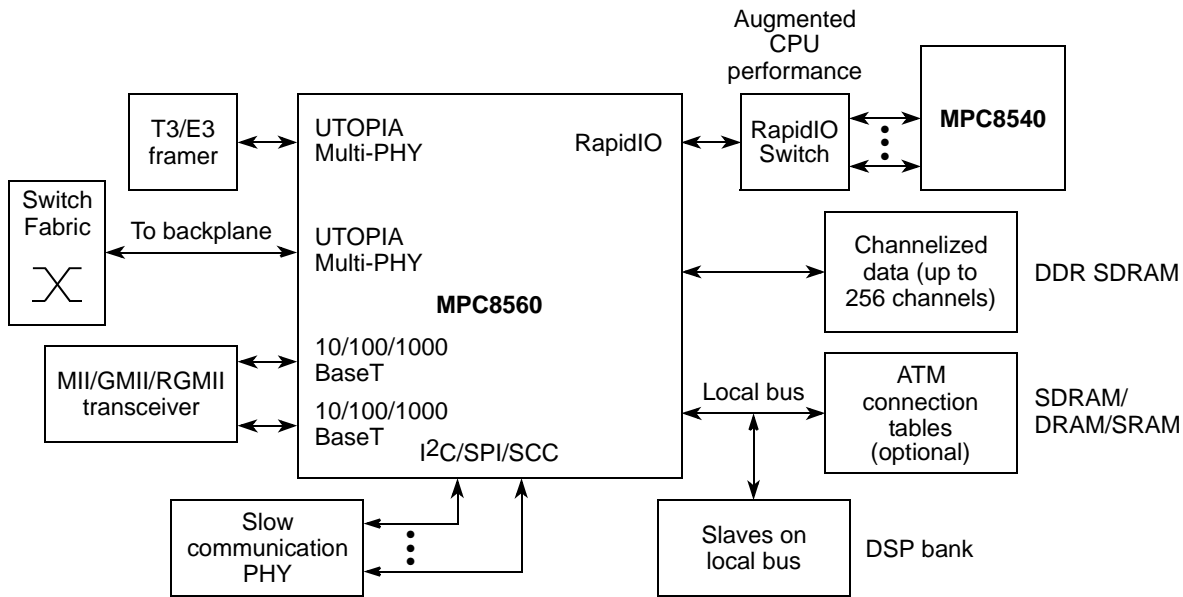


Figure 4. Wireless 3G Base Station Controller

An important issue to be considered is the transport protocol transition in 3G networks. Infrastructure providers and wireless network operators need the ability to migrate the existing installed base and develop new designs that support both ATM and IP protocols. Release 3 systems are currently being deployed supporting the ATM transport network layer. Release 5 will specify support for an TCP/IP-based transport network layer providing operators the choice of implementing TCP/IP or ATM transport. The PowerQUICC III processor supports an IP-based network with its TDM and gigabit Ethernet interfaces and also supports ATM interworking using its UTOPIA interfaces. The PowerQUICC III provides an efficient TCP/IP to ATM interworking solution.

The PowerQUICC III offers a considerable range of flexibility and has the performance to offer a complete solution in this application. It provides essential functionality for a radio network controller while incorporating other equally important capabilities such as redundancy in links, unit level high-speed interconnect, and glueless interoperability with system elements. The PowerQUICC III encapsulates all such functionality making it possible to easily provide performance, quality, reliability, and simple enhancement capability for the wireless infrastructure market.

4.2 Enterprise Edge Router

Edge routers transfer data between one or more local area networks (LANs) and wide area networks (WANs) such as an ATM backbone network. These routers additionally provide intelligence to manage traffic for each network segment. The PowerQUICC III enables a viable solution for such systems by providing a high-speed core with a closely located memory controller and fast interconnect options such as RapidIO for unit connections within the system. These PowerQUICC III features enable a true ‘high touch’ packet system for surpassing the normal processor tasks of exception handling in router applications and supplying a means to perform sophisticated packet classification.

An implementation of a regional office/enterprise router is depicted in Figure 5, utilizing the PowerQUICC III dual gigabit Ethernet interfaces for LAN connections and OC-3 ATM interfaces for the WAN side connection. DDR SDRAM, RapidIO enabled peripherals, and a direct interface to most physical layer (PHY) devices are depicted in Figure 5. In ATM mode, the local bus is used to store connection tables for active ATM connections. Additional ports remain available for system management functions.

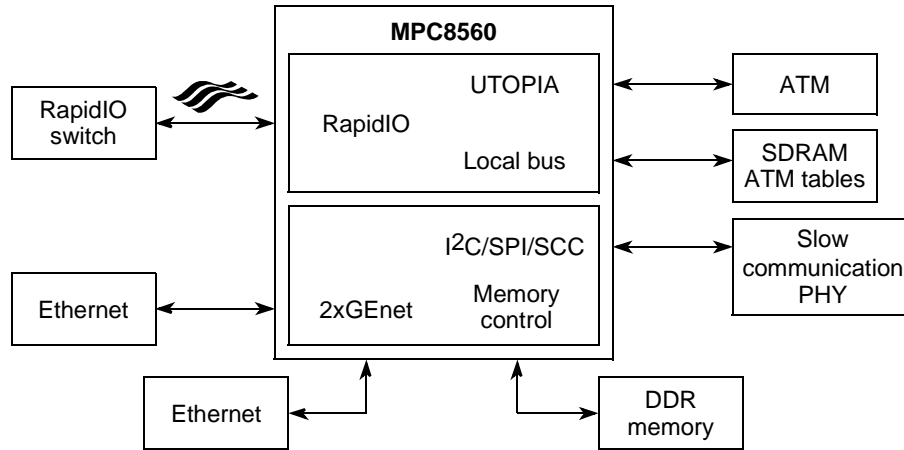


Figure 5. Regional Office/Enterprise Router

The PowerQUICC III offers a solution that incorporates high-speed interconnectivity with high-performance processing capability. Designs such as shown in Figure 5, along with similar solutions, can be employed in access, edge, and can be used with a network processor for high-end systems. The SoC architecture provides the flexibility for the CPM or other components of the system to be removed yielding such products as the MPC8540 and potentially other future derivatives of the PowerQUICC III that will have the capability to deliver greater performance flexibility for router applications.

4.3 Storage Networking—RAID Controller

With the expansion of data-intensive applications such as data warehousing, e-commerce, and broadband video delivery, the performance demands on storage are skyrocketing. These increasing demands are coupled with a strong need to manage this storage effectively from both a cost and performance point of view. It is estimated that by 2005, up to 70% of typical IT budgets will be devoted to various aspects of storage, from storage networking devices, disk, tape and other storage devices, and storage management software.

Redundant arrays of inexpensive disk (RAID) technologies have improved the performance and cost-effectiveness of storage in mainframe and enterprise environments by enabling multiple small disks to operate together as a single storage system. Storage networks are now delivering the promises of this technology to the general information technology market. Figure 6 shows a generic storage area network (SAN), which connects the traditional Ethernet LAN/WAN to various storage devices. This SAN design takes into account the unique performance and reliability requirements of storage networking relative to regular Ethernet networks. Figure 7 shows an MPC8450 as the control processor on a RAID controller card, an important device that connects RAID storage to the storage network.

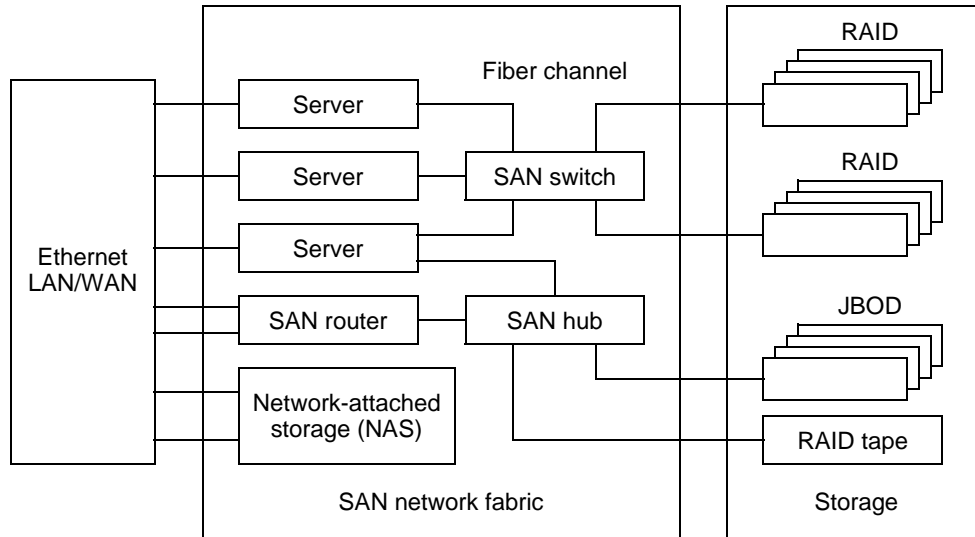


Figure 6. Storage Area Network

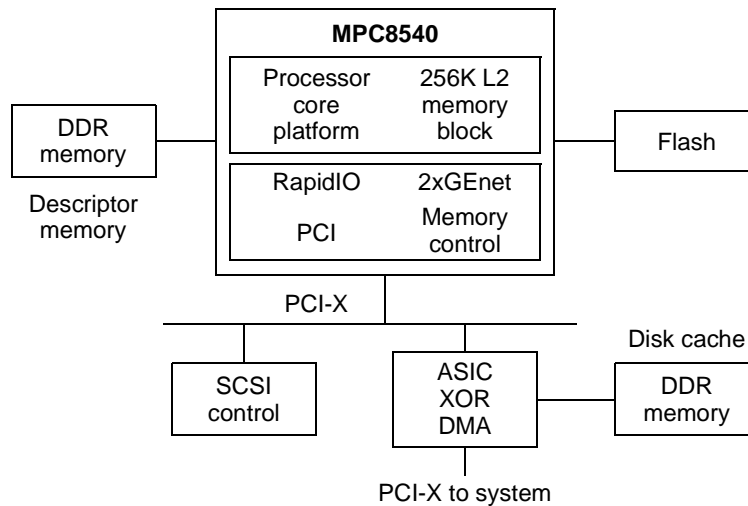


Figure 7. MPC8540 in RAID Controller Card

RAID controller cards are used to interface RAID devices to the storage network. They are similar to a bridge adapter used to connect servers to networks; however, they also implement RAID algorithms with additional hardware functionality. The application in Figure 7 shows the MPC8540 connected to the disk drives via the PCI-X bus.

With its high level of integration, memory interfaces, and PCI-X and local bus support, the PowerQUICC III delivers a feature set that is suited for storage networking infrastructure applications. Features such as the DMA engine offload data path FPGA management allowing more of the 2.3 MIPS/MHz of processor power to be applied to boosting system performance. The on-chip memory controller and DDR SDRAM interface reduce critical memory access latency. On-chip configurable SRAM on the PowerQUICC III provides additional means to reduce memory access latencies. Applications such as SAN switches or SAN host bridge adapters will also benefit from the feature set of the PowerQUICC III. The PowerQUICC III is a useful solution for the storage networking market both for storage devices including RAID and networking fabric devices such as directors and switches providing interconnection between the application servers and storage devices.

4.4 Digital Subscriber Line Access Multiplexer (DSLAM)

The PowerQUICC III can serve as the solution in multi-service access platforms that manage different communications media. Digital subscriber line access multiplexers (DSLAMs) facilitate the connection between the public network and residential, small business, and enterprise subscribers as shown in Figure 8.

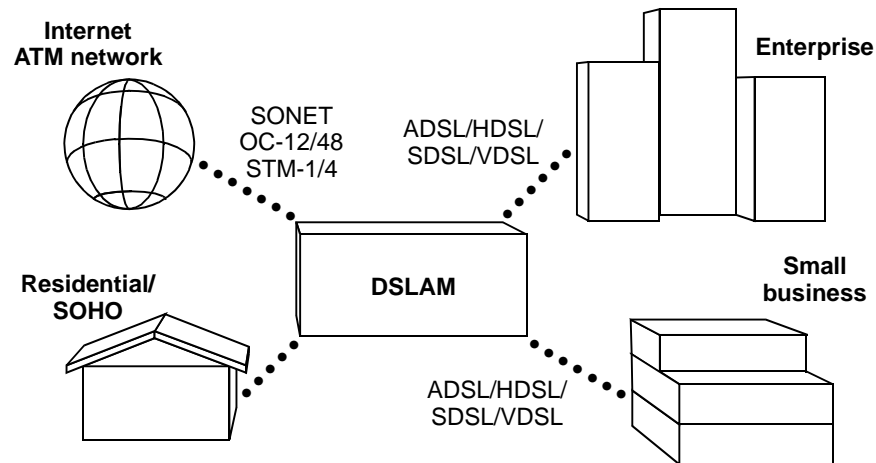


Figure 8. DSLAM Topology

The DSLAM is a network element defined to support high-bandwidth access to the public network. With the ability to support data and voice services over existing subscriber lines, the DSLAM can assist local phone service providers and ISPs in minimizing cost while maximizing the efficiency of their networks and enabling the provision of broadband services.

Traditionally, DSLAM elements have been fairly unsophisticated devices which act as ATM multiplexers that funnel ATM virtual channels (VCs) from subscribers into a common trunk interface. In this way, the DSLAM incorporates very little intelligence and has no upper layer protocol awareness. Network access equipment providers are concerned about provisioning efforts and VC depletion with this model where VC aggregation and subscriber termination occurs at a centralized location.

To address some of these concerns, DSLAM vendors and providers have begun migrating away from the traditional centralized approach, pursuing a more distributed architecture involving adding intelligence into the DSLAM, for example, adding support for IP. Many top tier vendors have added an adjunct card known as an IP service blade permitting IP routing and broadband remote access server (BRAS) features. The IP blade terminates the large number of customer VCs, and aggregates the traffic into a smaller subset of circuits. Provisioning time and cost is reduced in bringing up new users with the added IP functionality. Also, new options such as aggregation via L2TP tunnels or new services for VPN and video multi-casting can be explored. Overall, a distributed architecture bodes well with many service providers' future plans and attempts to push more services and content across the access network to the end user.

Motorola's PowerQUICC III can provide an efficient solution for the trunk card (also referred to as the uplink card) in the DSLAM implementation. Figure 9 illustrates an IP-based trunk card that connects to an ATM backplane. The PowerQUICC III communications processor enables access providers to leverage either ATM or native TCP/IP if they choose for their traffic transport through the inherent capabilities of its CPM. The PowerQUICC III provides functionality coupled with the higher performance that will be instrumental in newer DSLAM designs.

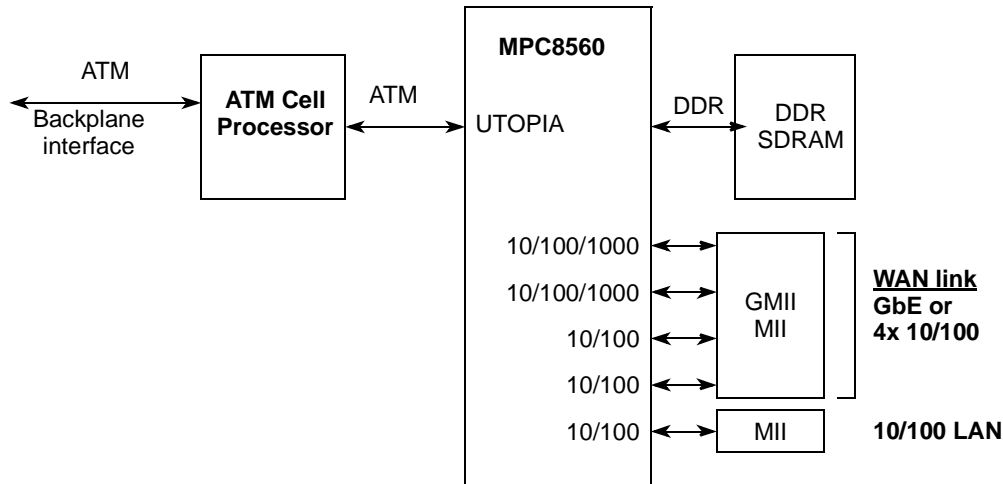


Figure 9. IP-Based Uplink (Trunk) Card

Motorola has an established base of PowerQUICC I (MPC8xx) and PowerQUICC II (MPC82xx) DSLAM design wins with top-tier equipment manufacturers and these product families have been extremely successful in addressing the CPU performance and low cost requirement needed on DSL line cards. The PowerQUICC III solution further extends this capability to add IP forwarding, multicast, and filtering as well as virtual channel (VC) aggregation and demultiplexing.

4.5 Media Gateway

Packet telephony (or IP telephony), a general term for the technologies that use the suite of internet protocols to exchange voice, fax and data (and other forms of multimedia information) using packet-switched networks, utilize a range of infrastructure systems including media gateways. Growing data networks as well as the opportunity and capability to utilize advances in compression techniques, are driving the adoption of packet telephony and the widespread focus on utilizing packet-switched networks. Media gateways and switches supporting the integration of VoIP, legacy public switched telephone network (PSTN), and ATM networks make this convergence possible.

A representation of a packet telephony system is shown in Figure 10. The media gateway bridges the packet-based network and the circuit-based network. The media gateway controller coordinates network routing activity and is the home of the communications processor.

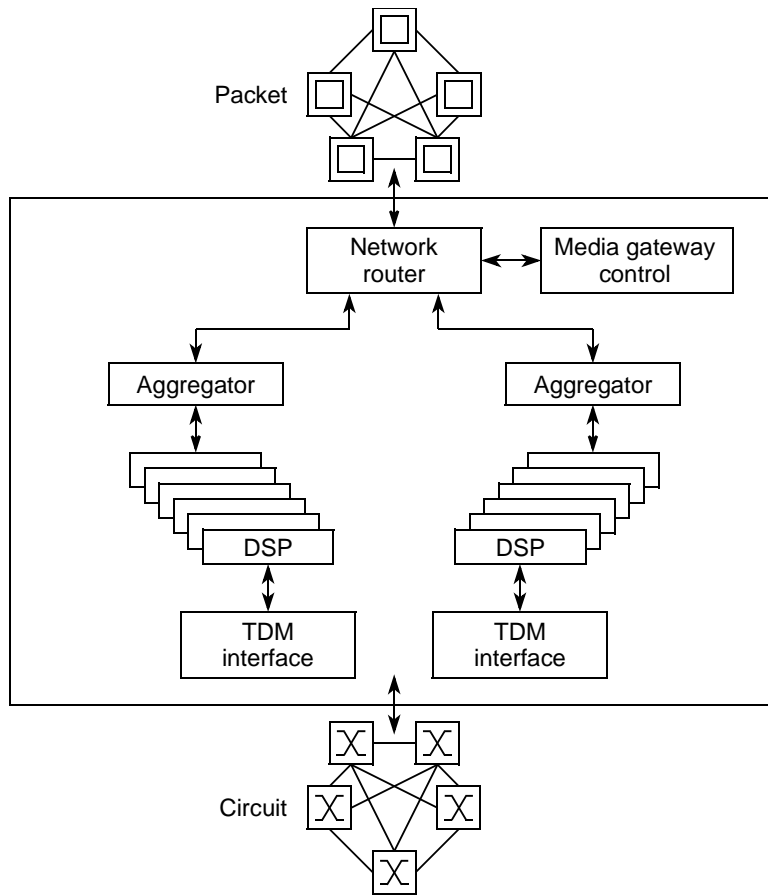


Figure 10. Packet Telephony Basic System Level Partitioning

The example shown in Figure 11 is a demonstration of the use of an MPC8540 inside a media gateway.

The PowerQUICC III in Figure 11 provides the intelligence of the media gateway unit as the media gateway control processor. The integrated communications processor is responsible for converting data between interfaces quickly. The PowerQUICC III is equipped with the processing power to complete packet conversion and it also provides up to 1 GHz CPU processing performance to complete such needed tasks as routing, firewalling, and security.

The PowerQUICC III additionally provides the much needed adaptability for different system configurations by having already incorporated interfaces needed to run concurrently such as its 64-bit 133 MHz PCI-X (or 66 MHz PCI) bus, local bus, RapidIO, and Ethernet interfaces. Extra CPU performance is provided due to the processor's ability to efficiently leverage on-chip resources, such as the direct memory access (DMA), interrupt handling, and certain I/O interfaces using integrated blocks such as the e500 coherency module, the programmable interrupt controller, and the non-blocking OCeAN switching fabric.

The MPC8540 offers an attractive solution for high-performance standardized interconnects and interfaces via its high speed gigabit Ethernet interfaces and RapidIO interconnect. The use of RapidIO simplifies routing and can be used to replace an otherwise custom DSP aggregation FPGA with a commodity switch, eliminating the need for any proprietary FPGA in the system. RapidIO further allows the PSTN information to be injected anywhere in the system, whether it be through the DSP processor or other packet oriented interfaces.

The PowerQUICC III full feature product, the MPC8560 can become an even more complete solution in a design where such functionality as the formatting of voice packets into appropriate network protocol can be handled by the CPM. As a controller in the media gateway unit, the PowerQUICC III provides flexibility and extendability widening the pathway for building enhanced media gateway solutions in the future.

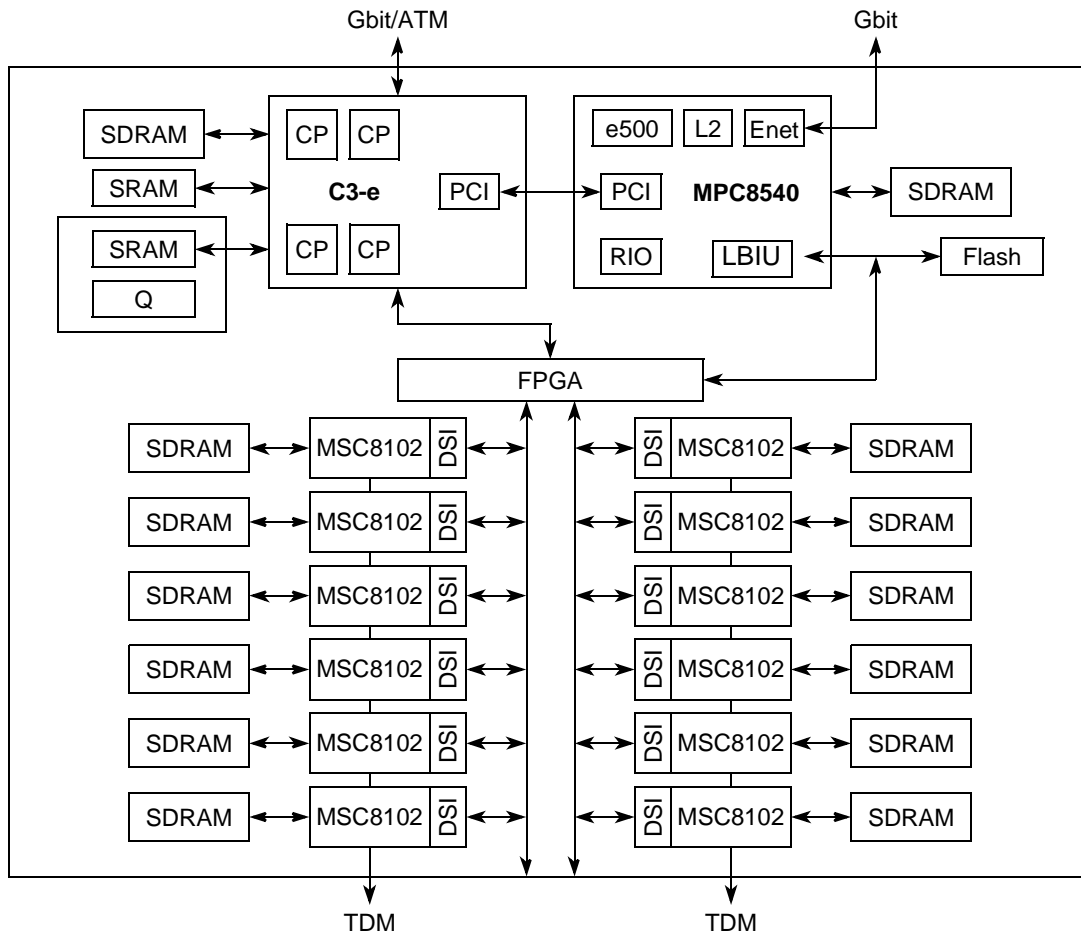


Figure 11. Generic Media Gateway Unit

5 Summary

Motorola's PowerQUICC III integrated communications processor delivers flexibility, standardization, high performance, and integration to address various processing needs including network control, enterprise storage channel processing, and high density distributed computing platforms. The PowerQUICC III provides a platform for a family of Motorola application-specific standard products for networking, communications, automotive, and consumer applications. Motorola, with its PowerQUICC III, has optimized this SoC platform for performance and flexibility focusing on performance, power, and price. A rich feature set has been enhanced by an extensive set of microcode packages that have been designed to enable new and current customers to integrate forwarding plane functionality into their existing and next generation networking equipment. The PowerQUICC III communications processor includes the necessary integration to optimize applications, yet still defines a flexible architecture for easy integration of value-added intellectual property.

Providing two distinct processors, the full feature MPC8560 and the Ethernet-capable MPC8540 without the CPM, the PowerQUICC III is appropriate for customized solutions in different applications.

Additionally, the same flexible architecture lends itself to future derivative products with further enhancements including process improvements, and extended hardware functionality, such as security to address key application requirements. The architecture provides solutions for today and is a stepping stone for tomorrow, with the ability to offer extensions to the current functionality as well as reduced functionality derivatives for cost-sensitive applications. With such a complete roadmap for the PowerQUICC III integrated communications processor, the PowerQUICC III is well placed to offer system architects a solution that simplifies their system architecture, shortens equipment development cycles, reduces time to market, and provides a platform for future upgrades to ensure a longer time in market.

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