White Paper

QorIQ Qonverge Portfolio

Next-Generation Wireless Network Bandwidth and Capacity Enabled by Heterogeneous and Distributed Networks

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Abstract

From the wireless operators' perspective, the key factors in building wireless networks are the ability to meet demand for high-bandwidth base stations in different form factors, end user capacities and quality of service, while significantly reducing network deployments and operating costs. The world has already moved from 3G toward 4G. The performance race toward supporting LTE and LTE-Advanced, at the highest data throughputs and highest user densities, is now underway. This paper briefly describes LTE technology, its challenges and Freescale's solutions for addressing these challenges.

Table of Contents

Preface

The increased use of smartphones and other mobile devices utilizing Internet applications, video, social networking and email traffic is driving an unprecedented increase in worldwide wireless network traffic. From a network operator's perspective, the key factors in driving wireless network topologies are their ability to meet demand for bandwidth, user capacities, users' quality of service (QoS) and reduce network costs.

As the world moved from 2G to 3G, and now to the 4G LTE and LTE-Advanced standards, demand for bandwidth capacity is increasing exponentially. Globally, mobile data traffic will increase 13-fold between 2012 and 2017. Mobile data traffic will grow at a CAGR of 66 percent between 2012 and 2017, reaching 11.2 exabytes per month by 2017. (Source: Cisco Visual Networking Index Global IP Traffic Forecast, 2012–2017.)

Achieving the required capacities, QoS and lower costs is contingent upon multiple factors such as proximity of the users relative to the base station or the RF transceivers, the number of users in a cell, data throughputs and patterns, core network capabilities, base station costs and operating costs.

Traditional macro sites are installed on rooftops or at designated cell sites that typically have the baseband units in a cabinet enclosure with the transceivers and RF power amplifiers while the antenna resides on a tower mast. The cabinet is then connected using a coaxial cable to the antenna on the antenna mast, which is the most common cell site approach for building mobile networks.

Moving to LTE and LTE-Advanced, this type of architecture is being transformed and enhanced with the introduction of remote radio heads (RRH) connected to a base station cabinet via fiber optic cables that can reach beyond 10 km or deployment of small cells—both methods bring the users "closer" to the base station. A distributed antenna system employs a macro or micro base station, the same as a traditional cellular site, but instead of the tall antenna mast, fiber optic cables are used to distribute the base stations' signals to a group of antennas placed remotely from the baseband processing in outdoor or indoor locations where required.

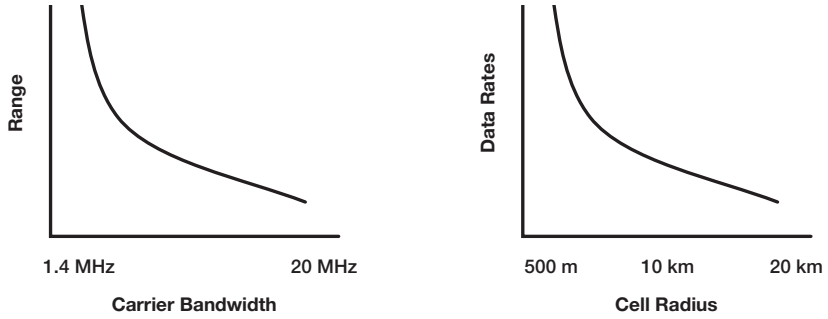
Subscribers are demanding faster data speeds, but due to limited coverage in dense urban areas and inside buildings, wireless networks built of only traditional macro base stations handling hundreds of users with high-power amplifiers no longer will be sufficient. Instead, new types of overlay network deployments will be required for 4G data services and the types of base stations at the forefront of these new deployments will be the small base stations called enterprise femtocells, picocells, metrocells and distributed antenna systems. These base stations typically handle up to two sectors and carrier aggregation that was lately introduced as part of LTE-Advanced covering a relatively small radius up to 5 km supporting fewer users and lower power amplifiers installed outdoors in metro areas such as building walls, lampposts, poles, rooftops, campuses, enterprises, bus and train stations, as well as indoor deployments covering a radius of up to 500 m. Having these base stations installed and operated by mobile operators will ensure the right equipment form factor for the right situation to meet the ever-growing need for greater capacity.

Wireless networks are evolving, but the transition to 4G technology won't happen in one day. Keeping the base stations as compact as possible, while having them on a single baseband card, results in the need to support 3G and 4G users simultaneously and a single baseband processor is key to enable that support.

Key to any base station design are the digital baseband processing elements that define its users' capacity, data throughputs, scalability and impact on equipment and operational costs. A high degree of integration and sophistication is key, especially for compact base station design, as it is lowering the cost and power consumption of the digital processing elements while maintaining the high throughputs and capacities.

This paper outlines Freescale's solutions that enable the creation of these new types of base stations.

Figure 1: Need for Small Cell and Distributed Antenna Deployments



Ranges, Data Rates, Antenna Configurations and Bandwidth in LTE

Carrier bandwidth has a significant impact on the effective range due to the distribution of energy from a limited source over multiple frequencies. A wider carrier bandwidth results in shorter range for a given data rate or in lower data rates for a given range.

The charts in figure 1 depict small cell deployments that can provide advantages by having many small self-contained boxes mounted at convenient locations closer to the users, maximizing the throughputs over a larger service area. As LTE deployments proceed it is expected that wireless networks in dense urban areas—where multi-path affects intensify, obstructions block the transmission or other interferences exist—will consist of large numbers of small cells and/or larger cells with distributed radio heads.

Another method to increase data rates and ranges is to use sophisticated multiple input, multiple output (MIMO) techniques requiring a higher number of antennas. However, the implementation of such configurations may result in higher overhead cost for indoor deployments where installation space and base station enclosure dimensions are confined.

System throughputs in areas with high concentration of user equipment can be maintained by installing small cells or by bringing the RF transceiver closer with lower power RF amplifiers than used in traditional macro base station configurations. This allows operators to support maximum throughput and capacity within a given area.

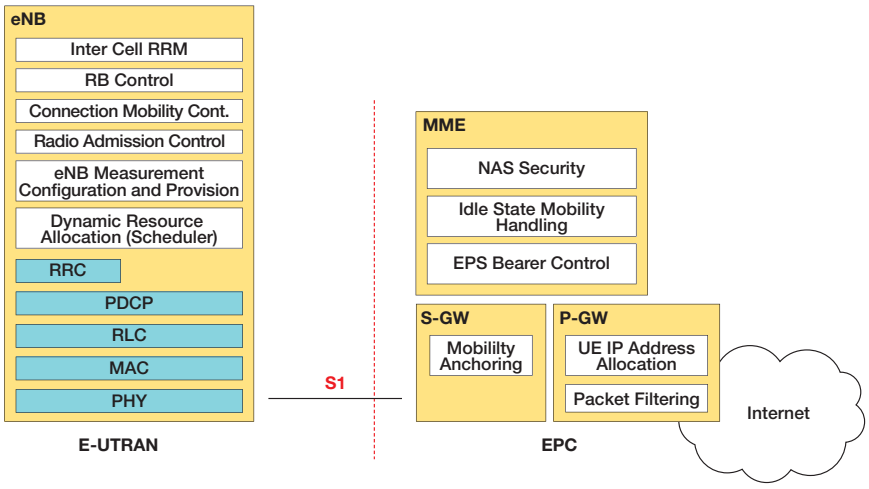
Digital Baseband Processing Elements in LTE eNodeB (eNB) Base Station

Digital baseband processing in LTE base station (eNB) is divided into several layers. Typically, the processing elements include a general-purpose multicore processor (GPP) device or core to process the MAC-Scheduler, RLC, RRC, PDCP and Transport layers, multicore digital signal processor (DSP) device or core with L1 baseband accelerators to process the physical layer (PHY) and digital radio front-end logic typically in an ASIC, FPGA or off-the-shelf transceiver to prepare the signal to be sent to the RF amplifier.

Figure 2 describes the different layers of LTE processing in LTE eNB base station.

In typical macro and micro base stations, the baseband channel card is composed of a single GPP device and multiple DSP devices due to the need for handling a scalable and variable number of sectors, number of users and throughputs based on the specific deployment requirements. Alternately, picocell and metrocell base stations typically handle a single sector and a given number of users and data throughputs. The traditional single GPP device and single DSP discrete device paradigm is now changing to a single unified system-on-chip (SoC) solution.

Figure 2: Digital Baseband Processing Elements in LTE eNodeB (eNB) Base Station



Source: *3GPP TS 36.300 V8.12.0*

L2 and L3 Layers

Figures 3 and 4 depict the different functions in building L2 and L3 layers in an LTE base station. These typically are implemented by the GPP. The three sub-layers are medium access control (MAC), radio link control (RLC) and packet data convergence protocol (PDCP).

PHY (L1) Physical Layer

Figures 3 and 4 depict the chain of functions building the PHY (L1) layer in an LTE base station, typically implemented by the DSP cores and baseband accelerators.

Figure 3: Downlink and Uplink Chains in LTE Base Stations

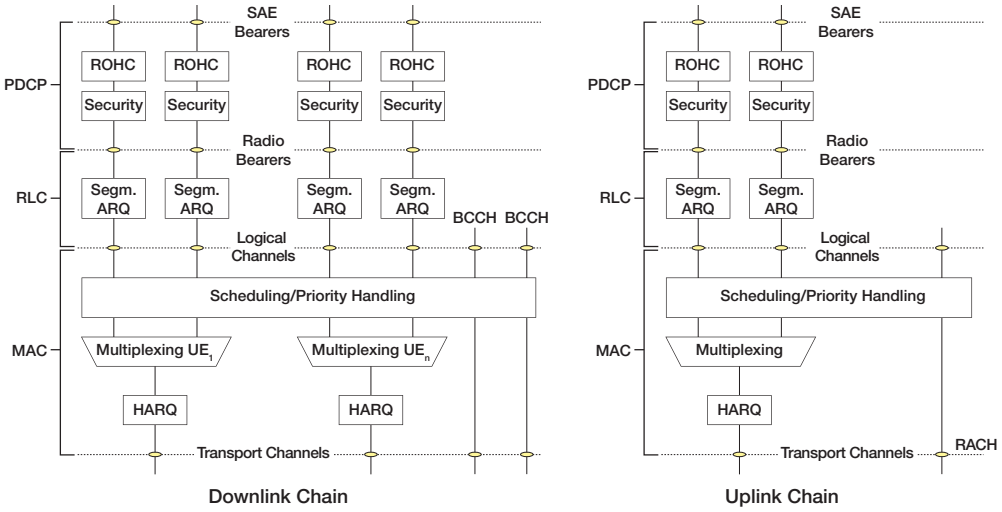
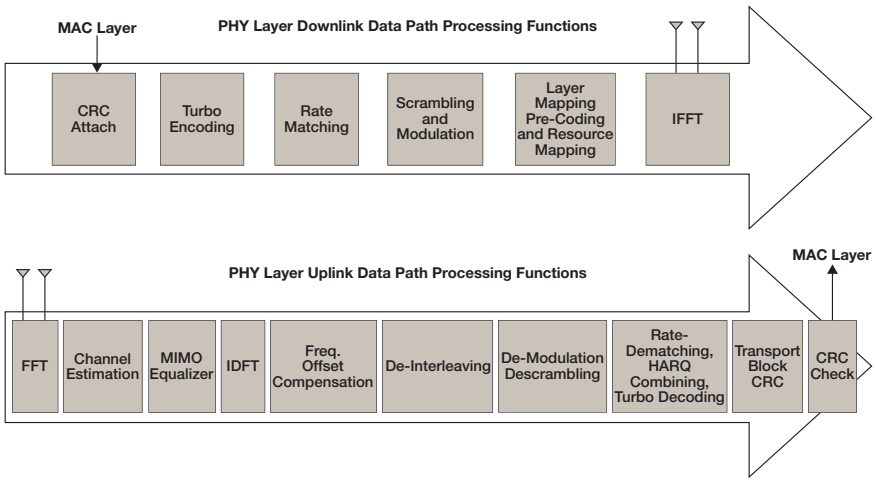


Figure 4: PHY (L1) Physical Layer



Challenges in Evolving Networks

As wireless networks evolve, support for LTE and WCDMA standards and multimode operation with both technologies running simultaneously are becoming requisite. Given the inherent differences between these wireless standards, a number of technical challenges have to be solved on various levels of the processing stacks.

On the L1 physical layer, the 3GPP standards for third-generation WCDMA and next-generation LTE have taken different approaches to modulate and map the data onto the physical medium. As the name indicates, WCDMA is based on code division multiple access and typically requires processing resources to efficiently perform spreading/despreading, scrambling/descrambling and combining operations. These are the main functions needed in the RAKE receiver approach typically used in WCDMA. The L1 operations in WCDMA are a mix of streaming and batch type operations, which the baseband architecture must process efficiently.

In contrast, LTE uses a mix of OFDMA for downlink and SC-FDMA modulation for uplink. This multicarrier approach follows the principle of modulation for orthogonal subcarriers to maximize the spectrum density. The predominant operations in OFDMA/SC-FDMA are the discrete fourier transforms in the form of FFT or DFT and forward error correction (FEC) and MIMO techniques.

The nature of data organization and subframe structure in LTE allows the L1 processing steps to be scheduled sequentially according to the available subframe user and allocation information. The key challenge is meeting the tight latency budgets of the physical layer processing to maximize the available time budget in the MAC layer scheduler.

Baseband Acceleration and Addressing the Multimode Challenges

With Freescale devices, the PHY is implemented using a mix of StarCore high-performance DSP cores and the multi acceleration platform engine (MAPLE) for baseband. MAPLE accelerators provide highly efficient hardware implementation of the standardized building blocks for each of the air interface standards in single mode and in multimode operations, handling:

- Fourier transform processing: Used primarily in LTE for FFT and DFT fourier transform operations as well as RACH operations. It also can be used in WCDMA for frequency domain search and RACH operations. The ability to perform additional vector post and pre-multiplier operations makes this unit also very suitable for correlation and filtering operations.
- Turbo/Viterbi decoding processing: Used for forward error correction (FEC) deploying Turbo and Viterbi decoding algorithms in LTE/LTE-A and WCDMA standards. Other functions such as CRC calculation, rate de-matching operations and HARQ combining are also covered.
- Downlink encoding processing: Used for FEC deploying turbo encoding algorithms in LTE/LTE-A and WCDMA standards and rate matching operations.
- Chip rate processing: Used to accelerate downlink (DL) and uplink (UP) spreading/despreading and scrambling/descrambling operations for both data and control channels. This block is used exclusively for WCDMA and CDMA2K/EV-DO standards.

- Equalization processing: Performs the MIMO equalization operations based on minimum mean square error (MMSE), interference rejection combining (IRC), successive interference cancellation (SIC) or maximum likelihood (ML) approaches, while its internal algorithms and outputs are performed and generated in floating-point mathematics. A number of configurable operation modes allow the adaptation of the equalization process to the user characteristics and channel conditions. These equalization algorithms are quite complex and require many computation resources. Hence, Freescale has selected to implement the algorithms in hardware acceleration, which is adaptable to different nuances and at the same time frees them from the DSP cores, leaving these for other tasks in the processing chain.
- Physical downlink data path: Performs an encoding of the physical downlink shared channel (PDSCH) starting from the user information bits up to the cyclic prefix (CP) insertion and antenna interface handshake. Including DL-MIMO precoding and layer mapping operation.
- Physical uplink data path: Performs decoding of physical uplink shared channel (PUSCH), resulting in decoded information bits.

As mentioned previously, there is a need to support multiple standards concurrently as users migrate to LTE. It is especially important that small cells that cover a given, and relatively limited, cell radius and number of users continue to support multimode while providing an upgrade path for handling more advanced technologies.

In order to handle multimode operation, the DSP cores are fully programmable and can implement any standard. The MAPLE hardware block was designed in such a way to enable multimode operation such as Turbo and Viterbi decoding, Turbo encoding/decoding and FFT/DFT can operate concurrently on both standards in terms of the algorithms' processing and capacity.

The layer 2 and layer 3 algorithms use a mix of Power Architecture® general-purpose high-performance cores together with transport and security acceleration. Most of this processing is done on programmable cores where any standard, including multimode operation, can be implemented efficiently. The commonality between WCDMA and LTE standards is the requirement for secure backhaul processing. The bulk of this is Ethernet, QoS, IPsec and WCDMA frame protocol processing, which is offloaded to hardware acceleration and leaves software flexibility for the L2 stacks of both standards.

In terms of capacities, Freescale dimensioned its devices' multiple cores and accelerators in such a way as to enable operation on both standards simultaneously.

Freescale devices support multimode operation for different base station sizes from femtocell to macrocell.

Meeting the Latency Budget

To ensure continued competitiveness to 3G technology, the 3GPP standard body-based LTE technology on orthogonal frequency division multiplexing (OFDM) and MIMO antenna techniques. The major performance goals addressed are significantly increasing data rates, reducing latencies and improving spectrum efficiencies.

Latency is a key network metric and has a major influence on users' experience both in voice calls and data transactions such as video and Internet applications. The key challenge is meeting the tight latency budgets of the physical layer processing to maximize the available time budget for the rest of the PHY processing and MAC layer scheduler tasks. The LTE standard defines the end-user roundtrip latency as less than 5 ms, which requires the latency within the base station to be significantly lower (less than 0.5 ms in downlink and less than 1 ms in uplink).

MIMO equalization/detection and FEC are heavily used in newer, high bit rate wireless communication standards such as LTE and WiMAX. The MIMO equalizer and turbo coding error correction algorithms both in uplink and downlink are the major influencers on base station throughput and latency. Freescale has developed a set of hardware accelerators that meet the low latencies by designing them for three to five times higher throughputs than the defined throughput. This is expected to result in completing these tasks ahead of time and leave more room for the other algorithms in the processing chain.

About Intellectual Property Ownership

Unlike some competitors, Freescale's ownership of key intellectual properties (IP), coupled with deep engagement with leading OEMs in the wireless access market already proved itself by being first to introduce solutions for LTE base stations, making Freescale a leader in this market. This puts Freescale in a position to define next-generation architectures to drive further integration that provides performance, power and cost benefits. Being relatively independent from external IP providers' next-generation technologies and timelines enables Freescale to drive a roadmap of devices that helps meet OEM targets for performance and timelines for next-generation wireless technologies.

The key processing elements in any device for mobile wireless infrastructures are the programmable cores, hardware accelerators, internal interconnects and high-speed interfaces. Freescale has long been an embedded processing leader. The market-proven Power Architecture core is at the heart of Freescale's strength and has been used by leading wireless OEMs worldwide for many years. While significantly enhanced from generation to generation, it comes with a very rich ecosystem to provide customers with a seamless migration from their current products to higher performance products. The StarCore DSP core has been enhanced by Freescale from generation to generation for more than a decade and is known for its high performance and programmability. The StarCore SC3850 and SC3900 DSP cores are used today in discrete DSP and SoC devices deployed by many of the wireless manufacturers in LTE, WCDMA and TD-SCDMA deployments and has earned leading results from top benchmarking firms.

Other important components are the internal fabric and accelerator throughputs and standard compliance. The internal fabric is a component that connects all processing elements and memories within the device; it must enable high throughputs and low latencies for data movement throughout the SoC as well as not stalling any of the elements attached to it for processing its data. Both the internal fabric and the accelerators were proven to be highly efficient and were field deployed by Freescale customers.

Device Architectures and Capacities

Freescale has developed powerful and innovative multicore processors, DSPs and SoC devices. Some of these devices are in full production today and deployed in the field utilizing some of the industry's most advanced silicon technology. These devices that are already being used in commercial and trial networks were designed to allow base station manufacturers to develop new technologies like LTE while increasing performance and reducing costs for existing wireless technology such as WCDMA.

The 3GPP standard body defined several levels of data rates for FDD 20 MHz carrier bandwidth depicted in table 1.

Freescale has created a family of products that scales with LTE throughputs per sector ranging from 100 to 300 Mb/s in the downlink and from 50 to 150 Mb/s in the uplink.

By leveraging the high-performance programmable architectures, Freescale can offer a family of software-compatible devices that scale from femtocells to macrocells. The following sections describe Freescale solutions addressing the different types of base stations designs.

Table 1: Data Rates for 20 MHz Carrier Bandwidth

Category		1	2	3	4	5
Peak Rate Mb/s	DL	10	50	100	150	300
	UL	5	25	50	50	75

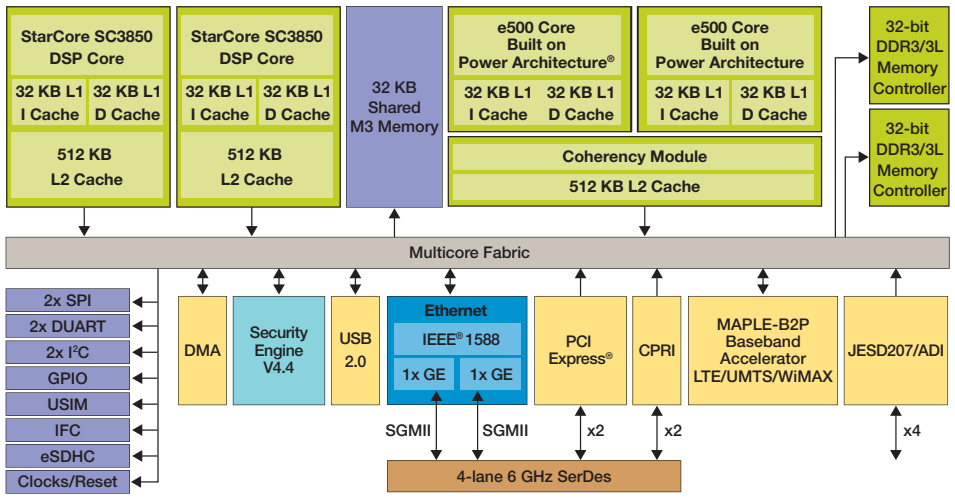
QorIQ Qonverge BSC9132 SoC for Enterprise Femtocell/Picocell Solutions

- Standards: FDD/TDD LTE (Rel. 8/9) and WCDMA (Rel. 99/6/7/8/9)
- LTE bandwidth: 20 MHz single sector or two sectors at 10 MHz
- WCDMA-HSPA+ bandwidth: 2x 5 MHz
- LTE throughputs: 150 Mb/s DL/75 Mb/s UL with 2 x 4 antenna MIMO
- HSPA+ throughputs: Dual cell—84 Mb/s DL/23 Mb/s UL
- Active users in single mode
  - LTE—100 users
  - AMR/HSPA+—64 users respectively
- Active users in dual mode
  - 32 LTE users and 32 HSPA users simultaneously

QorIQ Qonverge BSC9132 Device Features

- Dual Power Architecture e500 cores at up to 1.2 GHz
- Dual StarCore SC3850 DSPs at up to 1.2 GHz
- MAPLE-B2P baseband accelerator platform
- Security acceleration engine handling IPsec, Kasumi, Snow-3G
- DMA engine
- Dual DDR3/3L, 32-bit wide, 1.333 GHz, with ECC
- IEEE® 1588 v2 and interface to GPS sync support
- 2G/3G/4G sniffing support
- Secured boot support
- Interfaces
  - Four SerDes lanes combining 2x Ethernet 1G SGMII, 2x CPRI v4.1 @ 6.144G antenna interface, 2x PCIe at 5 Gb/s
  - Quad JESD207/ADI RF transceiver interfaces, USB 2.0, NAND/NOR flash controller, eSDHC, USIM, UART, I²C, eSPI

Figure 5: QorIQ Qonverge BSC9132 Processor

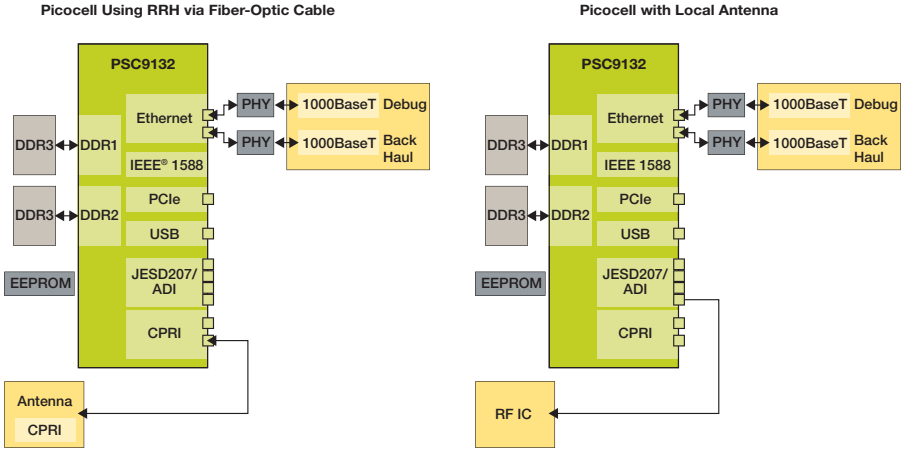


Different Antenna Configurations

Combining the digital baseband devices together with the transceivers and the power amplifiers in the same enclosure forms a compact base station that can be mounted almost anywhere outdoors and inside buildings by connecting the JESD207 standard antenna interfaces to the local transceivers covering a few hundred meters of cell radius. If increased cell coverage is required, a remote antenna can be mounted on the top of the mast, or in a remote location, and connected to the baseband unit through the CPRI optical interface. Figure 6 depicts the different options.

The combination of the four JESD207 interfaces or the two CPRI interfaces enables the BSC9132 SoC to support dual mode WCDMA and LTE standards with different antenna configurations, for example 2 x 2 for WCDMA 5 MHz and 2 x 4 for LTE 20 MHz simultaneously.

Figure 6: Antenna Configurations



QorIQ Qonverge BSC9131 SMB/Home Femtocell Solution

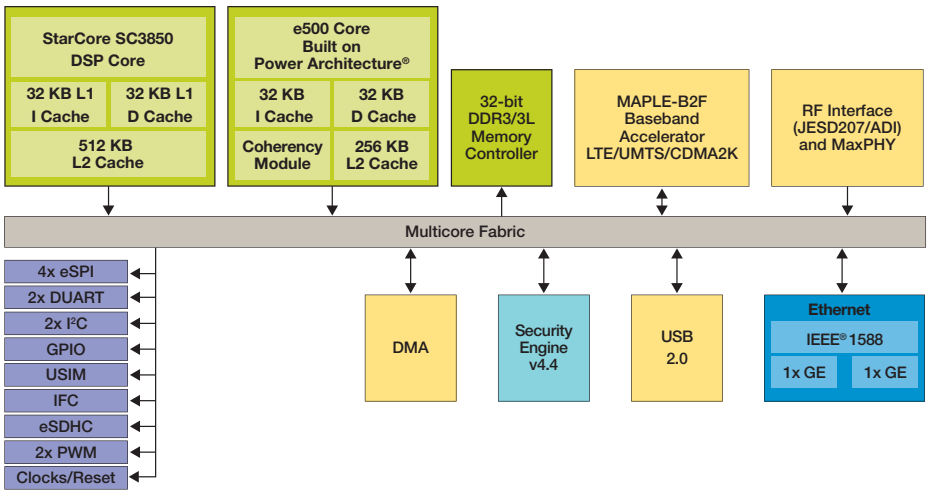
The QorIQ Qonverge BSC9131 SoC device is targeted at small-to-medium business (SMB)/ home base station deployments. The solution standards and capacities include:

- Standards: FDD/TDD LTE (Rel. 8/9), WCDMA (Rel. 99/6/7/8) and CDMA2K/EV-DO
- LTE bandwidth: 20 MHz single sector
- WCDMA/HSPA+ bandwidth: 5 MHz
- LTE throughputs: 100 Mb/s DL/50 Mb/s UL with 2 x 2 antenna MIMO
- HSPA throughputs: Single cell—42 Mb/s DL/11 Mb/s UL
- Active users in single mode
  - LTE—16 users
  - HSPA—16 users
- Active users in dual mode
  - Eight LTE users and eight HSPA users simultaneously

QorIQ Qonverge BSC9131 Device Features

- Power Architecture e500 core at up to 1 GHz
- StarCore SC3850 DSP at up to 1 GHz
- MAPLE-B2F baseband accelerator platform
- DMA engine
  - Security acceleration engine handling IPsec, Kasumi, Snow-3G
  - DDR3/3L, 32-bit wide, 800 MHz, with ECC
  - IEEE 1588 v2, NTP and interface to GPS sync support
  - 2G/3G/4G sniffing support
  - Secured boot support
  - Interfaces: 2x Ethernet 1G RGMII, 3x JESD207/ADI RF transceiver interfaces, USB 2.0, NAND/NOR flash controller, UART, eSDHC, USIM, I^2C, eSPI

Figure 7: QorIQ Qonverge BSC9131 Processors

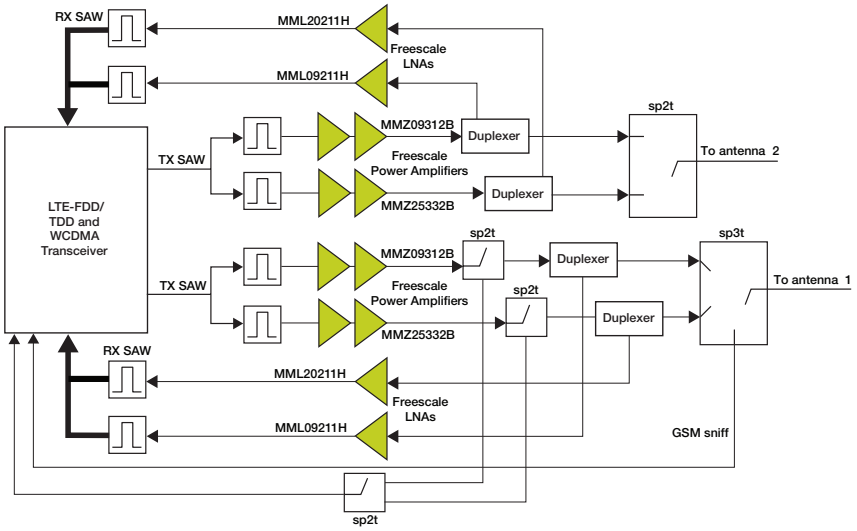


Airfast-Optimized RF Solutions for Small Cells

The AFT26HW050GS is designed specifically for wide instantaneous bandwidth microcell/metrocell LTE applications between 2500 and 2700 MHz.

- 2620–2690 MHz performance in Doherty Test Fixture
  - Peak power: 50 Watts
- At 8 Watts avg. output power:
  - Gain: 15.5 dB
  - Drain efficiency: 48 percent
  - DPD correction to –54 dBc using 20 MHz LTE signal

Figure 8: RF Module Block Diagram

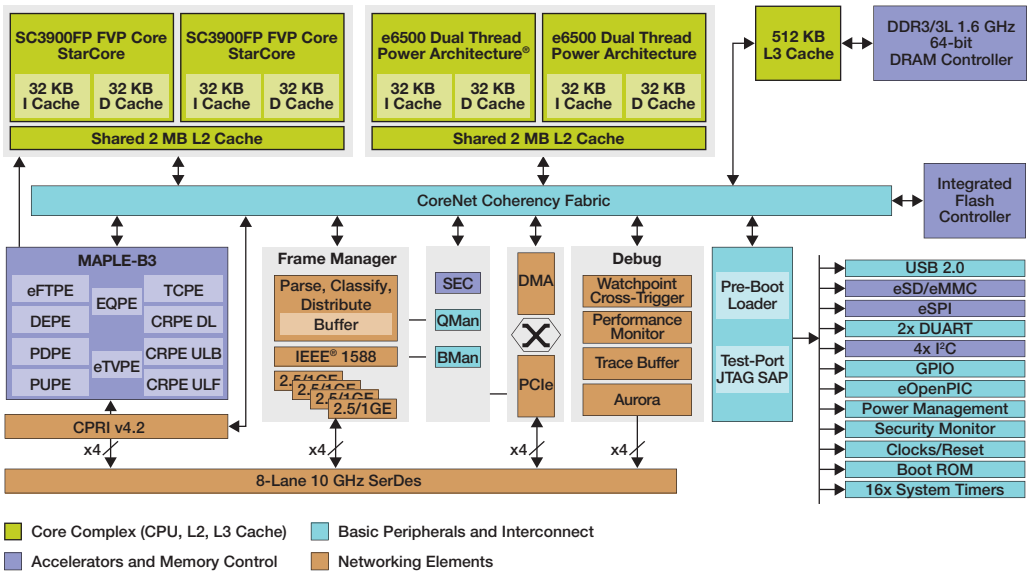


Metrocell Solution: QorIQ Qonverge B4420 Baseband Processor

QorIQ Qonverge B4420 multicore SoC architecture is designed for high-performance wireless infrastructure applications. It provides ultra high performance for carrier-grade metrocell and microcell base station platforms supporting various wireless standards including WCDMA (HSPA/HSPA+), FDD-LTE, TDD-LTE and LTE-Advanced standards.

This multicore SoC includes four programmable cores, two dual-thread 64-bit Power Architecture cores and two cores based on a StarCore flexible vector processor (FVP) and high-throughput, low-latency hardware accelerators for layer 1, layer 2 and transport to enable highly optimized processing for the radio processing chain from PHY to transport layers.

Figure 9: QorIQ Qonverge B4420 Block Diagram



Macrocell Solution: QorIQ Qonverge B4860 Baseband Processor

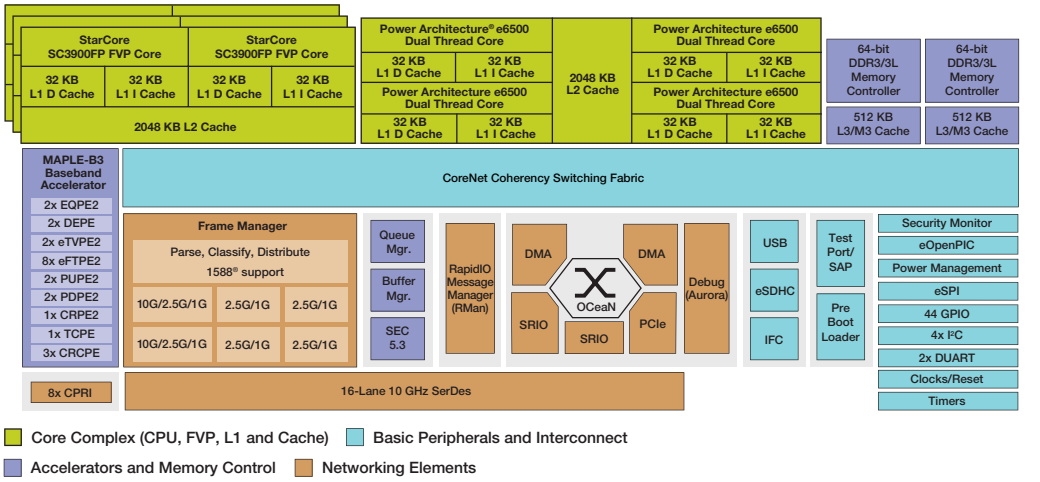
The QorIQ Qonverge B4860 device is a multistandard wireless base station SoC based on 28 nm process technology, enabling the processing of three 20 MHz sectors of LTE.

The B4860 device reduces overall power consumption for high-end wireless macro base stations to deliver the industry's highest performance solution. The multicore SoC includes 10 programmable cores based on StarCore FVP and 64-bit Power Architecture cores, as well as CoreNet and MAPLE technologies. The B4860 SoC targets broadband wireless infrastructure and builds upon Freescale's proven success of existing multicore SoCs, processors and DSPs in wireless infrastructure markets.

The B4860 processor is designed to adapt to the rapidly changing and expanding standards of LTE (FDD and TDD), LTE-Advanced and WCDMA, as well as provide simultaneous support for multiple standards.

Layer 1 is implemented using a mix of StarCore SC3900FP fix and floating-point high-performance FVP cores and the MAPLE baseband accelerator platform, which provides a highly efficient hardware implementation of standardized algorithms for each of the air interface standards in single and multimode operations. Layer 2 and transport processing are implemented using a mix of e6500 64-bit dual thread Power Architecture cores, data path and security accelerators.

Figure 10: QorIQ Qonverge B4860 Block Diagram



Macrocell Solution: QorIQ P4080 Processor and 3x MSC8157 DSP

The QorIQ P4080 processor, built on Power Architecture technology, and 3x MSC8157 DSPs are discrete solutions targeted at macrocell base station deployments. Supporting standards and capacities include:

- Standards: FDD/TDD LTE (Rel. 8/9) and WCDMA (Rel. 99/6/7/8/9)
- LTE bandwidth: 20 MHz up to three sectors

- LTE-Advanced bandwidth: 60 MHz single sector
- WCDMA-HSPA+ bandwidth: Up to six cells of 5 MHz
- LTE aggregated throughputs: 900 Mb/s DL/450 Mb/s UL with 4 x 4 MIMO
- Active users
  - LTE—900 users
  - HSPA+/AMR—384/900 active users respectively

The above macro base station channel card architecture is capable of delivering the highest throughputs allowed by the LTE standard for 20 MHz and enable connecting to RRH via fiber optic cables using the common radio public interface (CPRI) protocol that can spread over 10 km or more.

QorIQ P4080 Processor

Device features

- Eight high-performance e500mc Power Architecture cores up to 1.5 GHz
- Three level cache-hierarchy: 32 KB I/D L1, 128 KB private L2 per core, 2 MB shared L3
- Dual 64-bit (with ECC) DDR2/3 memory controllers up to 1.333 GHz data rate
- Data Path Acceleration Architecture (DPAA), incorporating acceleration for packet parsing, classification and distribution
- Queue management for scheduling, packet sequencing and congestion management
- Hardware buffer management for buffer allocation and de-allocation
- Security engine
- Pattern matching
- Ethernet interfaces:
  - Two 10 Gb/s Ethernet (XAUI) controllers
  - Eight 1 Gb/s Ethernet (SGMII) controllers
- IEEE 1588 v2
- High-speed peripheral interfaces:
  - Three PCI Express® v2.0 controllers/ports running at up to 5 GHz
  - Dual Serial RapidIO® 4x/2x/1x ports running at up to 3.125 GHz
- Hardware hypervisor for safe partitioning of operating systems between cores
- Secured boot capability
- SD/MMC, 2x DUART, 4x I^2C, 2x USB 2.0 with integrated PHY
- Other peripheral interfaces: Two USB controllers with ULPI interface to external PHY, enhanced local bus controller, SD/MMC, SPI controller, four I^2C controllers, two dual UARTs, two 4-channel DMA engines

Figure 11: eNodeB Channel Card

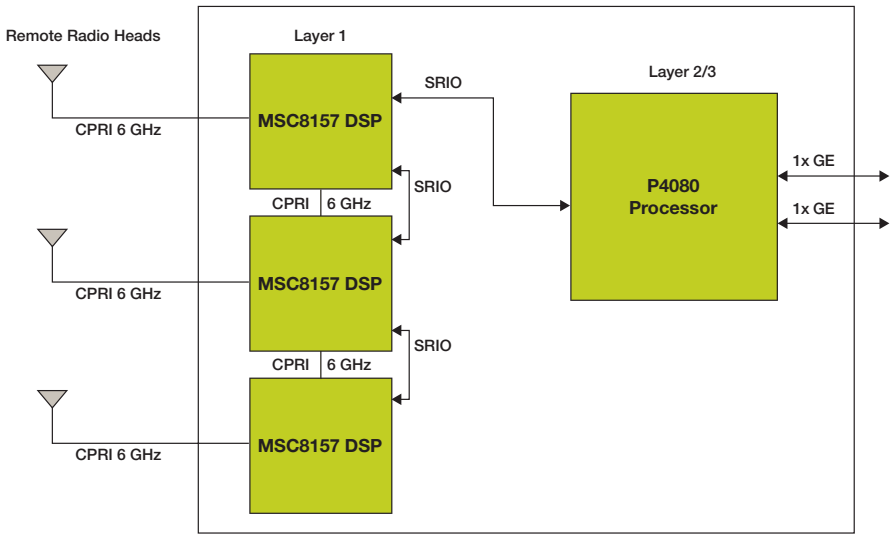
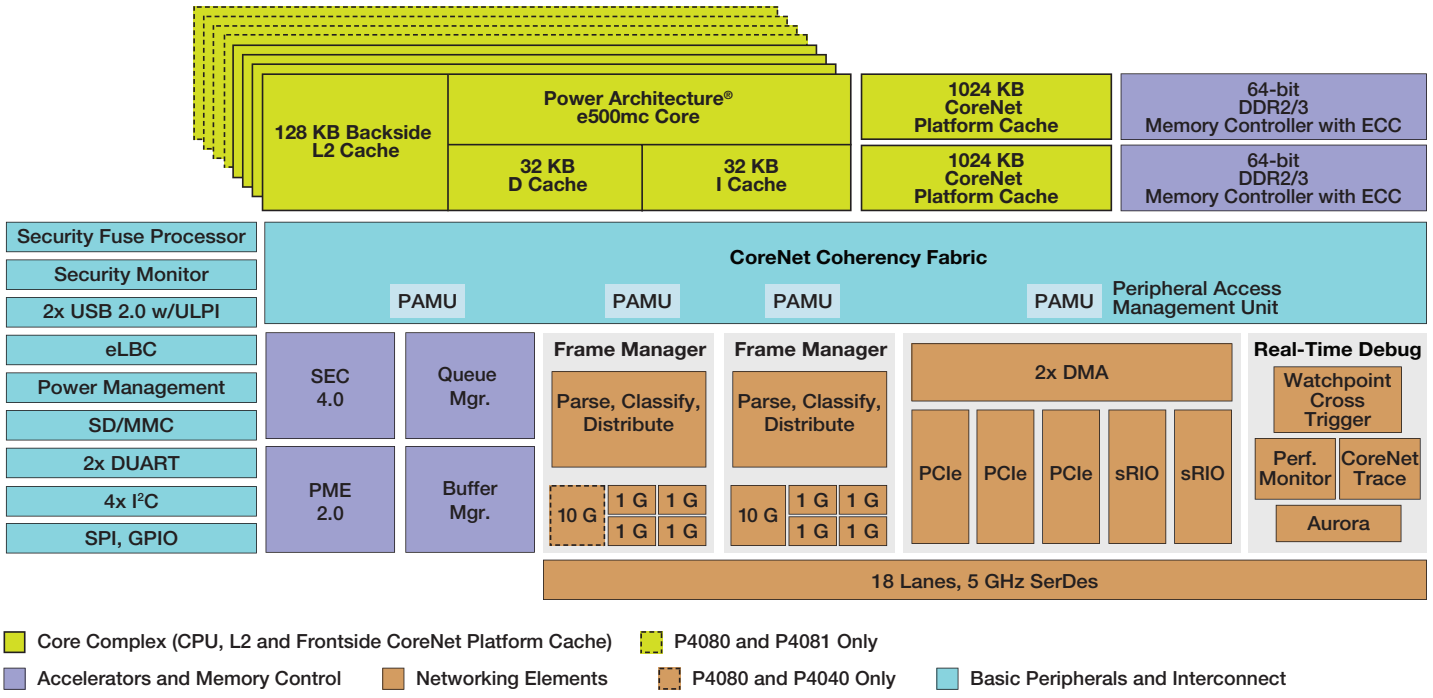


Figure 12: QorIQ P4080/P4040/P4081 Communications Processor Block Diagram



MSC8157 DSP

Device features

- 6x SC3850 DSP cores subsystems each with:
  - SC3850 StarCore DSP core at up to 1.2 GHz
  - 512 KB unified L2 cache/M2 memory
  - 32 KB I-cache, 32 KB D-cache, write-back-buffer (WBB), write through buffer (WTB), memory management unit (MMU), programmable interrupt controller (PIC)
- Internal/external memories/caches
- 3 MB M3 shared memory (SRAM)
- DDR3 64-bit SDRAM interface at up to 1.333 GHz, with ECC
- Total 6 MB internal memory
- CLASS—chip-level arbitration and switching fabric
- Non-blocking, fully pipelined and low latency
- MAPLE-B baseband acceleration platform
- Turbo/Viterbi decoder supporting LTE, LTE-Advanced, 802.16e and m, WCDMA chip rate and TD-SCDMA standards
- FFT/DFT accelerator
- Downlink accelerator for turbo encoding and rate matching
- MIMO acceleration support for MMSE, SIC, ML schemes and matrix inversions
- Chip rate despreading/spreading and descrambling/scrambling
- CRC insertion and check
- 10 SerDes lanes, high-speed interconnects
- Two 4x/2x/1x Serial RapidIO® v2.0 at up to 5G, daisy-chain capable
- Six-lane CPRI v4.1 up to 6.144G, daisy-chain capable
- PCI-e v2.0 4x/2x/1x at 5 GB
- Two SGMII/RGMII Gigabit Ethernet ports
- DMA engine: 32 channels
- Other peripheral interfaces: SPI, UART, I^2C, GPIOs, JTAG 1149.6

Figure 13: MSC8157 DSP

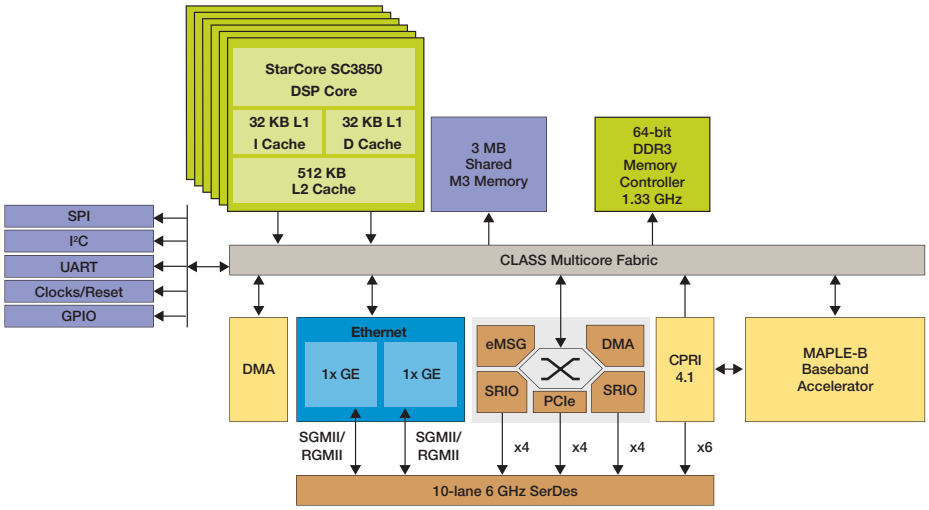


Figure 14: MSC8157 DSP–PHY Downlink Uplink Chain

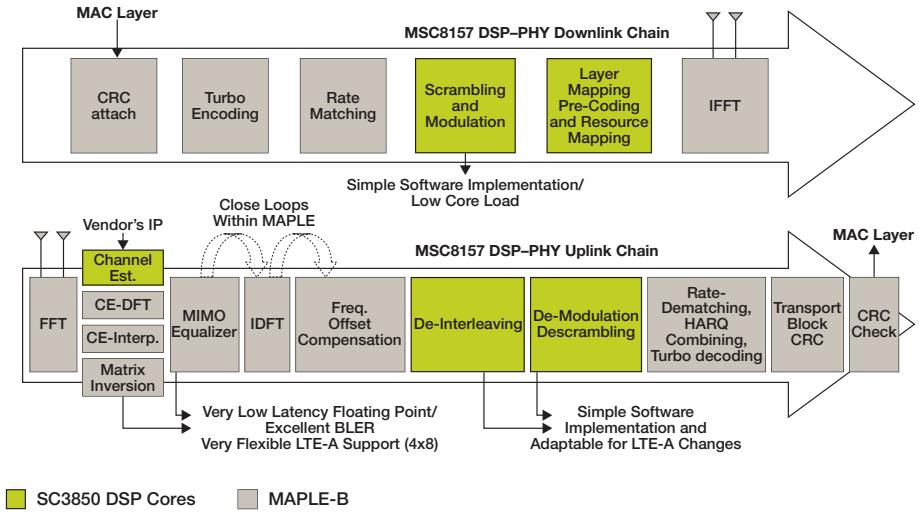
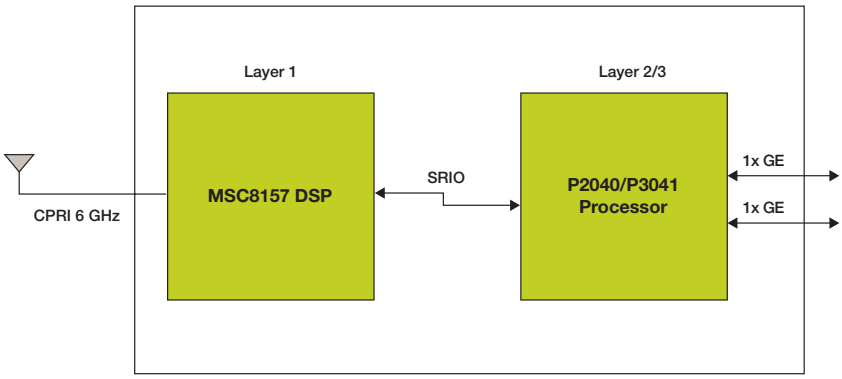


Figure 15: Microcell Channel Card



Microcell Solution: QorIQ P3041 or QorIQ P2040 Processor and MSC8157 DSP

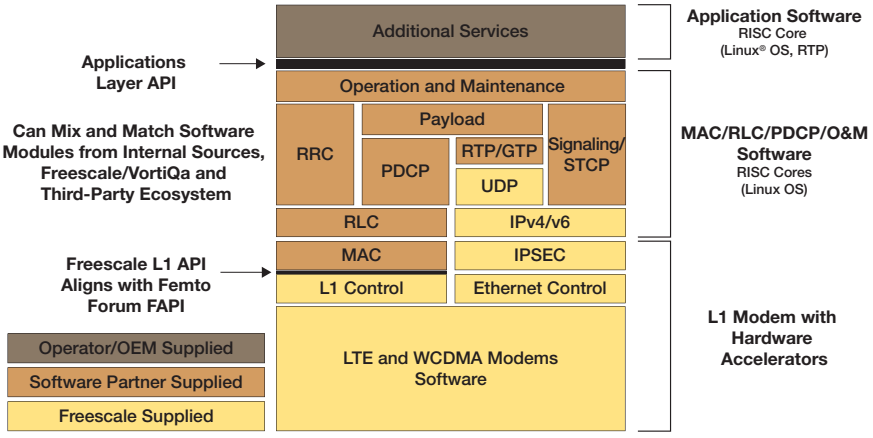
Built based on the QorIQ P3041 or P2040 processor and the MSC8157 DSP, targeted at microcell base station deployments. Supported standards and capacities include:

- Standards: FDD/TDD LTE (Rel. 8/9/10) and WCDMA (Rel. 99/6/7/8/9)
- LTE bandwidth: 20 MHz up to two sectors
- LTE-Advanced bandwidth: 20 MHz single sector
- WCDMA-HSPA+ bandwidth: Up to three cells of 5 MHz
- LTE throughputs: 300 Mb/s DL/150 Mb/s UL with 4Tx and 4Rx antenna MIMO
- Active users
  - LTE—300 users
  - HSPA+/AMR—128/300 active users respectively

VortiQa Layer 1 Software Migration

Many leading OEMs are deploying the QorIQ family and the MSC8156/7 DSP devices in their macro base station designs. The family of devices for small cells brings an unprecedented high level of software reuse from the macrocells by reusing the same basic elements. The DSP and processor cores are software backward compatible and MAPLE processing elements keeps the same API calls moving from macro and micro devices to small cell SoCs and vice versa. This kind of reuse means much faster development time from the OEMs, resulting in lower engineering costs and faster time to market.

Figure 16: VortiQa Layer 1 Software Offering and Mapping for BSC913X



VortiQa Layer 1 Software Offering and Mapping for QorIQ Qonverge BSC913x

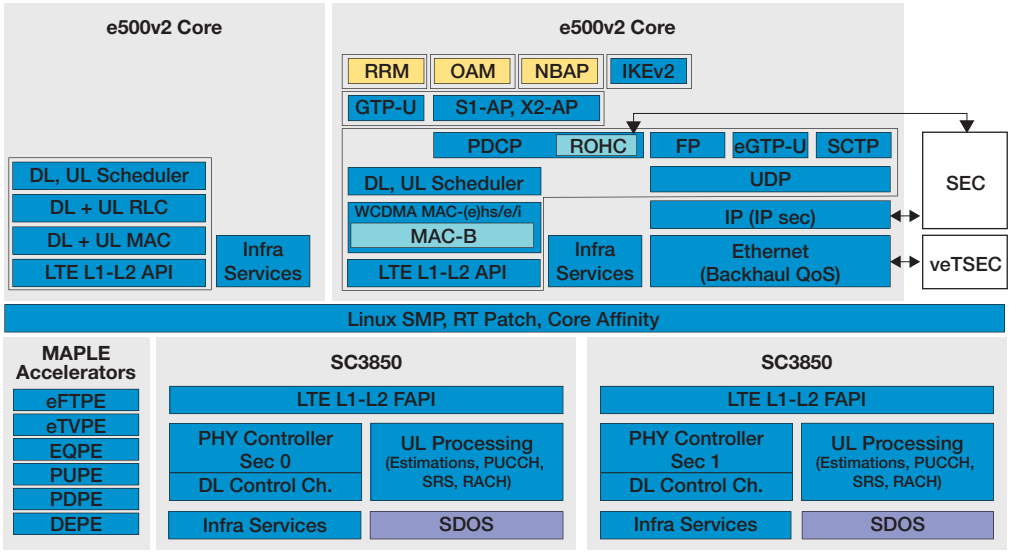
Freescale provides not only the silicon but also a comprehensive software solution for small cells and the ability to run it in simultaneous dual mode. Figure 17 depicts the software engagement model where Freescale delivers L1 modem software for LTE, WCDMA and dual mode while its partners deliver L2 and L3 software protocol stacks.

VortiQa Layer 1 Software Mapping on QorIQ Qonverge BSC9132

Figure 17 provides an example on the functional mapping of the LTE software components on the QorIQ Qonverge BSC9132 device.

The physical layer (L1) processing is handled entirely by the StarCore core subsystems with the support of the MAPLE-B accelerator. This functional split allows the encapsulation and control of the modem part under the femto API (FAPI) as proposed by the Femto Forum. This API provides the guidelines for the logical interface between the L1 and L2 that the industry has widely adopted.

Figure 17: Software Mapping on QorIQ Qonverge BSC9132



Summary

Major changes are happening in the radio access network including multimode and multi-standard base stations, and small/compact base stations such as femtocells, picocells, metrocells, microcells and macrocells with more flexible and distributed antenna systems for 3G and 4G. The standards evolution and all the above create new commercial and technical challenges for OEMs and wireless operators. Shorter time to market and a broader, more complex range of development creates an urgent need for scalability and reuse in both hardware and software. With the wealth of products that meet different base station capacities, and by leveraging the high-performance processor and DSP cores together with baseband accelerators optimal for both LTE and WCDMA processing, designers can improve base stations' spectral efficiency and costs.

Freescale products address the key business needs of the OEMs and wireless operators by enhancing and optimizing to the future wireless network in multiple key areas of macrocells, microcells and small cells. To achieve these enhancements, Freescale uses an array of in-house core technology innovations in baseband processing that are all designed in flexible and software upgradeable manners. Moreover, easy software migration between cores, technologies and different wireless standards delivered with commercial layer 1 software stacks for the small cells, enable fast time to market and continuous optimization for throughputs, power and costs when moving from one generation to another. Freescale is using more advanced IP and process technologies as demand for higher performance increases and as the network evolves to smaller cells and distributed antenna systems that evolve with the ever-changing standards and services needs.

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Document Number: QORIQQONVERGEWP REV 3